

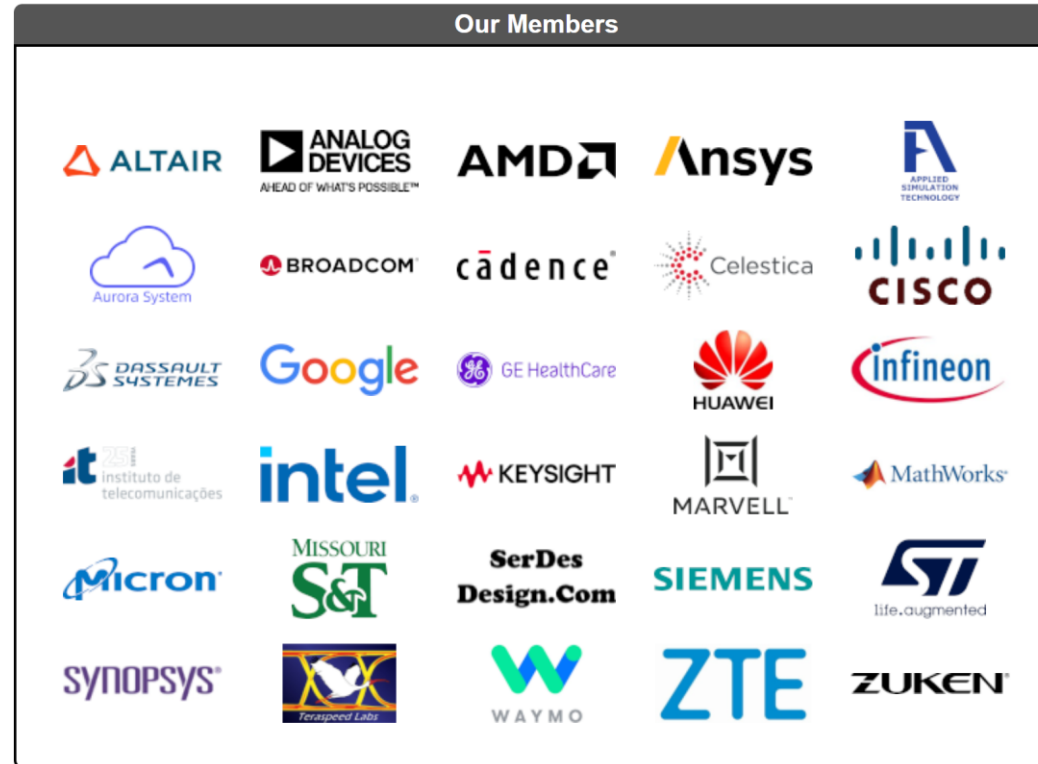
IBIS Chair's Report

Randy Wolff
Siemens EDA
Chair, IBIS Open Forum

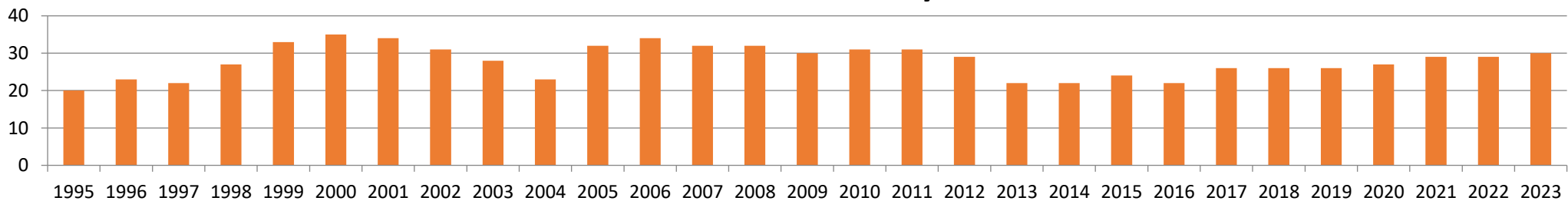
European Hybrid IBIS Summit with IEEE SPI 2023
Aveiro, Portugal
May 10, 2023



30 IBIS Members (Organization-based)



Number of Members by Year



IBIS Officers June 2022- May 2023

Chair: *Randy Wolff, Siemens EDA*

Vice-Chair: *Lance Wang, Zuken USA*

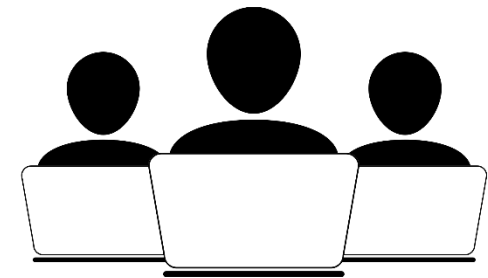
Secretary: *Graham Kus, MathWorks*

Treasurer: *Bob Ross, Teraspeed Labs*

Librarian: *Zhiping Yang, MST*

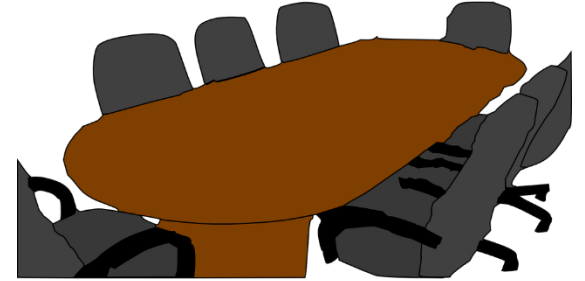
Postmaster: *Curtis Clark, ANSYS*

Webmaster: *Steve Parker, Marvell*



- Starting the election process for new officers for 2023
 - Nominations accepted May 17 through May 31
 - Seeking nominations for all roles

IBIS Meetings



- Weekly teleconferences
 - Quality task group (Tuesdays, 09:00 PT)
 - Advanced Technology Modeling (ATM) task group (Tuesdays, 12:00 PT)
 - Interconnect task group (Wednesdays, 08:00 PT)
 - Editorial task group (suspended)
- IBIS Open Forum teleconference every 3 weeks (Fridays, 08:00 PT)
- IBIS Summit meetings (USA and international)
 - DesignCon, IEEE SPI, IEEE EMC+SIPI, Shanghai, Taipei, Tokyo (JEITA-organized)
- Participants: ~280 in 2022

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, and Michael McNair
- SAE ITC provides financial, legal, and other services
- <https://www.sae-itc.com/>



Task Groups



- Advanced Technology Modeling Task Group
 - Chair: Arpad Muranyi, Siemens EDA
 - https://ibis.org/atm_wip/
 - Develop non-interconnect technical BIRDs
- Editorial Task Group
 - Chair: Michael Mirmak, Intel
 - https://ibis.org/editorial_wip/
 - Produce IBIS specification documents
- Interconnect Task Group
 - Chair: Michael Mirmak, Intel
 - https://ibis.org/interconn_wip/
 - Develop on-die/package/module/connector interconnect modeling BIRDs
- Quality Task Group
 - Chair: Bob Ross, Teraspeed Labs
 - https://ibis.org/quality_wip/
 - Oversee IBISCHK parser testing and development

BIRD = Buffer Issue Resolution Document

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1:**
 - Behavioral buffer model (fast simulation)
 - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2:**
 - Package models
 - Electrical Board Description (EBD)
- 2002-2006 **IBIS 4.0-4.2:**
 - Receiver models
 - AMS languages
- 2007-2012 **IBIS 5.0-5.1:**
 - IBIS-AMI SerDes models
 - Power-aware model



Celebrating 30 Years in 2023!

I/O Buffer Information Specification

- 2013-2015 **IBIS 6.0-6.1:**
 - PAM4 multi-level signaling
 - Power delivery package models
- 2019 **IBIS 7.0:**
 - Back-channel time-domain support
 - Interconnect modeling using IBIS-ISS and Touchstone
- 2021 **IBIS 7.1:**
 - DDRx IBIS-AMI support
 - Electrical Module Description (EMD)
 - IBIS-AMI back-channel statistical optimization
- 2023 **IBIS 7.2:**
 - Redriver simulation flow fixes
 - PAMn IBIS-AMI support

Other Work

- 1995: **ANSI/EIA-656 (IBIS 2.1 International standard)**
- 1999: **ANSI/EIA-656-A (IBIS 3.2 International standard)**
- 2001: **IEC 62014-1 (IBIS 3.2 International standard)**
- 2003: **Interconnect Model Specification (ICM 1.0)**
- 2006: **ANSI/EIA-656-B (IBIS 4.2 International standard)**
- 2009: **Touchstone 2.0**
 - Official Touchstone donated from Agilent/Keysight
- 2011: **IBIS-ISS 1.0 (Interconnect SPICE Subcircuit)**
 - Subset of HSPICE
- **IBISCHK:** IBIS file syntax parser
 - Current version 7.2.0
 - Source code available for purchase
 - Compiled executables available free of charge
- **TCHK2:** Touchstone 2.0 file syntax parser
 - Current version 2.0.1
 - Source code available for purchase
 - Compiled executables available free of charge

What's Next for IBIS?

- IBIS Open Forum's task groups are discussing these topics:
 - Expanded system-level perspective
 - Clock/data relationships, timing information, equalization training
 - Power Integrity focused modeling
 - Improved Power Supply Induced Jitter (PSIJ) modeling (BIRD220 and others)
 - Chip-level Standard Power Integrity Model (SPIM, BIRD223)
 - Voltage regulator, diode, and inductor models
 - Multi-level analog buffer modeling
 - Interconnect Modeling
 - Touchstone 3.0 with Pole/Residue and port mapping support
 - Touchstone 1.x expansions
 - IBIS-ISS expansions
 - What else should we be looking at? Bring your ideas!

Participation in IBIS

- The success of IBIS depends on active participation and volunteering
- Bringing your ideas and talents to IBIS
 - Task groups for technical discussions and document editing
 - IBIS email reflectors
 - Open Forum teleconferences for event planning and voting
 - Summit presentations
 - IBIS Board and task group volunteering
 - Writing BIRDs – Buffer Issue Resolution Documents
 - Official method for submitting a proposed change to the IBIS specification
 - Many developed collaboratively in task groups
 - Discussed and voted on in Open Forum meetings



IBIS Board Opportunities

- Nominations of IBIS officers in late May
- New board positions start mid-June
- All positions are open
- Potential to modernize board positions
 - Currently: Chair, Vice-chair, Secretary, Treasurer, Librarian, Webmaster, Postmaster, and University Relations (not listed in Policies & Procedures)
 - Better alignment with needs: Chair, Vice-chair/Summits Lead, Secretary, Treasurer/Membership, Web/Email, Software Lead, University Relations
 - Requires change to Policies & Procedures
- Remember the importance of mentoring younger engineers and encouraging them to participate in IBIS

IBIS Website Resources

IBIS Summits

Task Group Info

Member FAQ

Spec documents

*IRDs

Email support

Syntax Parser
Downloads

The screenshot shows the IBIS Open Forum website. At the top, it says "Welcome to the IBIS Open Forum". Below this, there are three news items, each starting with "NEW":

- [IBIS Celebrates 30 Years!](#)
- [IBIS 7.2 Specification](#) approved and available for download.
- IBIS 7.1 Parser IBISCHK7.1.1 is now available: [IBISCHK7](#)

Below the news items is a section titled "Our Specifications" with a table of specifications:

Our Specifications	
I/O Buffer Information Specification	(IBIS 7.2) (SAE/EIA-STD-656-B) (IEC-62014-1)
IBIS Interconnect Modeling Specification	(ICM 1.1) (SAE/GEIA-STD-0001)
IBIS Interconnect SPICE Subcircuit Specification	(IBIS-ISS 1.0)
Touchstone® File Format Specification	(Touchstone 2.0)

Below the specifications is a section titled "Our Members" displaying a grid of logos for various companies and organizations, including:

- ALTAIR, ANALOG DEVICES, AMD, Ansys, APPLIED SIMULATION TECHNOLOGY
- Aurora System, BROADCOM, cadence, Celestica, CISCO
- DASSAULT SYSTEMES, Google, GE HealthCare, HUAWEI, infineon
- instituto de telecomunicações, intel, KEYSIGHT, MARVELL, MathWorks
- Micron, MISSOURI S&T, SerDes Design.Com, SIEMENS, life.augmented
- SYNOPSYS, Teraspeed Labs, WAYMO, ZTE, ZUKEN

On the left side of the website, there is a navigation menu with the following items:

- Upcoming Events
- Past Summits
- Open Forum
 - Minutes
- Regional Forums
 - China
- Task Groups
 - ATM
 - Quality
 - Interconnect
 - Editorial
- Members
 - FAQ
 - Roster
- Specifications
 - BIRDs
 - ISSIRDs
 - TSIRDs
- Models
- Support
 - Model Review
 - Training
- FREE Tools
- IBIS Parsers
 - IBISCHK
 - IBISCHK Bugs
 - TSCHK
 - TSCHK Bugs
- IBIS Cookbook
- Accuracy Handbook
- Site Map
- About IBIS
 - Articles
 - FAQ

[Thank You]



IBIS Open Forum:

Web: <https://ibis.org>

Email: info@ibis.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.