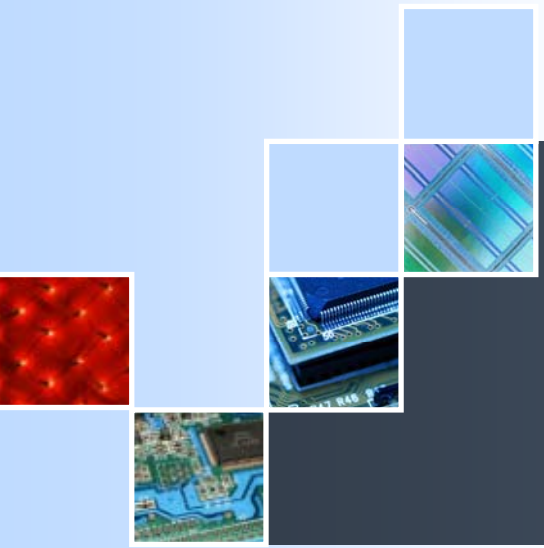

IBIS for SSO Analysis

Asian IBIS Summit, November 15, 2010

(Presented previously at Asian IBIS Summits, Nov. 9 & 12, 2010)

Haisan Wang

Joshua Luo

Jack Lin

Zhangmin Zhong

SIGRITY

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- Traditional I/O SSO Analysis
- Buffer Model in SSO Simulation
- BIRD95 Introduction
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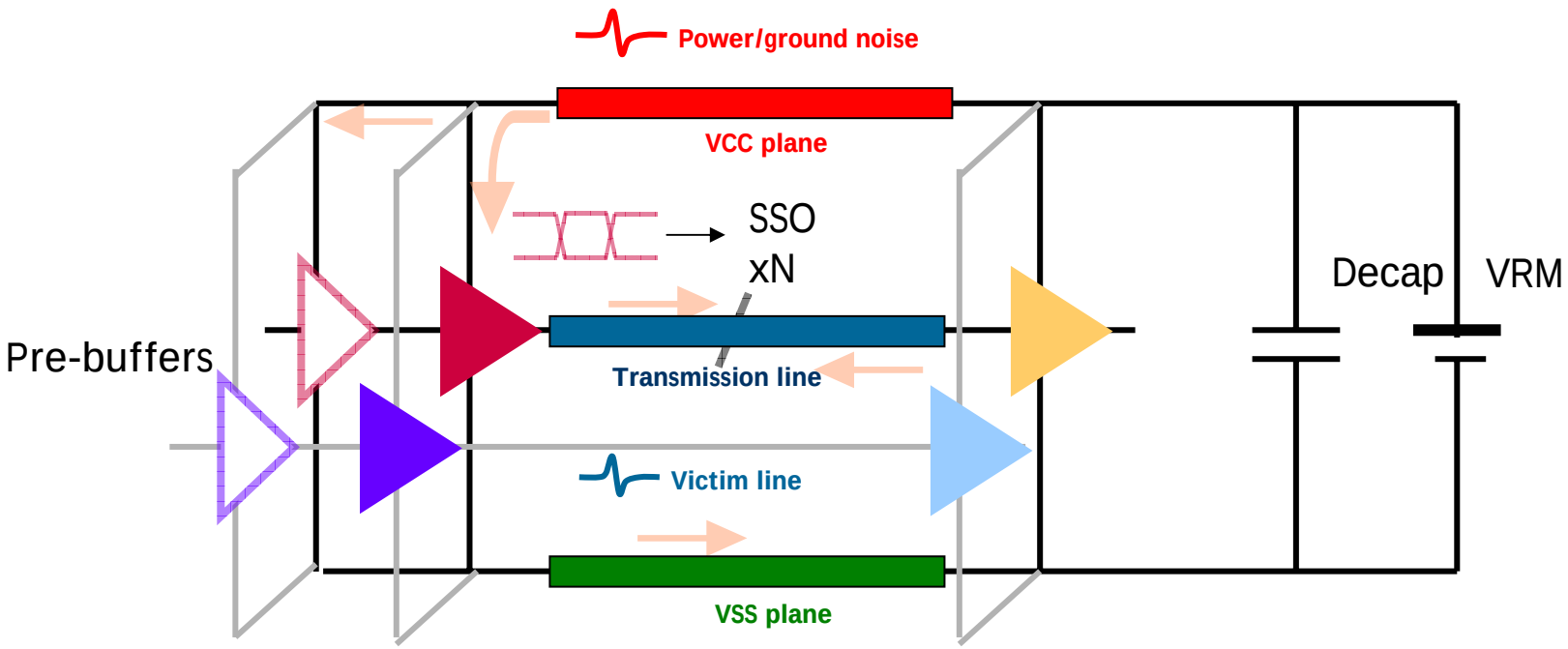
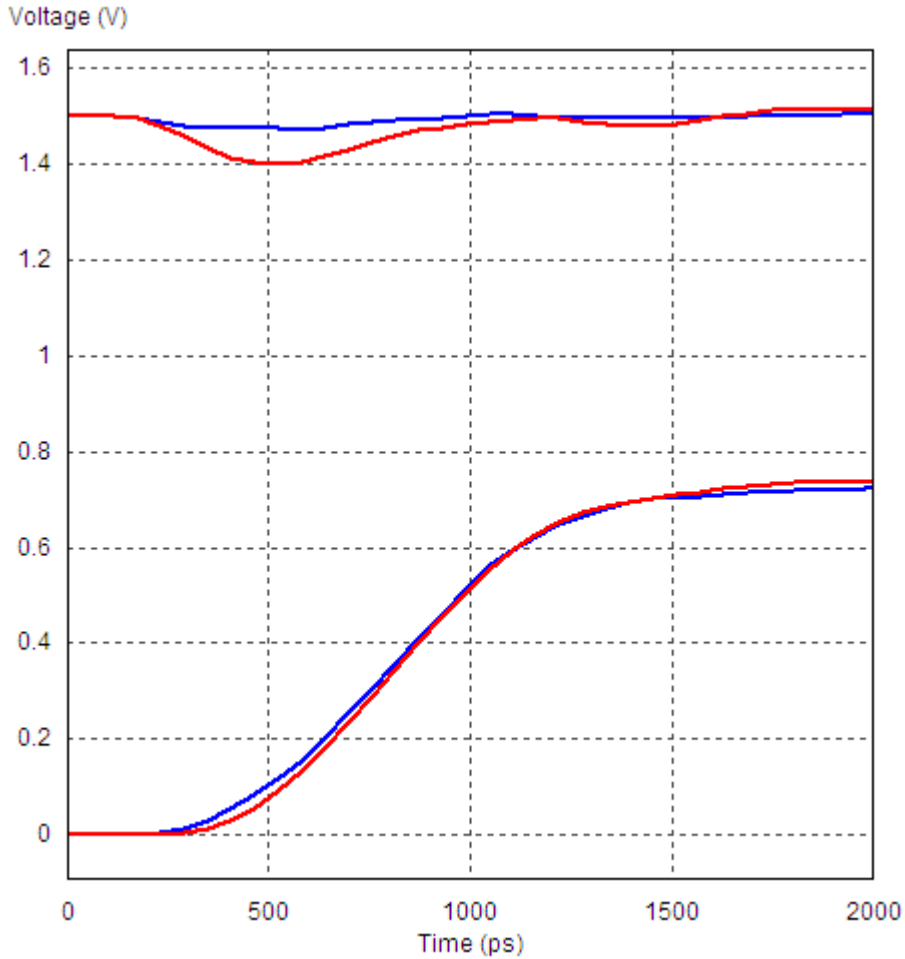
Traditional I/O SSO Analysis

- **The SSO/SSN problem:**
  - **PDN noise**
  - **Crosstalk**



Fundamentals of I/O SSO Mechanisms

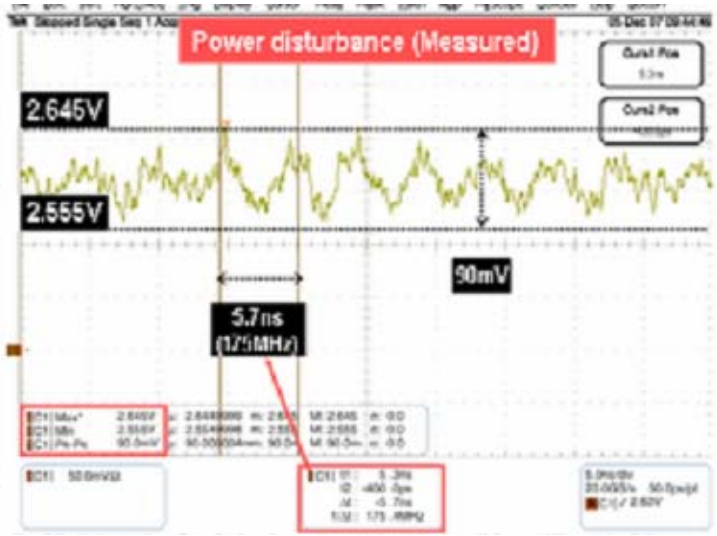
- SSO is a combination of signal and power integrity issues
- Affects signal edge rate, timing and voltage margins
- System-level issue involving both packages and PCBs
- Multiple signal net crosstalk mechanisms – trace / via / pin
- Two components of PDS noise
  - PDS current supplied to devices
  - Return currents from I/Os
- BGA inductance presents a fundamental limitation on the PCB's PDS freq. range; the package is responsible for decoupling above that freq. region
- PCB layout can only do so much – it cannot solve package design problems

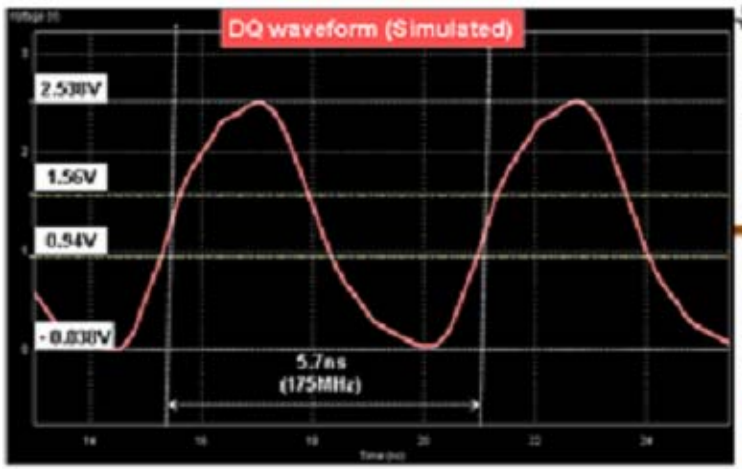


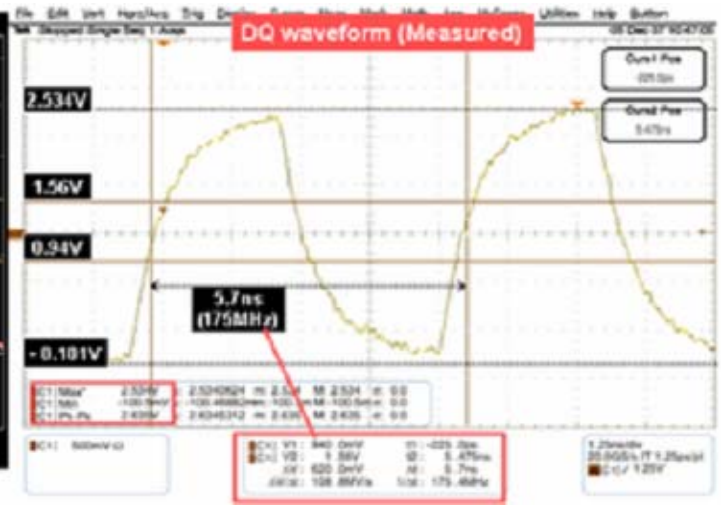
Blue – Single I/O switching results

Red – Two I/Os switching results

Case： DDR simulation VS measurement







Refer to: "http://www.sigrity.com/papers/2008/65nm%20DDR%20IO%20Paper%20May%202008.pdf "

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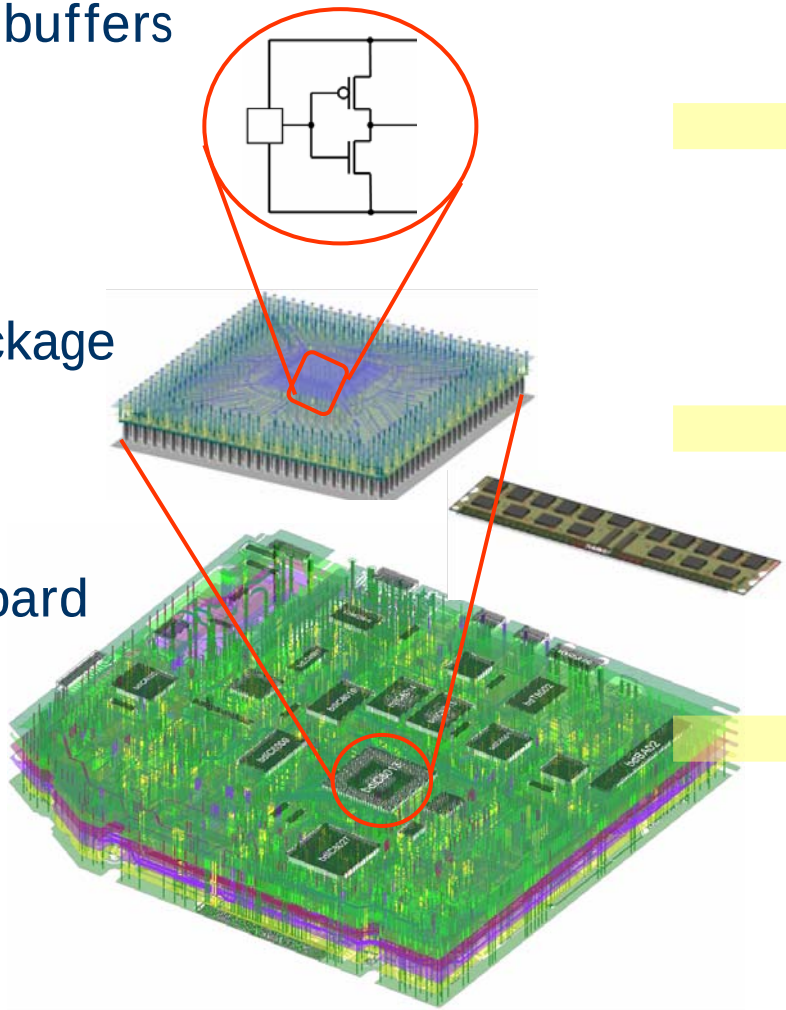
Components for SSO Simulation

IO buffers

Package

Board



Circuit simulation

EDA Tool

System/set vendors need to obtain IO models from IC vendors.

Circuits

- Equivalent circuits
- S-parameters

-Design (geometry)
- Equivalent circuits
- S-parameters

S-parameters

Design (geometry)

Trade-off in IO buffer model

	SPICE transistor level model	IBIS model
Contents	▪ Detailed circuits and netlists ▪ Device library, parameters ▪ Related deign information	▪ I-V/V-T for the final stage ▪ Pin information
Accuracy	Very good	▪ Good for SI ▪ ? for PI
Format	▪ Usually, encrypted for outside IC vendors. ▪ Usually, NDA is necessary.	▪ Text file ▪ Open format
Simulation time	Typically, several to 10 times slower than IBIS	Much faster than SPICE model
EDA tools Utilization	Specific simulator is necessary for encrypted models	Many SI/PI tools support.

There may be some other choices, such as the current mirror circuit or VCR

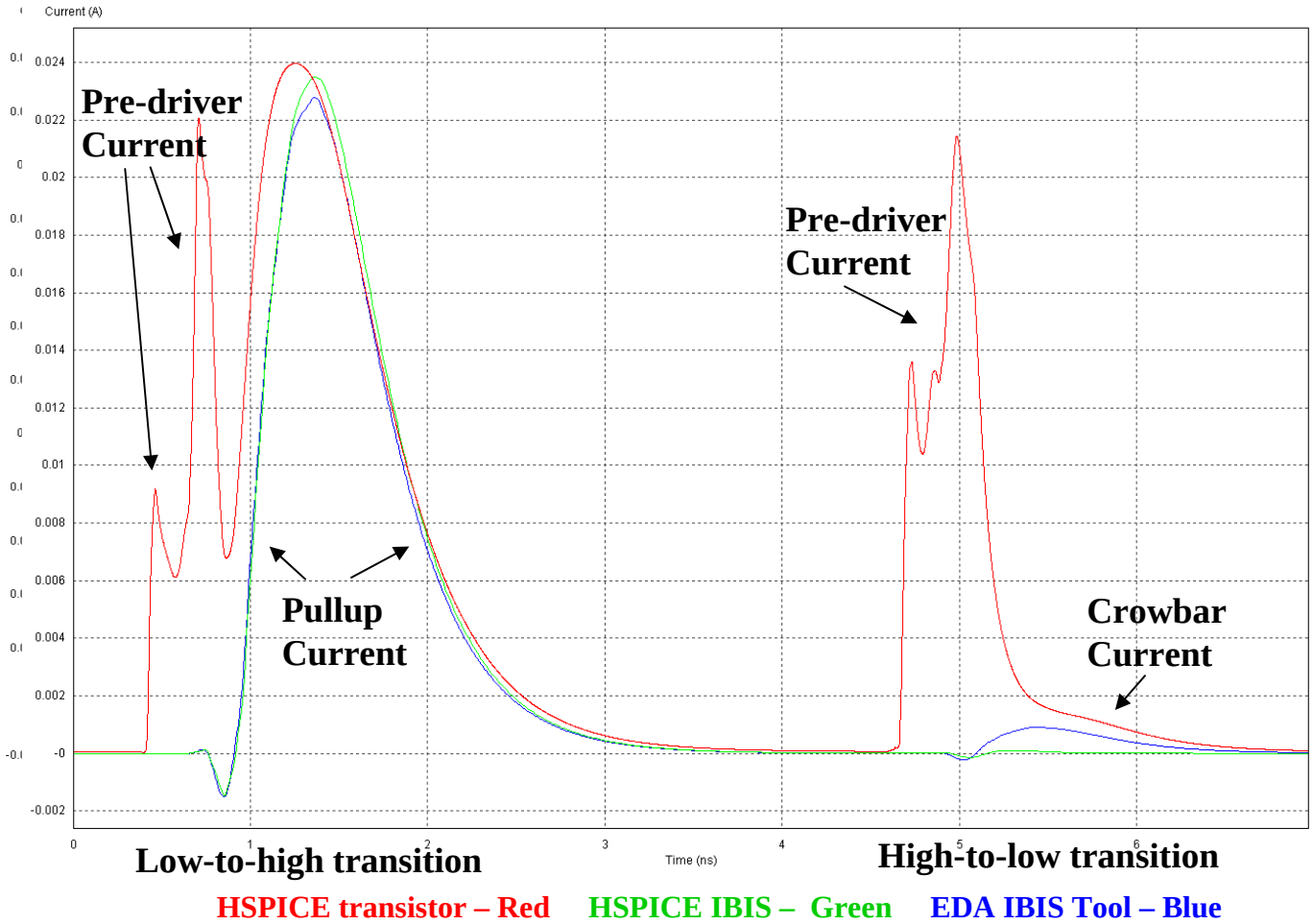
Requirements in SSO Simulation

- Easy setup
  - Hope to eliminate painful manual work
- Fast runtime
  - Want to test various conditions (corners, stimulus, …)
  - Want to promptly reflect package/board design change

→ SPICE transistor model may not fit.

→ What about IBIS model ?

Comparison of IBIS and SPICE total VDDQ current



HSPICE transistor – Red HSPICE IBIS – Green EDA IBIS Tool – Blue

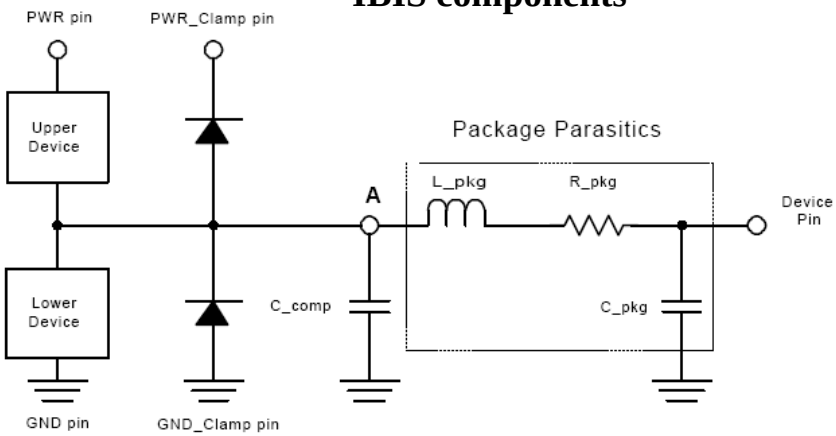
The total VDDQ current for the transistor-level model is significantly different from its pullup component. There is a large amount of pre-driver current due to crowbar effects and gate capacitance charging.

Pre-driver current occurs significantly earlier than the pullup current. The pre-driver current is rapidly decreasing as the pullup is turning on.

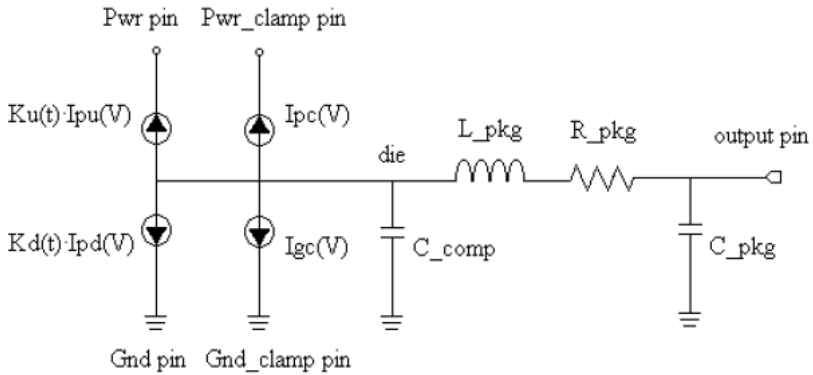
The pre-driver current peaks almost as high as the pullup current. Note that the dI/dt of the pre-driver is much larger than that of the pullup current.

Currents that IBIS can calculate

IBIS components



Analog Model of an IBIS output



- The pullup and pulldown components are modeled as voltage controlled current sources
- The instantaneous value for each voltage controlled current source is derived from the I/V tables and is scaled based on the information in the V(t) tables
- The voltage controlled current sources are simultaneously active to model crowbar
- Crowbar current can be approximated fairly well if all four V(t) tables are present in the IBIS file
- **Pre-driver Current is missing!!!**

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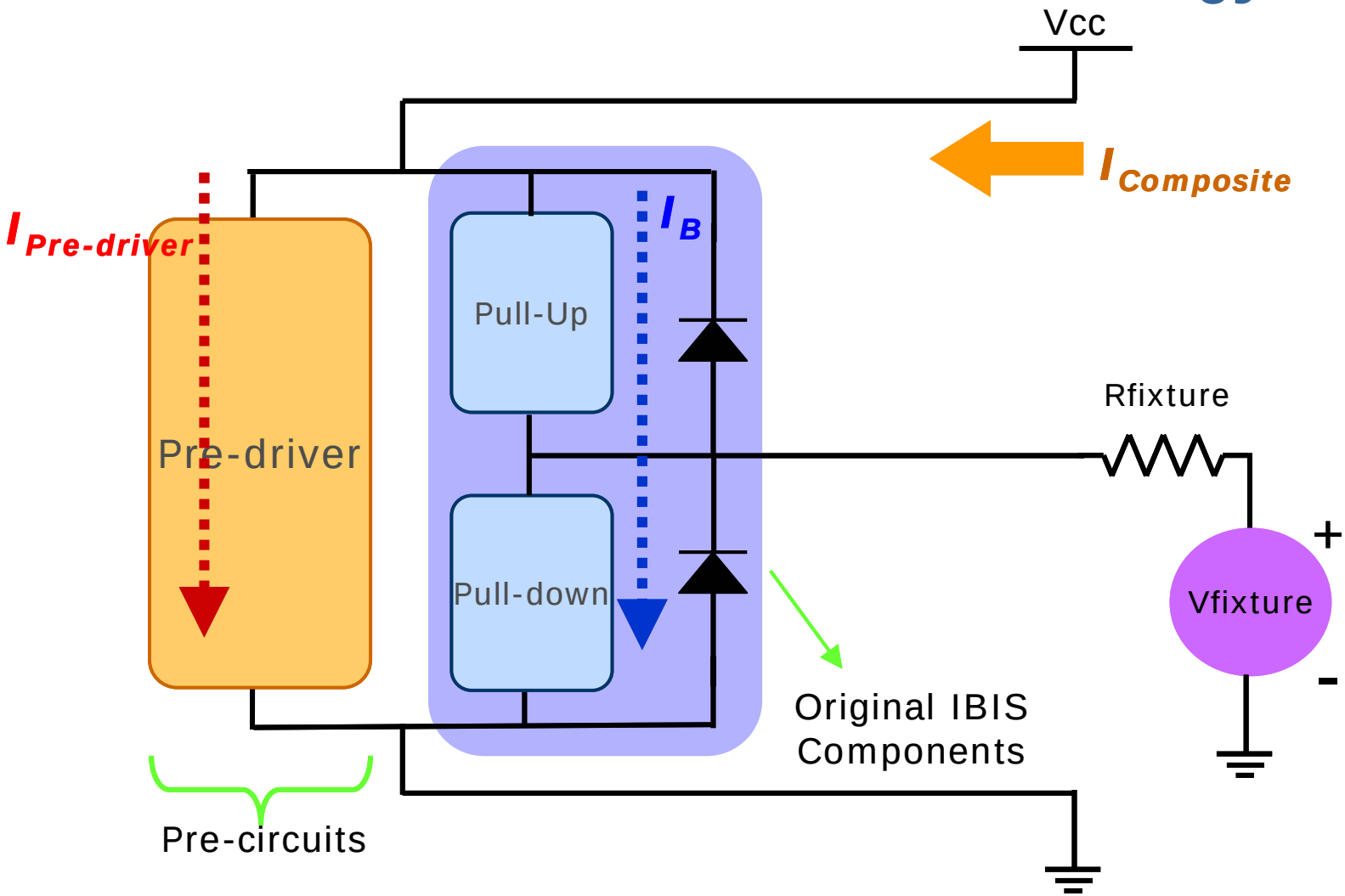
Overview of BIRD95 Methodology



- A new composite current $I_{Composite}$ will be provided to show total P/G currents, based on transistor simulation, for better P/G noise simulation

Description of Composite Current

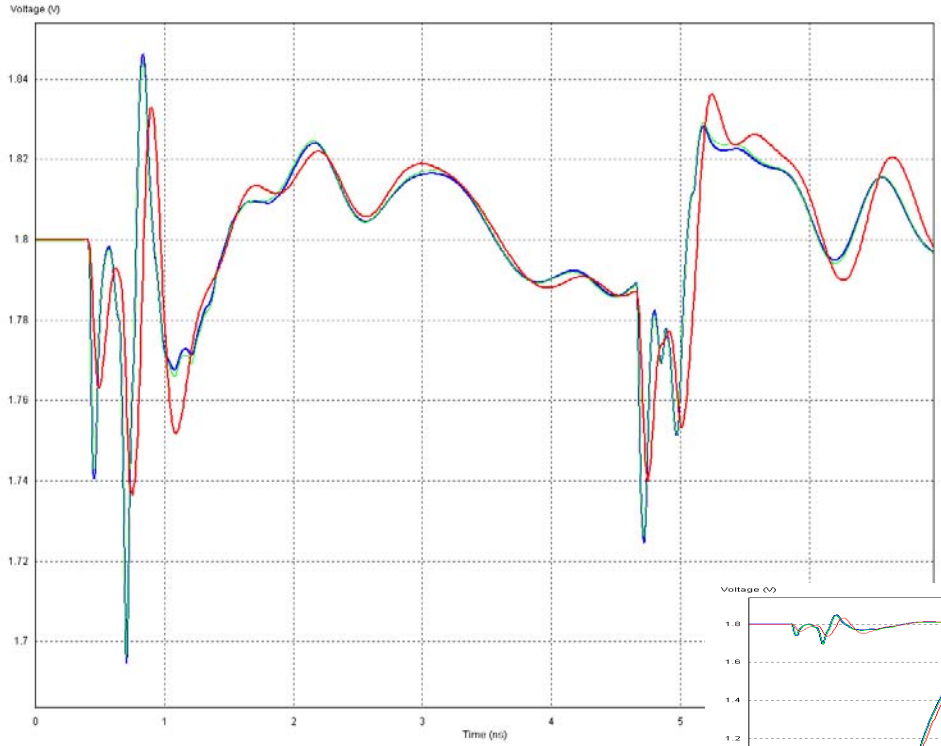
- Time table
- Synchronization is needed to [Rising/Falling Waveform]

```
[IBIS ver]        5.0
...
[Composite Current]
|
| Time                I(typ)              I(min)       I(max)
|
0.00000E+00         7.17370E-06         NA           NA
2.00000E-11         7.16590E-06         NA           NA
4.00000E-11         7.15820E-06         NA           NA
6.00000E-11         7.15040E-06         NA           NA
8.00000E-11         7.14270E-06         NA           NA
1.00000E-10         7.13490E-06         NA           NA
...
```

How Simulator handle IBIS with $I_{Composite}$?

- Obtain composite currents $I_{Composite}$ from IBIS file (version 5.0)
- Obtain I_B from regular IBIS simulation during pre-simulation
- Obtain $I_{Pre\text{-}driver}$, Using
  - $I_{Pre\text{-}driver}(t) = I_{Composite}(t) - I_B(t)$
- Add $I_{Pre\text{-}driver}(t)$ as PWL current source in parallel with IBIS B element model

Voltage waveforms for the new methodology

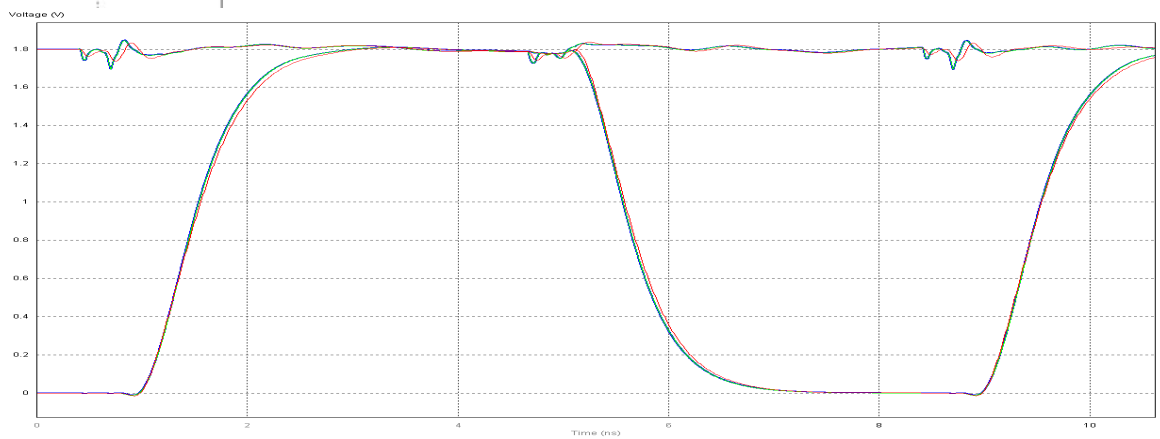


The new IBIS methodology is now able to model the pre-driver and final drive stage currents. Correlation with the SPICE results is significantly improved over the IBIS-only results.

Waveforms from both IBIS simulations were very similar. No artifacts were observed.

Note that the IBIS waveforms overestimate the peak-peak SSO magnitude and occur slightly before the SPICE peaks. The cause can be found by examination of the current waveforms.

SSO waveforms with realistic PDS, 10 pF driver load, PWL I(t) in parallel with the IBIS device

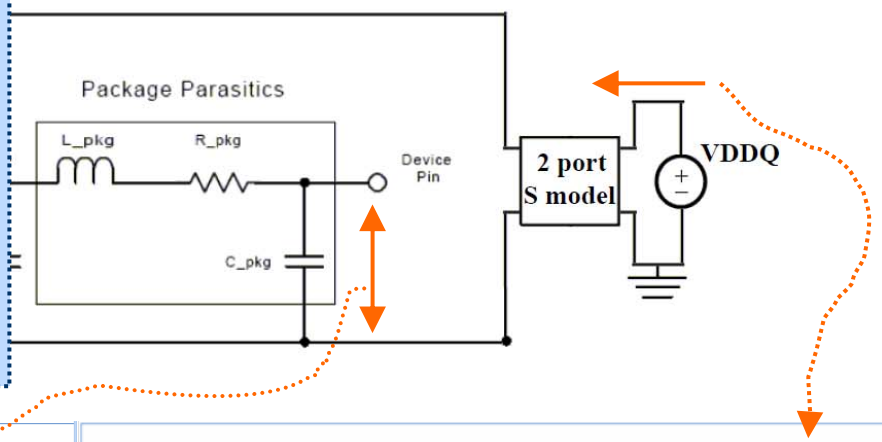


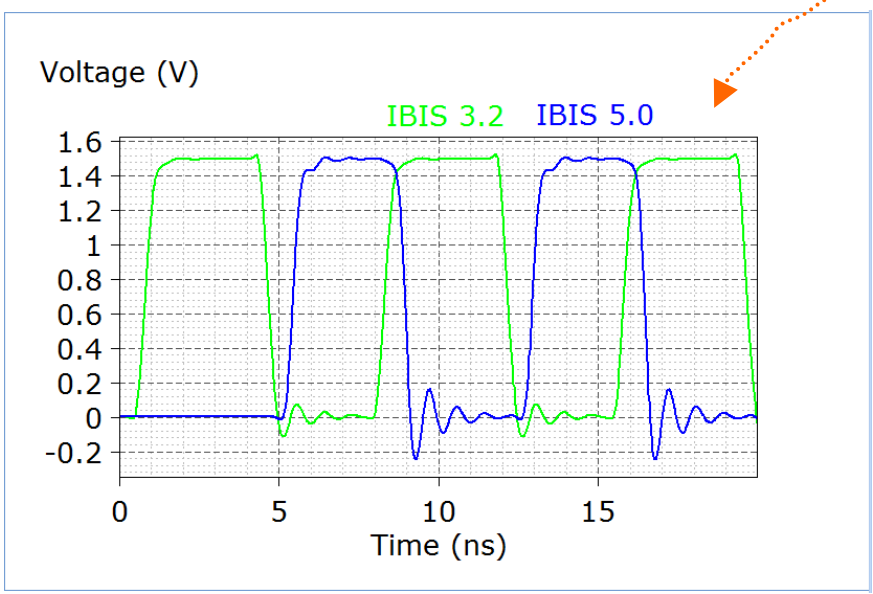
HSPICE transistor – Red HSPICE IBIS – Green EDA IBIS Tool – Blue

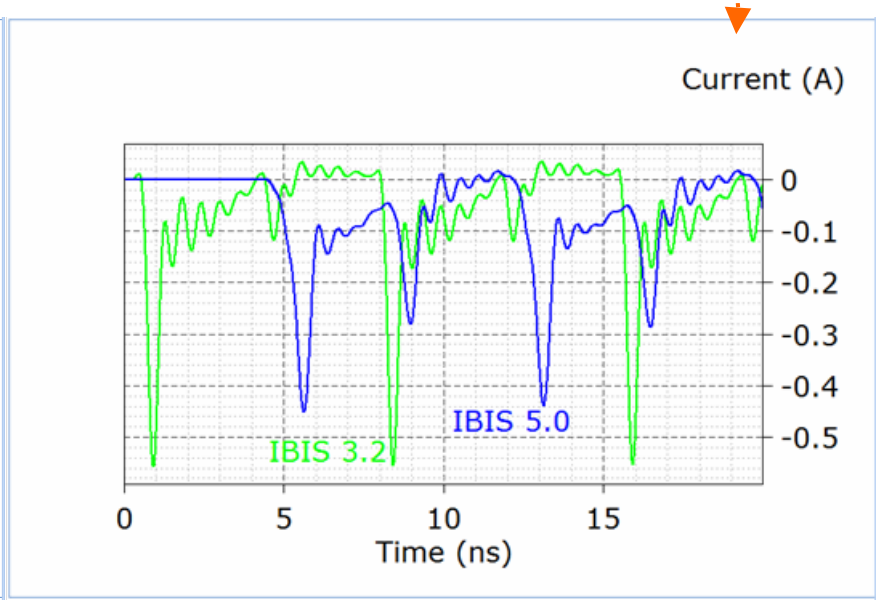
IBIS 5.0 vs IBIS 3.2

IBIS 3.2
→No Composite Current

IBIS 5.0
→ with Composite Current

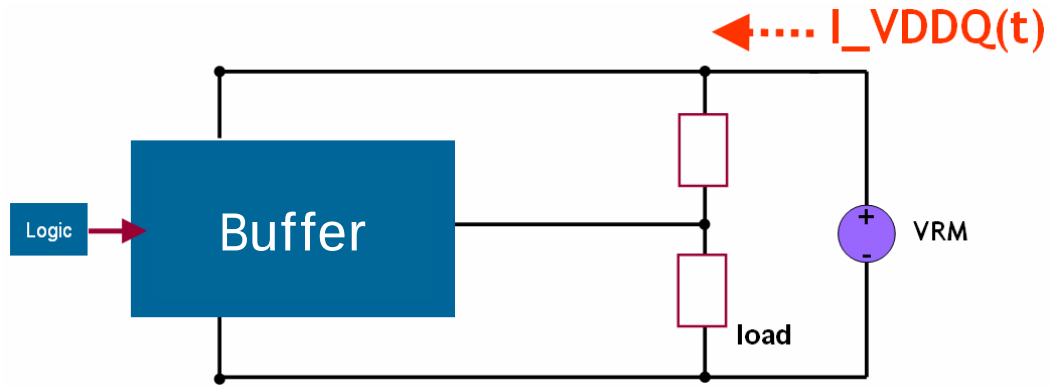


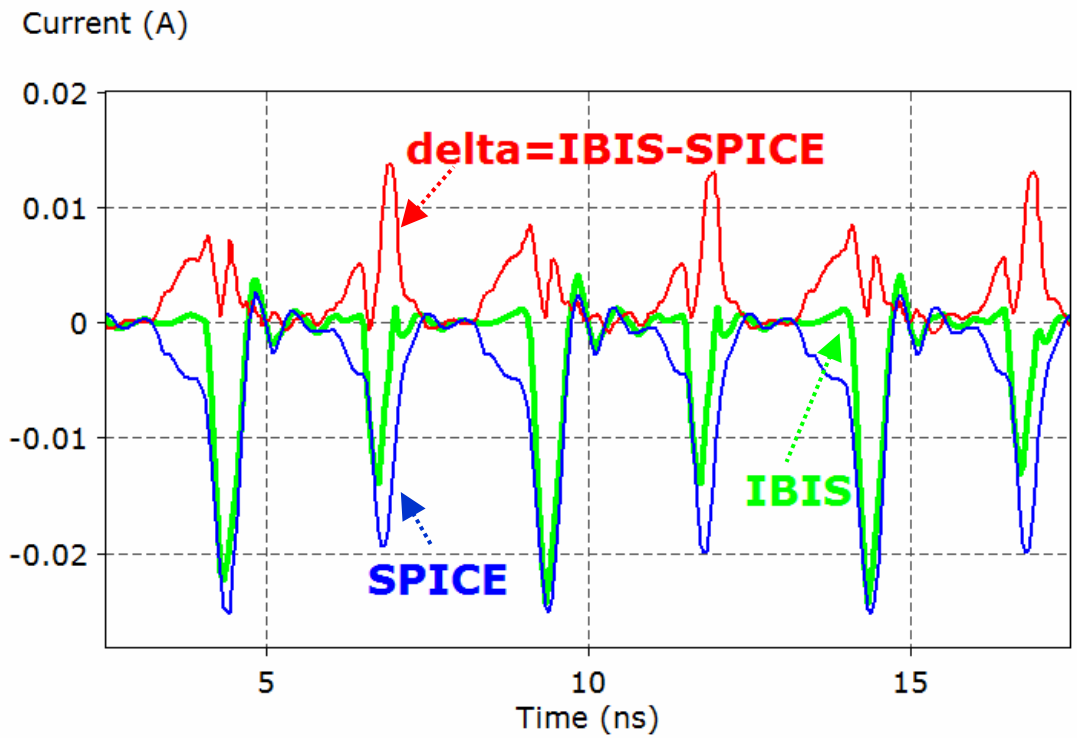




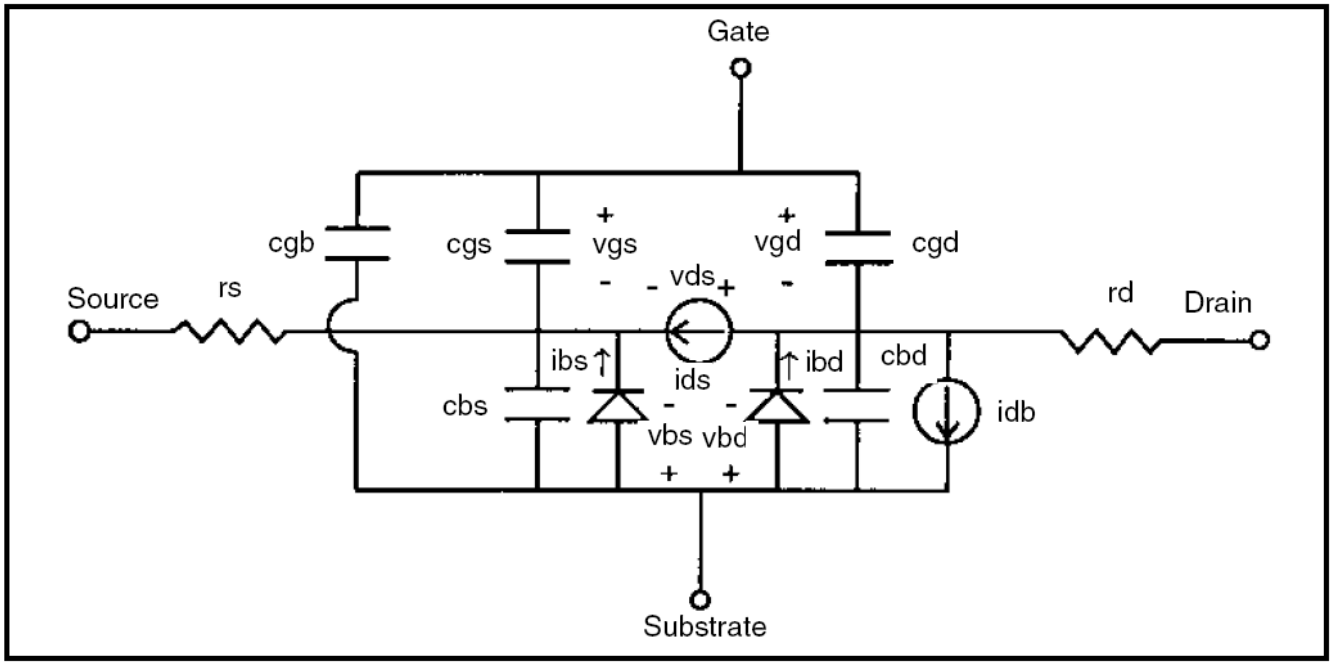
Power Current Difference

Test Circuit
Simulation : HSPICE
Buffer : DDR2-400 DQ
Load : Open



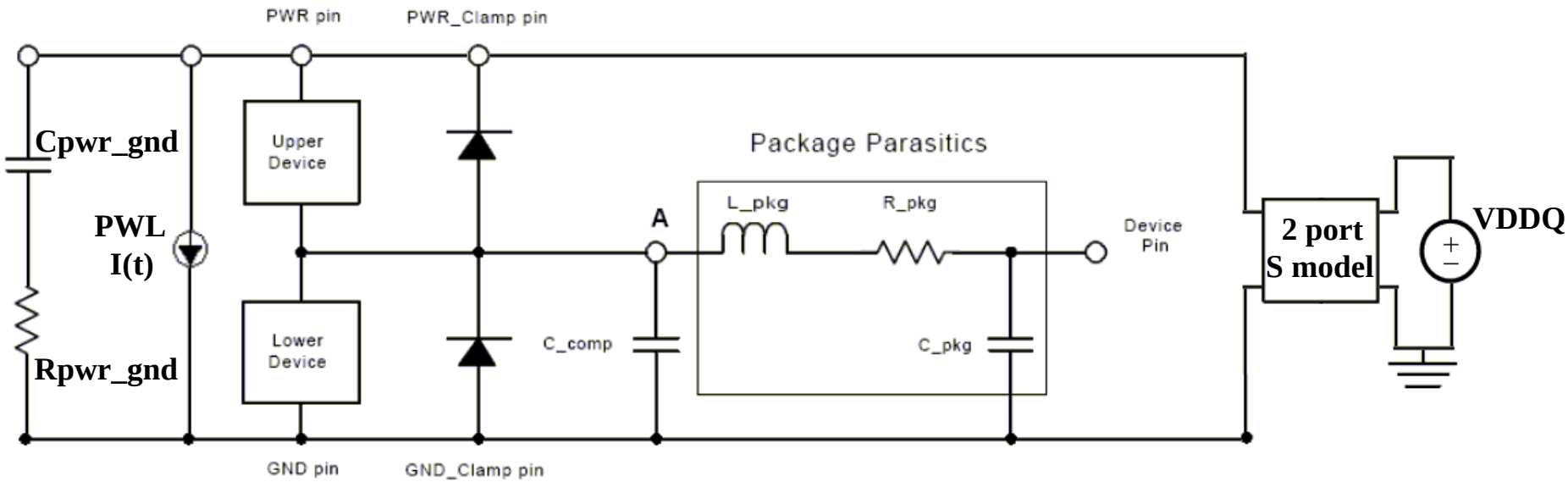


What is the model missing?



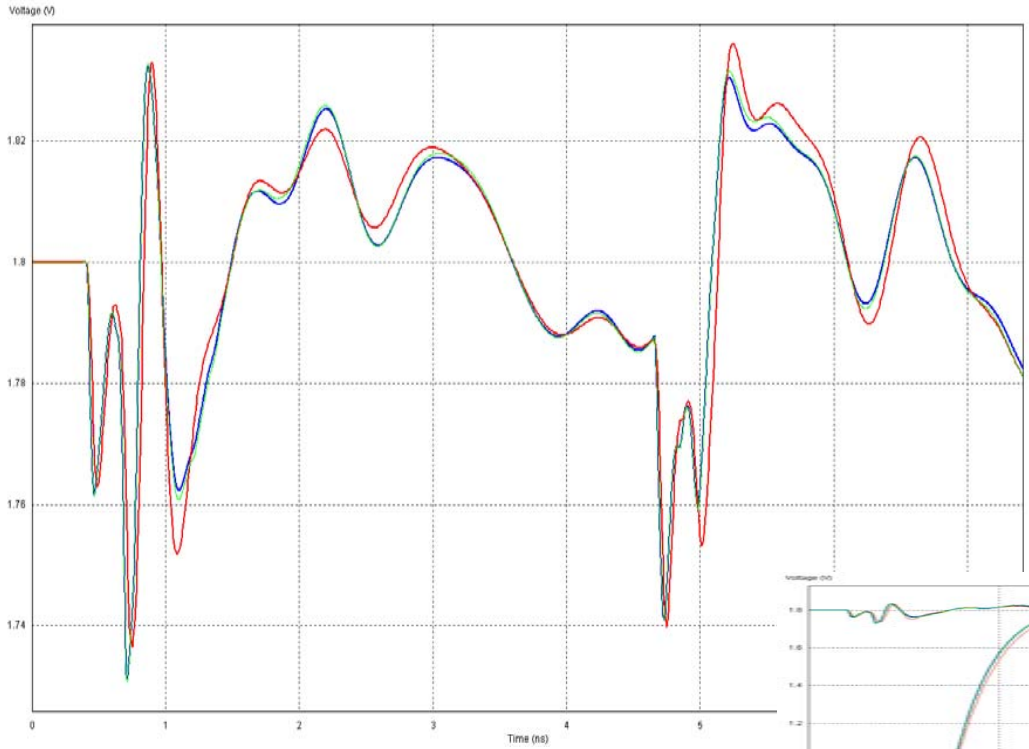
- Parasitic capacitance exists between all MOSFET terminals
- For the I/O pin, this is modeled in IBIS by C_comp
- A new compensation capacitor is needed for the power and ground parasitics to maximize SSO correlation with realistic PDS models

Suggested schematic to maximize correlation



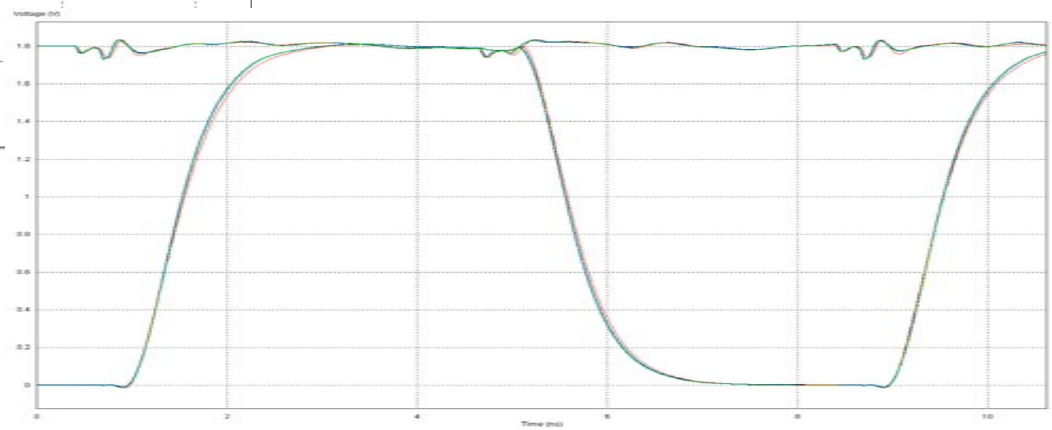
- A frequency domain analysis was performed to determine the impedance between power and ground for the transistor level model
- The impedance was curve fit to a series RC circuit for time domain analysis
- This circuit was added in parallel to the PWL current and IBIS driver

Voltage waveforms for the suggested improvement



The IBIS simulations now show excellent correlation with the SPICE results over the full simulation. With the addition of the RC circuit, the oscillations occur at the proper frequencies and the SSO magnitude is correct.

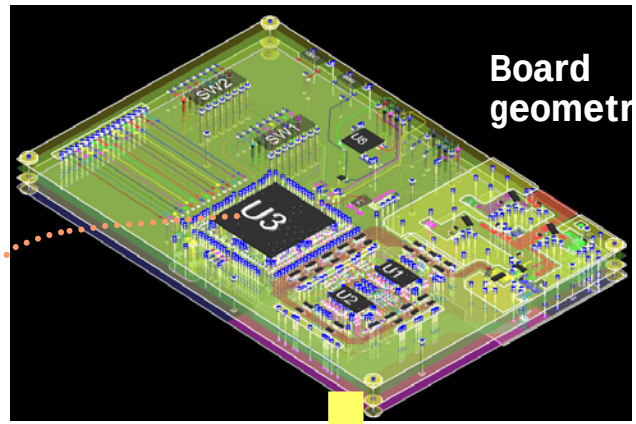
As before, waveforms from both IBIS simulations were similar and no artifacts were observed.



SSO waveforms with realistic PDS, 10 pF driver load, PWL I(t) and RC circuit in parallel with IBIS device

HSPICE transistor – Red HSPICE IBIS – Green EDA IBIS Tool – Blue

SSO Simulation with IBIS Model



Package
RLC

Simulation Model

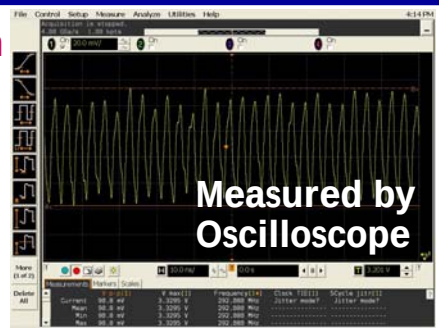
Die PDN capacitance
C=7nF
Measured by TDR

Receiver

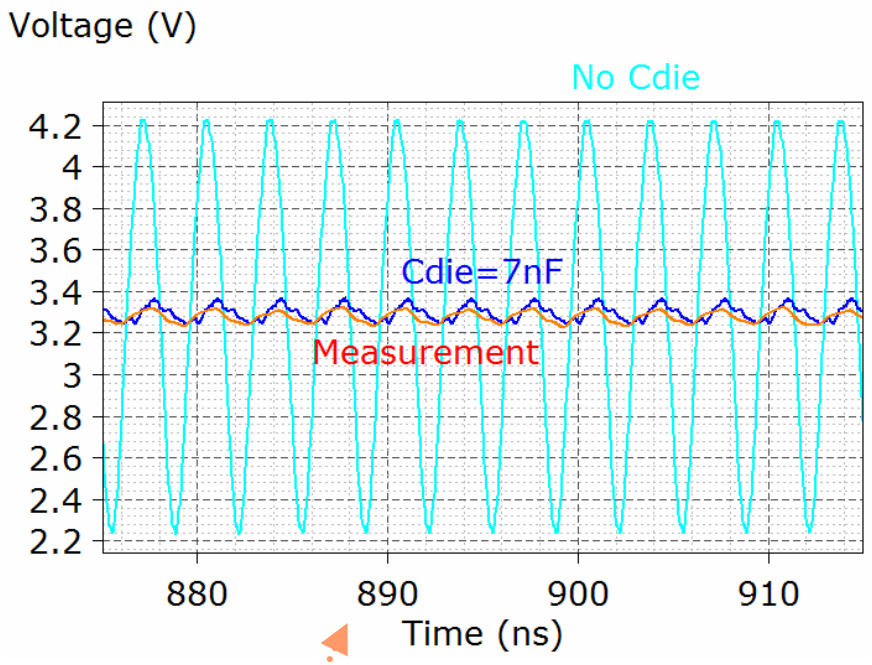
D0-15

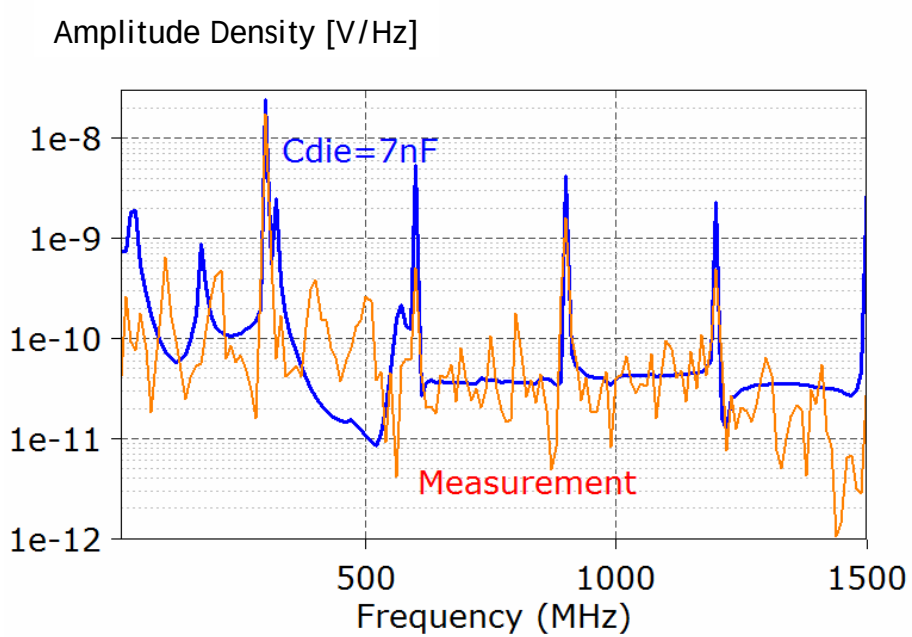
3.3V

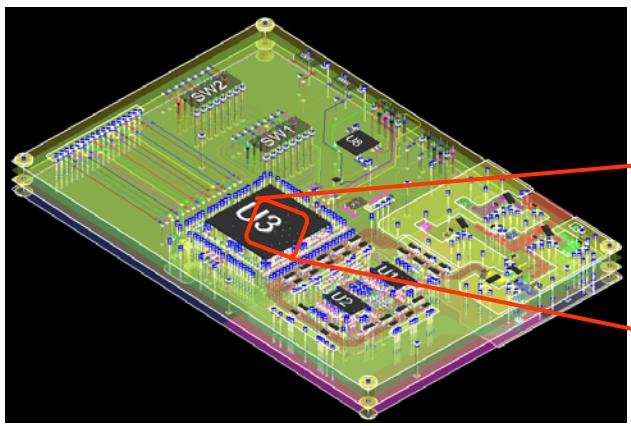
VDD-VSS voltage fluctuation
monitored underneath
the package

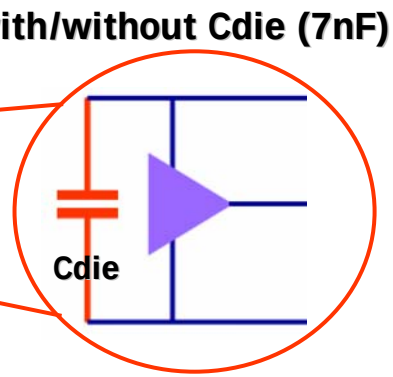


Comparison : w/wo Die PDN Capacitance









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Summary

- C_die value show a great impact on accuracy
- IBIS 5.0 improves accuracy in SSO simulation
  - $I_{Composite}$ extractions are relatively easy to generate
  - $I_{Pre\text{-}driver}$ can be calculated by $I_{Composite}$ and I_B
- IBIS model run with high efficiency and easy setup

Thank You!