
Modeling the On-die De-cap of IBIS 5.0 PDN-aware Buffers

Lance Wang, lwang@iometh.com

IO Methodology Inc.

Randy Wolff, rrwolff@micron.com

Micron Technology

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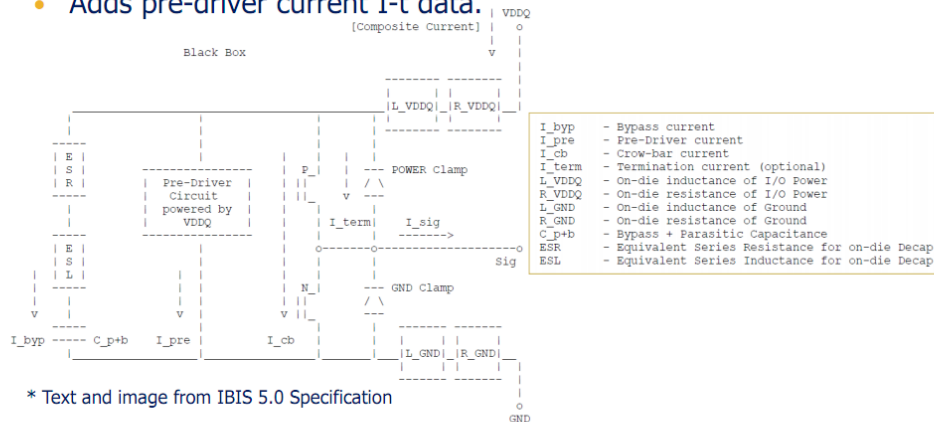
Outline

- Introduction to IBIS 5.0 PDN modeling
- On-die de-coupling circuit
- A test case and workaround
- An issue?
- Conclusions

Introduction to IBIS 5.0 PDN Modeling

[Composite Current]

- Describes the shape of the rising and falling edge current waveforms from the power reference terminal of the buffer*.
- Adds pre-driver current I-t data.



* Text and image from IBIS 5.0 Specification



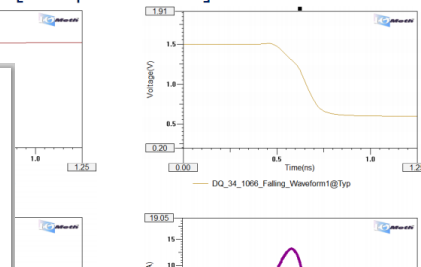
June 7, 2011



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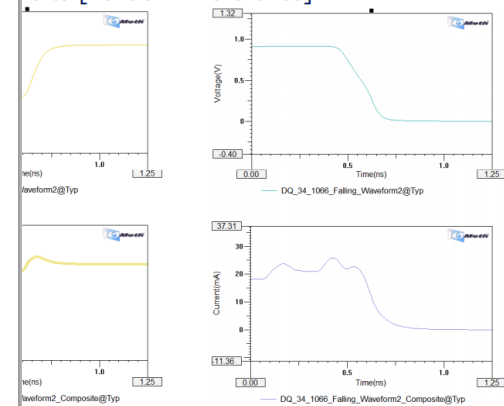
[Composite Current] Data

- Load = 50 ohms to [Pullup Reference]



[Composite Current] Data

ns to [Pulldown Reference]



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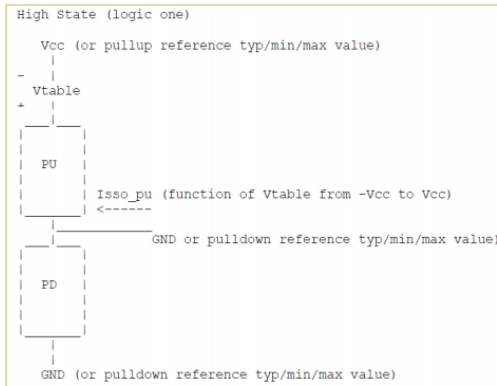
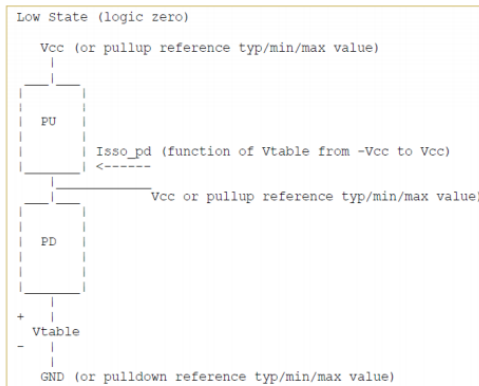


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Introduction to IBIS 5.0 PDN Modeling

[ISSO PU] & [ISSO PD]

- Data tables define the effective current of the pullup/pulldown structures of a buffer as a function of the voltage on the pullup/pulldown reference nodes*.
- Adds modeling of the gate modulation effect on driver current (I_{DS} vs. V_{GS}).



* Text and image from IBIS 5.0 Specification

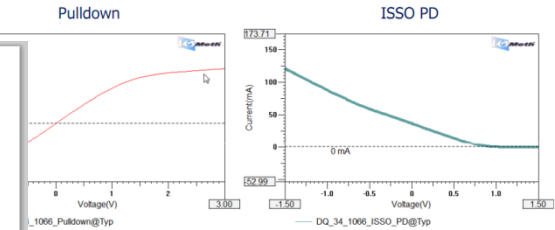


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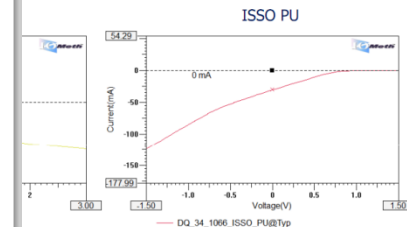
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[ISSO PD] Data



Name: DQ_34_1066_Pulldown@Typ Type: Crossing Y		Name: DQ_34_1066_ISSO_PD@Typ Type: Crossing Y	
X	Y	X	Y
1.500000e+000	3.697962e-002	0.000000e+000	3.713536e-002

ISSO PU Data

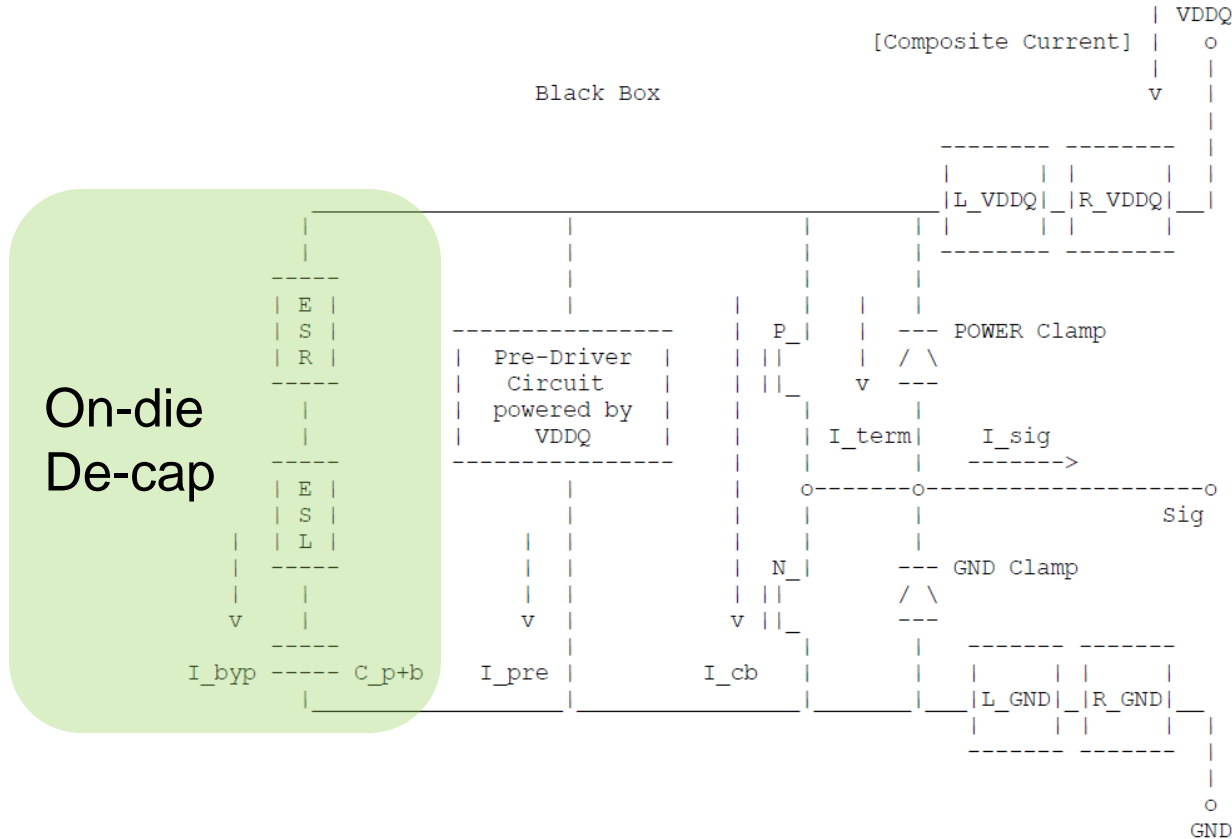


Name: DQ_34_1066_ISSO_PU@Typ Type: Crossing Y		Name: DQ_34_1066_ISSO_PU@Typ Type: Crossing Y	
Y	X	Y	X
-3.012817e-002	0.000000e+000	-3.016485e-002	

Introduction to IBIS 5.0 PDN Modeling

- IBIS 5.0 PDN modeling features are useful for SSN sensitive system designs
 - Parallel interfaces, Low power systems
 - Standard compliance models are interoperable and IP protected
- IBISCHK5 is up-to-date
 - Version 5.0.7 fixes BUG129
- At least 4 EDA simulators have implemented IBIS 5.0 PDN features
 - And more coming ...

On-Die De-Coupling Circuit

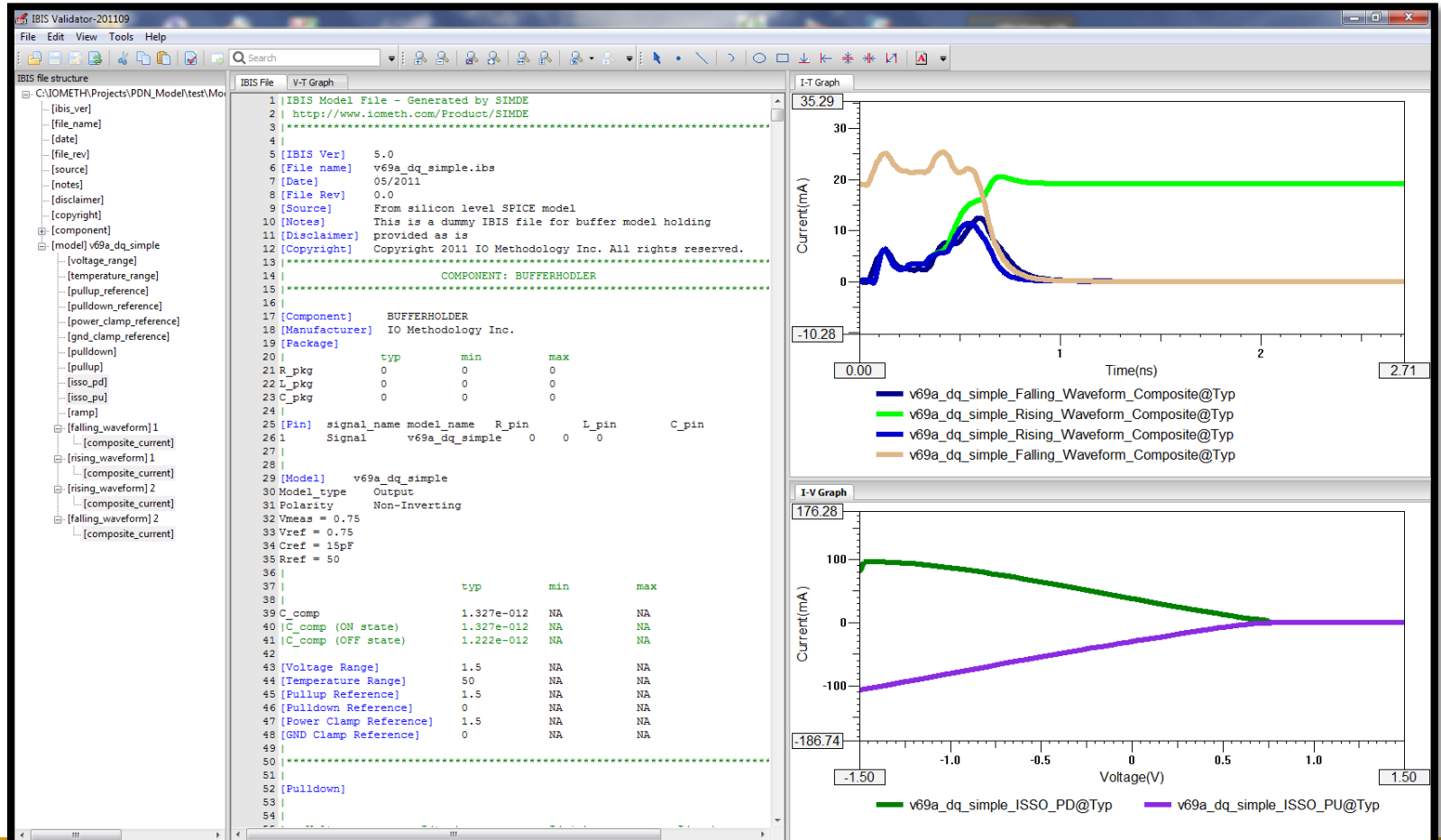


- De-cap may be on the order of 500pF per buffer

* Image from IBIS 5.0 Specification

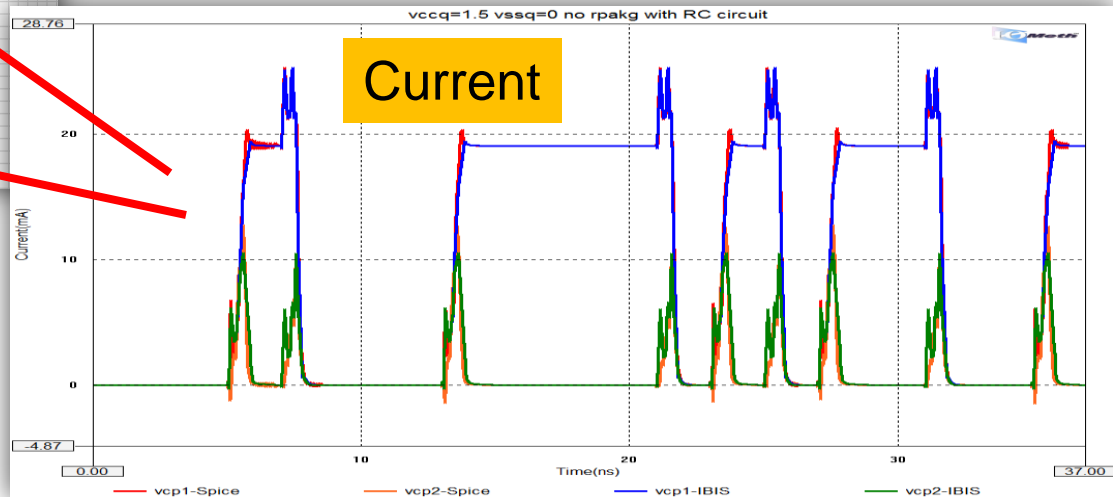
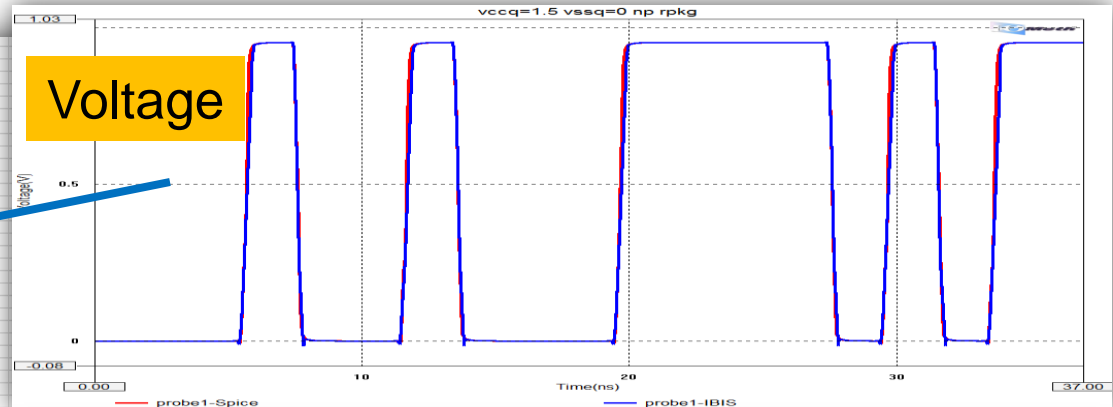
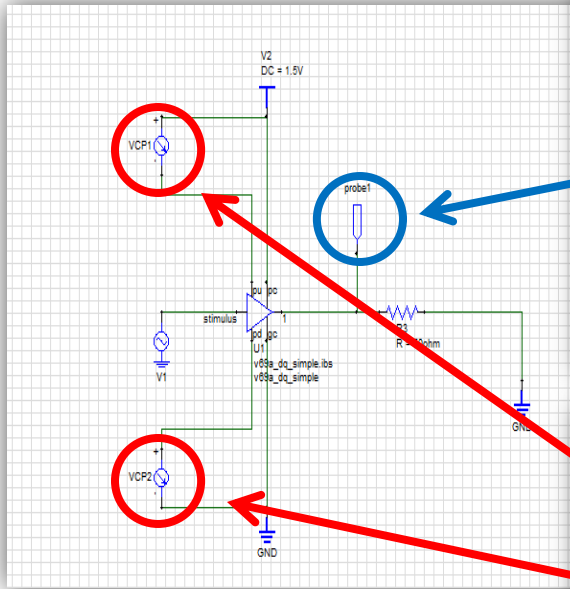
Test Case – IBIS Model

Extracted IBIS 5.0 Model – no on-die de-cap model



Test Case – IBIS vs. SPICE

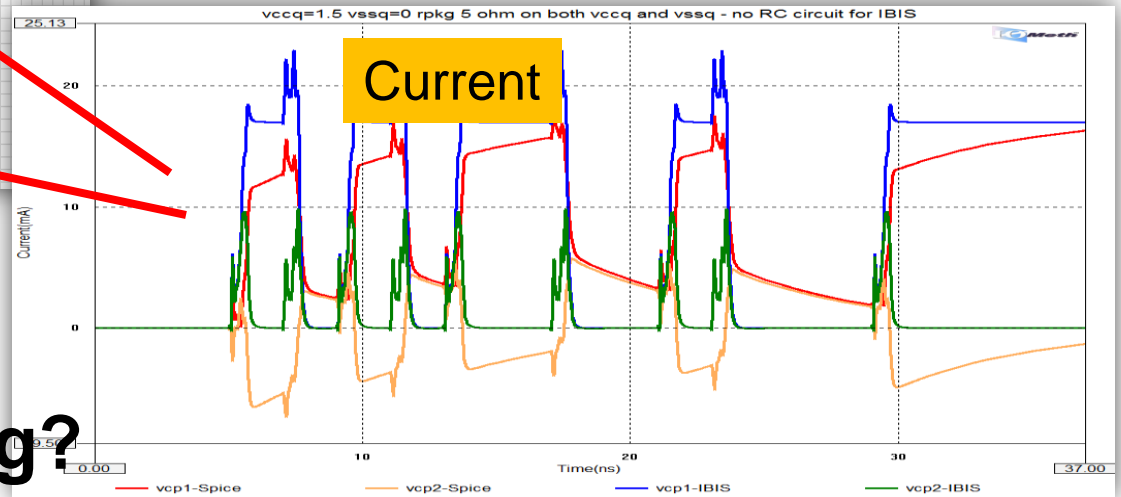
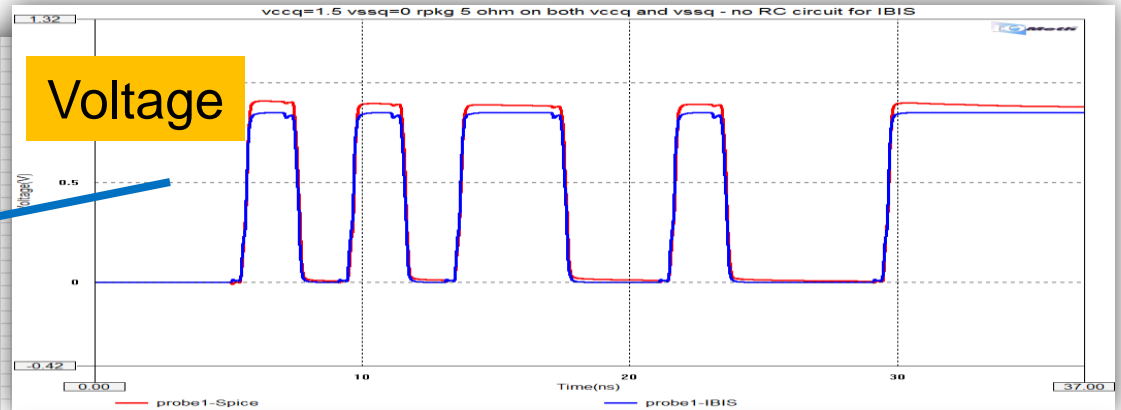
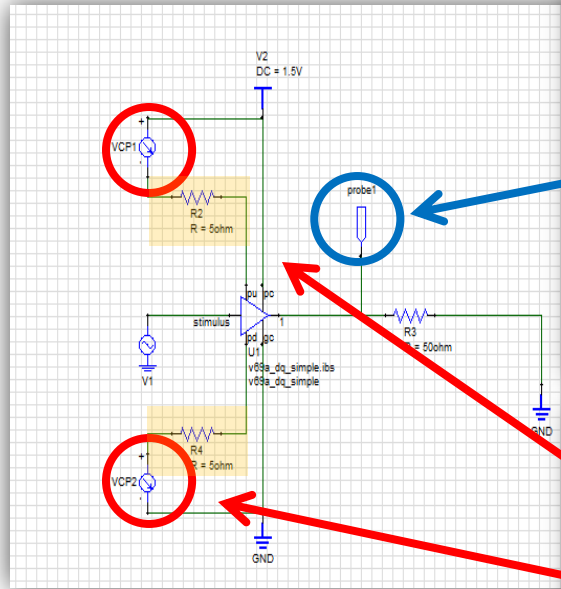
Validation with perfect power supply



Good Match!

Test Case – IBIS vs. SPICE

Validation with large R_pkg on power/gnd pins



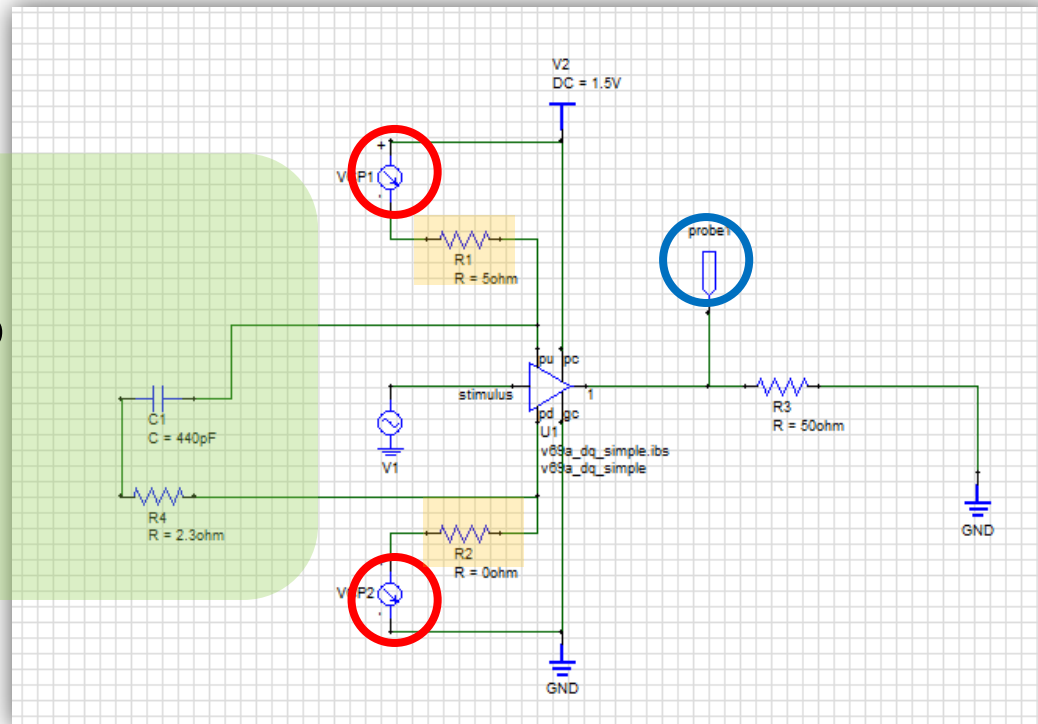
Oops!

Missing something?

Workaround

Validation with R_pkg on power/gnd pins

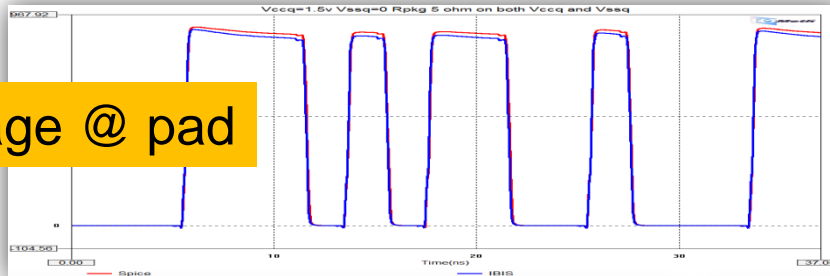
RC De-coupling circuit added into IBIS simulations



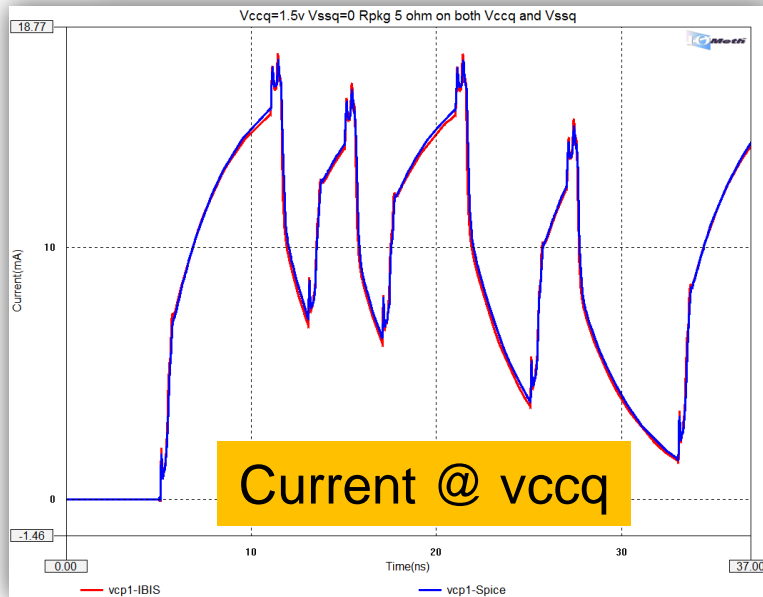
Workaround

Validating with R_pkg on power/gnd pins
– added RC de-coupling circuit

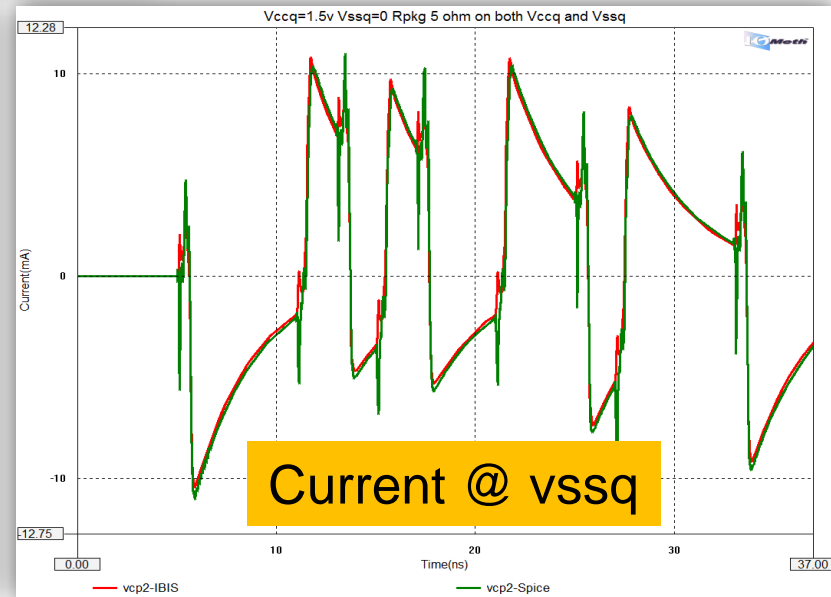
Voltage @ pad



Now they match!



Current @ vccq



Current @ vssq

Modeling On-Die De-Cap

- IBIS 5.0 model extracted using the static power supply
 - IBIS model data doesn't contain any info about de-coupling circuit between Vccq and Vssq
 - There is no place for us to add this info into the [Model] section
- Solution within existing IBIS Specification
 - Use IBIS "Series" Model type (e.g. [C Series], [Rc Series]) to model de-coupling circuit
 - Use [Series Pin Mapping] to connect with Power and GND pins

There is a problem!

What is the issue?

- The Series Model de-coupling circuit attaches at the [Component] Pin level, not inside the [Model]
 - On-Die de-coupling circuit belongs to each buffer
 - In most cases, multiple buffers share one power/gnd rail
 - The only way to model per-buffer de-cap is with a per-power bus model. This might not be the desired de-cap model.

Conclusion

- IBIS 5.0 [Model] does not contain any info about decoupling between Power and GND nodes
- On-die de-coupling circuit can be added outside of IBIS [Model] to achieve accuracy requirement
- Be careful using IBIS [Series Pin Mapping] feature for On-die De-coupling Circuit modeling
- BIRD145 might provide a solution
 - Would allow complex on-die de-cap model attached to each [Model] and modeling of other important PDN parasitics

Thank You

