

# Analysis of the Impact of Crosstalk in High-speed Serial Links

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# Agenda

- Introduction
- Crosstalk Contributors in High-Speed Serial Links
- Analysis of the Impact of Crosstalk in BGA area
- Summary

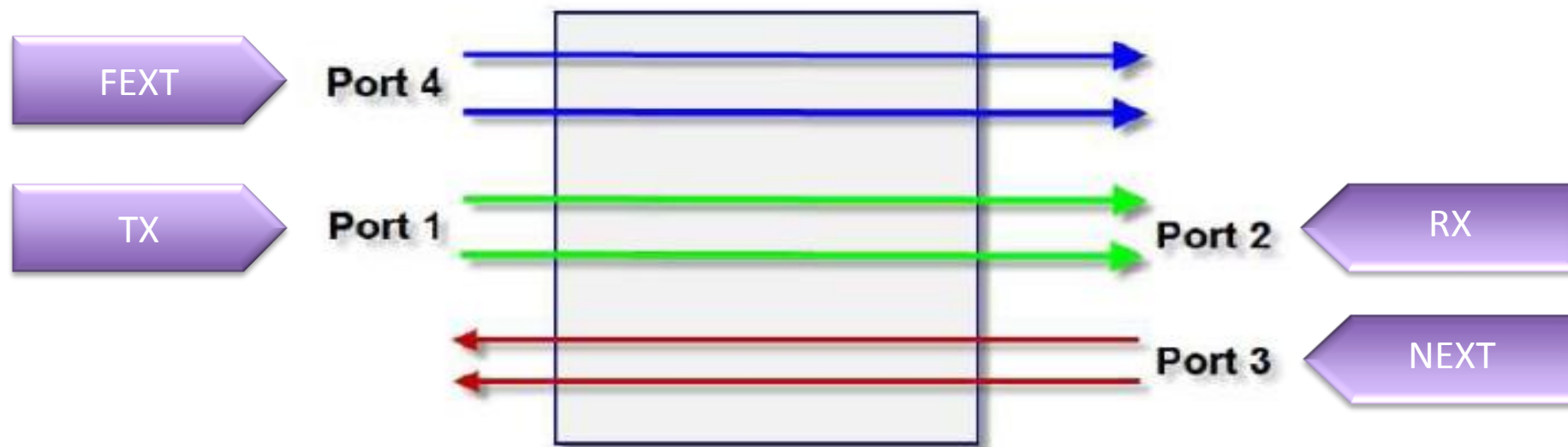
# Why Crosstalk?

- 10Gbps and even more higher speed channels need to be designed. So, crosstalk is inevitable.
  - Signal rise time (  $T_r$  ) in 10Gbps+ system is very small ,Which produces more high frequency components.
  - 10Gbps+ Interconnect System is very Sensitive with Impedance Mismatch , e.g., BGA fanout areas, Connectors, Pindrills and other Vias. Crosstalk from reflected aggressor signals and reflected crosstalk will further degrade the victim signal.
- The Crosstalk in High-speed Serial links must be carefully analyzed to meet the BER performance requirement.

# Definition of Crosstalk in SerDes System

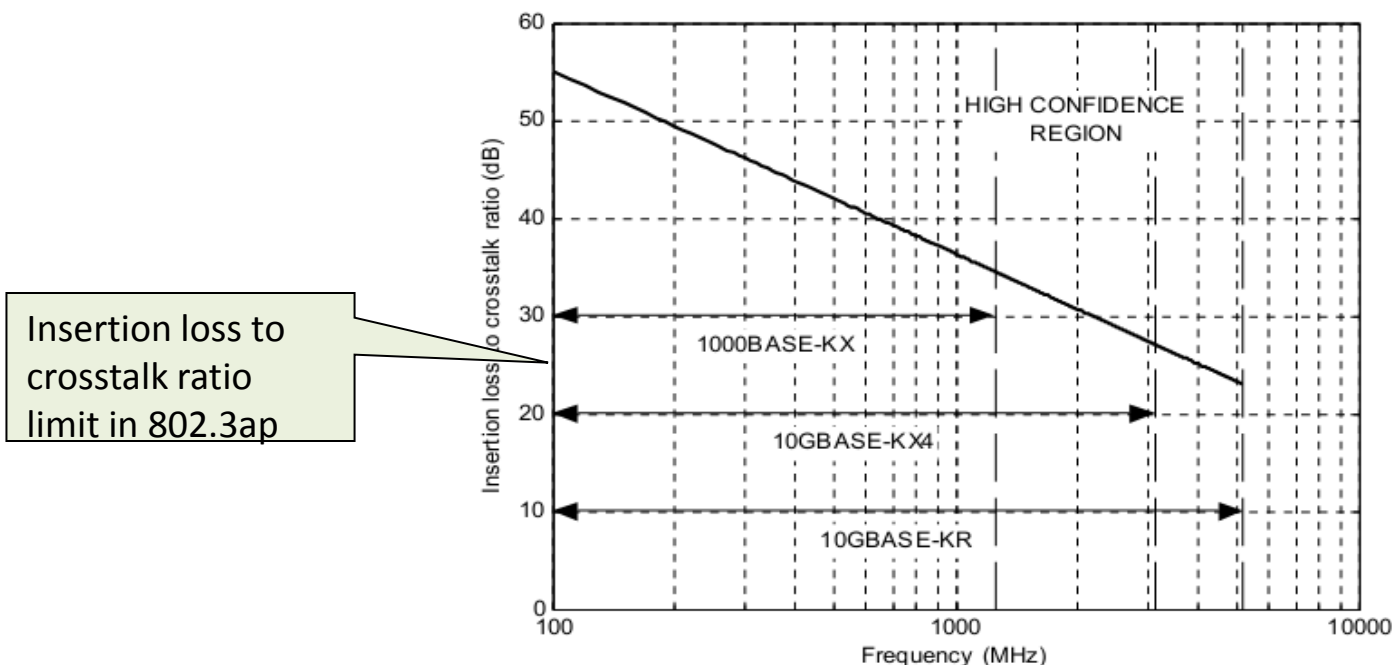
Crosstalk is usually subdivided to two parts. It is described in IEEE802.3ap as followed :

- Far-end crosstalk(FEXT) coming from data traveling in the same general direction as the channel of interest.
- Near-end crosstalk(NEXT) originating from a channel with a transmitter near the receiver of the channel of interest.



# Crosstalk Requirement in IEEE 802.3ap

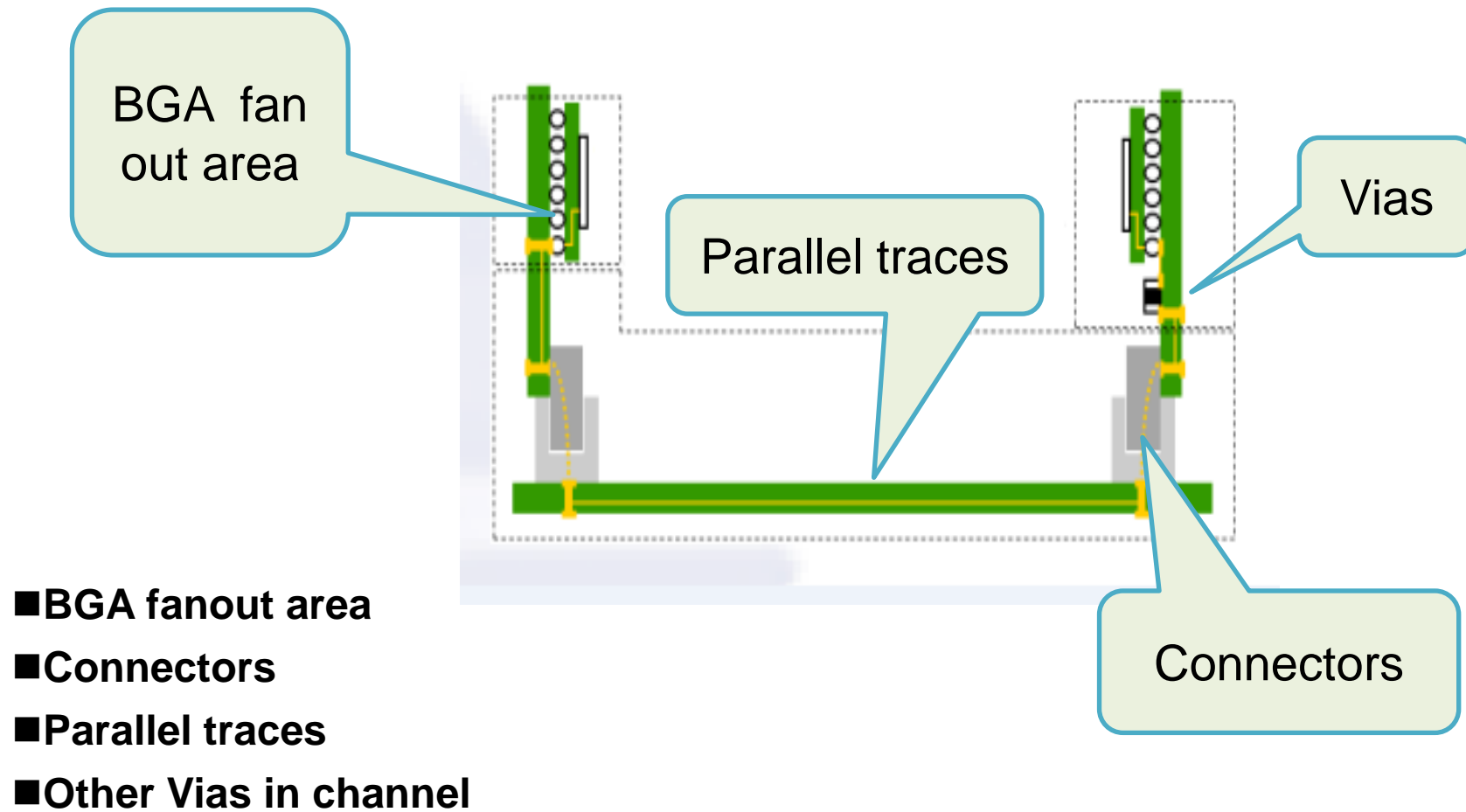
- Most of standards specify the requirement of crosstalk.
- In IEEE 802.3ap, it is specified as Insertion loss to crosstalk ratio ( ICR ) .



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# Crosstalk Contributors in High-Speed System



# Crosstalk Contributors in High-Speed System

## ■ BGA fanout area

Pay attention to BGA fanout area .The fanout patterns of differential pairs affect the crosstalk .

## ■ Connectors

Connectors are often the key contributor to crosstalk. Estimate TX/RX partition and pindrill to optimize the crosstalk performance.

## ■ Parallel traces

Find the longest parallel trace and carefully analyze the crosstalk to ensure the routing rules are suitable.

## ■ Other Vias in channel

The Vias for capacitors will cause crosstalk ,so keep appropriate distance between Vias of differential pairs.

# Why do we focus on Crosstalk in BGA Area

- We often focus on the crosstalk caused by connectors, connectors' pindrills and parallel traces.
- We paid few attention to crosstalk in BGA area in the past.
- BGA area is also an important part needed to be carefully analyzed.
- In the rest of this paper, we will look into the impact of BGA area.

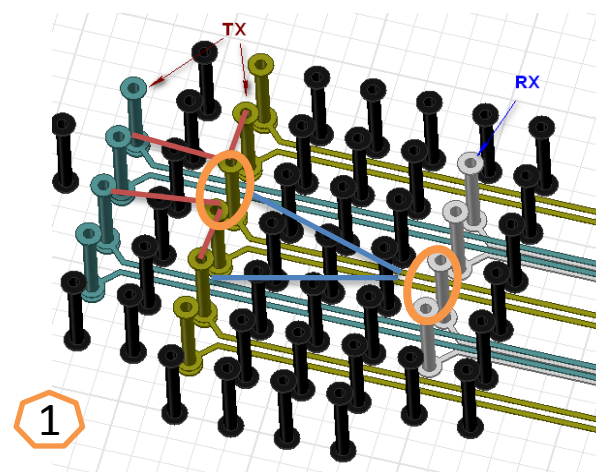
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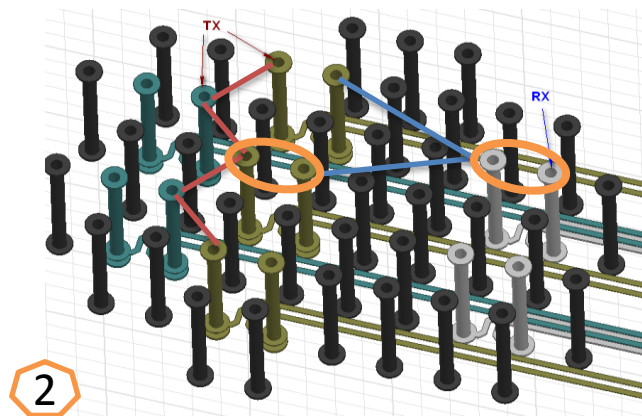
# Modeling for Crosstalk Analysis

In BGA fanout area, There are Three samples and their primary differences:

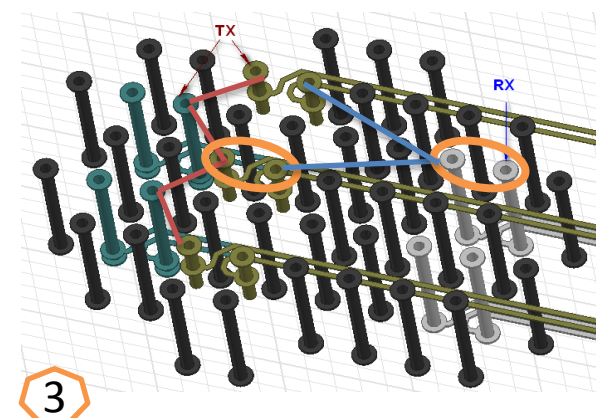
- Fanout pattern
- Distance between pairs
- Via length



Long Via, Fanout Pattern 1



Long Via, Fanout Pattern 2

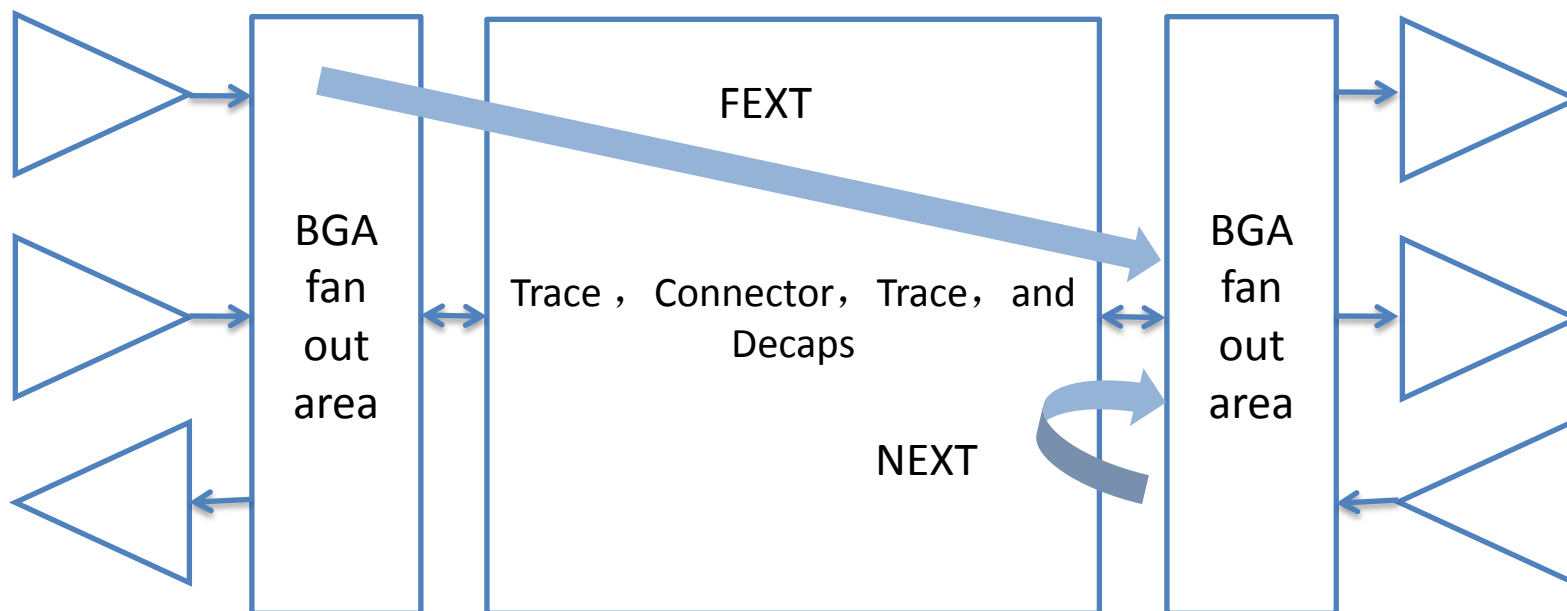


Short Via, Fanout Pattern 3

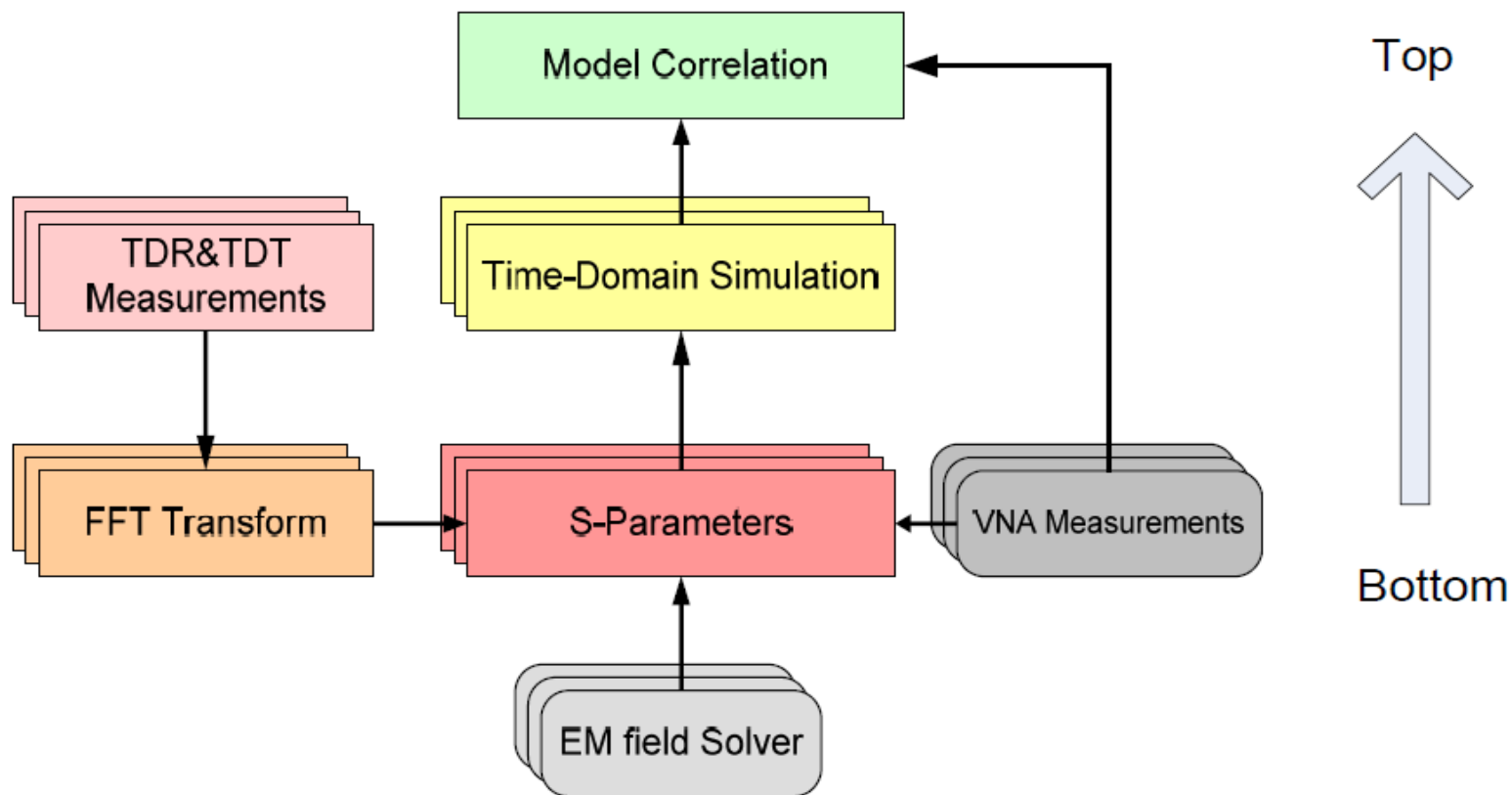
# Modeling for Crosstalk Analysis

There are three serial links in model:

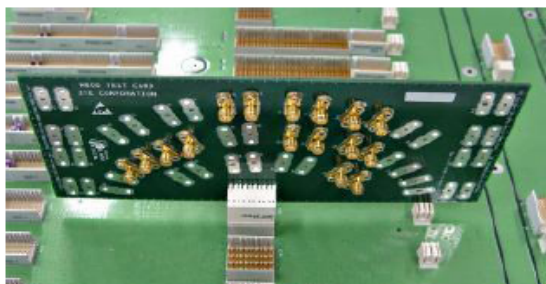
- Victim's channel ,aggressor channel for NEXT and aggressor channel for FEXT.
- S4p files for NEXT and FEXT.
- 40-inch length trace, 3W space, a certain connector model.



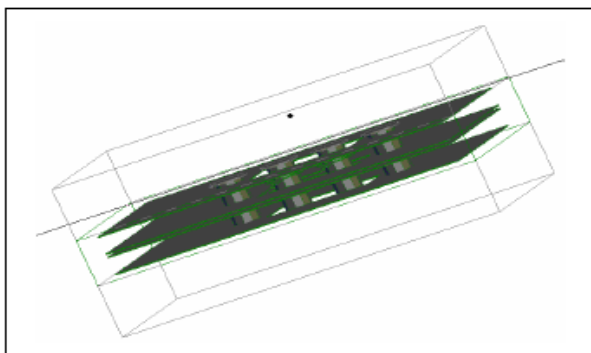
# Using S-Parameters for Crosstalk Analysis



# Using S-Parameters for Crosstalk Analysis



Measurement setup



3D EM Solver Modeling

## S-Parameter touchstone file

! FILE NAME

! DATE 10/20/05 22:27

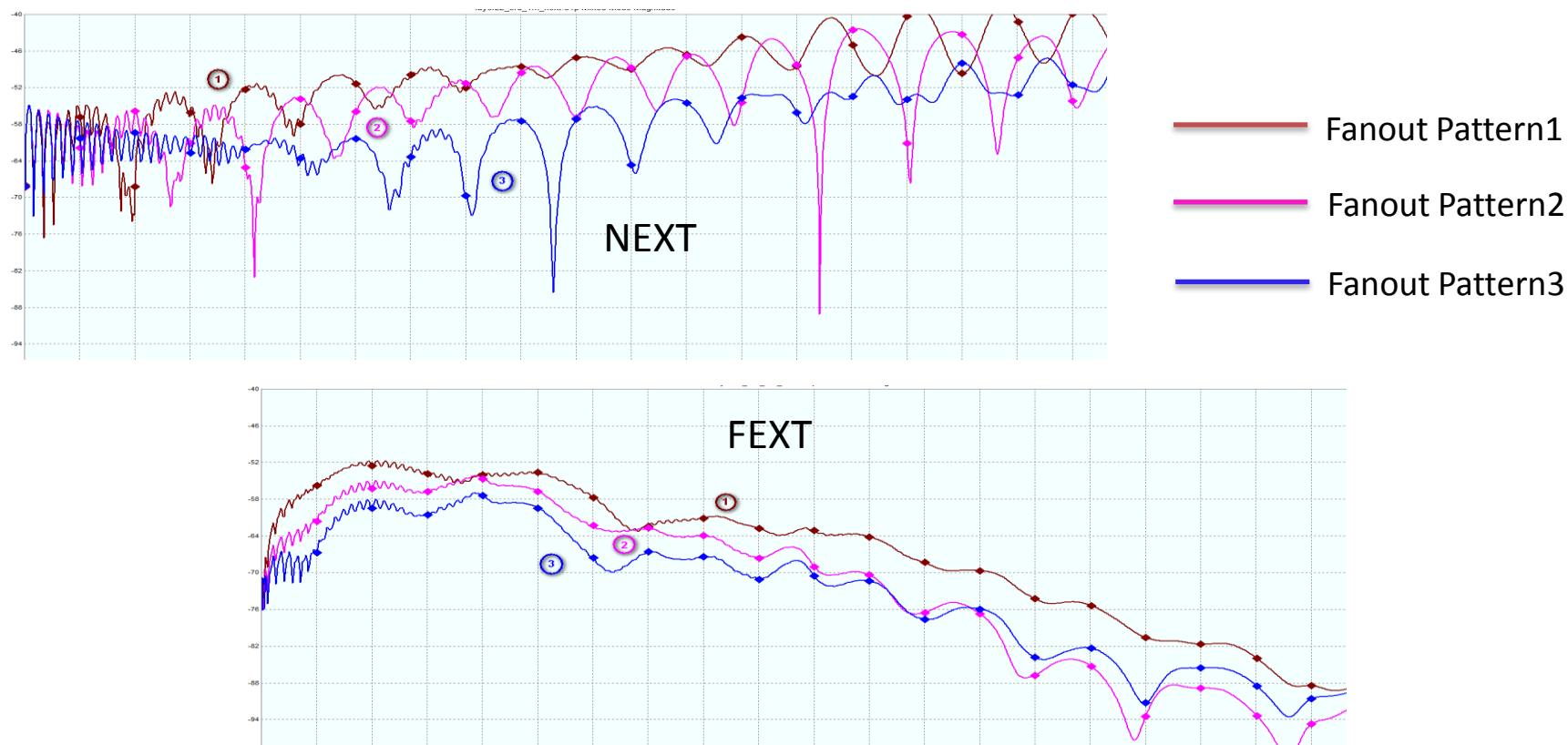
! CORRECTED DATA

# GHz S MA R 50.00

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0.010000000 3.217487E-02 25.539 1.433922E-02 73.163 7.022051E-04 -164.797 9.721752E-01 -14.501
1.437112E-02 73.522 8.342298E-02 21.247 9.721735E-01 -14.643 1.031352E-03 152.923
6.869677E-04 -166.566 9.750083E-01 -14.799 3.180707E-02 24.806 1.426077E-02 73.110
9.757603E-01 -14.762 1.043164E-03 148.597 1.442420E-02 73.191 3.261170E-02 27.190
0.019987500 4.338055E-02 24.741 2.759167E-02 60.757 1.264493E-03 172.773 9.619784E-01 -28.320
2.753260E-02 60.598 5.663544E-02 -7.471 9.629115E-01 -28.078 8.262120E-04 130.485
1.252529E-03 171.672 9.652648E-01 -28.414 4.342042E-02 20.989 2.762920E-02 60.190
9.660442E-01 -28.600 8.369133E-04 130.697 2.751868E-02 59.706 4.591656E-02 22.958
0.029975000 5.279364E-02 19.352 3.940318E-02 47.550 1.777378E-03 145.369 9.554404E-01 -42.013
3.933148E-02 47.604 3.671105E-02 -9.347 9.577851E-01 -41.765 7.441007E-04 136.632
1.751164E-03 143.245 9.584093E-01 -42.077 5.350023E-02 13.120 3.941780E-02 46.306
9.575923E-01 -42.330 7.423362E-04 133.941 3.934892E-02 46.433 5.596628E-02 14.271
0.039962500 6.059968E-02 11.269 4.905304E-02 34.608 2.323297E-03 117.191 9.492754E-01 -55.661
4.906615E-02 34.594 3.431321E-02 15.544 9.519293E-01 -55.371 1.174888E-03 136.972
2.295646E-03 114.989 9.529339E-01 -55.758 6.189575E-02 3.980 4.901626E-02 33.024
9.517830E-01 -55.968 1.161010E-03 136.920 4.896336E-02 33.055 6.299231E-02 3.407
0.049950000 6.662585E-02 1.555 5.628981E-02 21.659 2.841726E-03 90.468 9.434645E-01 -69.209
5.633547E-02 21.883 5.111281E-02 22.288 9.453543E-01 -68.928 1.940923E-03 116.840
2.788556E-03 88.049 9.454238E-01 -69.373 6.795117E-02 -5.423 5.627455E-02 19.599
9.449649E-01 -69.579 1.899390E-03 117.875 5.611407E-02 19.671 6.618402E-02 -7.747
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6.093212E-02 8.964 6.989614E-02 11.224 9.395743E-01 -82.342 2.770354E-03 88.655
3.227467E-03 61.858 9.384965E-01 -82.888 7.212381E-02 -15.124 6.077348E-02 6.385
9.384112E-01 -83.188 2.774367E-03 89.391 6.085816E-02 6.319 6.634015E-02 -18.404
0.069925000 7.160252E-02 -22.097 6.273439E-02 -3.632 3.720456E-03 37.930 9.326985E-01 -96.370
6.272058E-02 -3.522 8.357295E-02 -6.331 9.355087E-01 -95.783 3.570472E-03 57.951
3.599259E-03 36.141 9.323274E-01 -96.278 7.376438E-02 -24.634 6.278425E-02 -6.705
9.336231E-01 -96.646 3.602008E-03 58.589 6.281382E-02 -6.657 6.448640E-02 -28.081
0.079912500 7.081175E-02 -34.685 6.182219E-02 -16.100 4.040125E-03 12.437 9.270003E-01 -109.843
6.178188E-02 -15.966 8.959131E-02 -26.534 9.309905E-01 -109.271 4.262746E-03 27.041
3.903036E-03 11.300 9.269238E-01 -109.574 7.376363E-02 -34.289 6.182057E-02 -19.660
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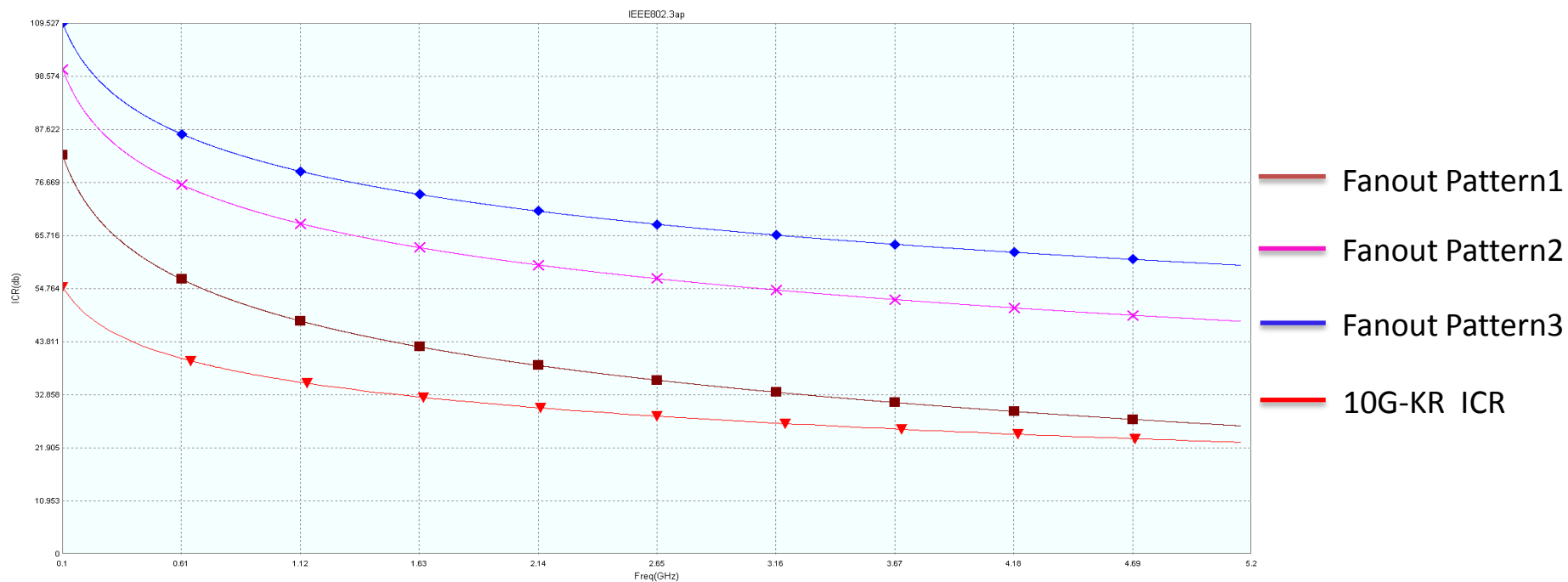
# Modeling for Three Fanout Patterns

- Exchange the BGA fanout area model with former three samples, and we get three different results for system NEXT and FEXT.



# ICR Simulation for Three Fanout Patterns

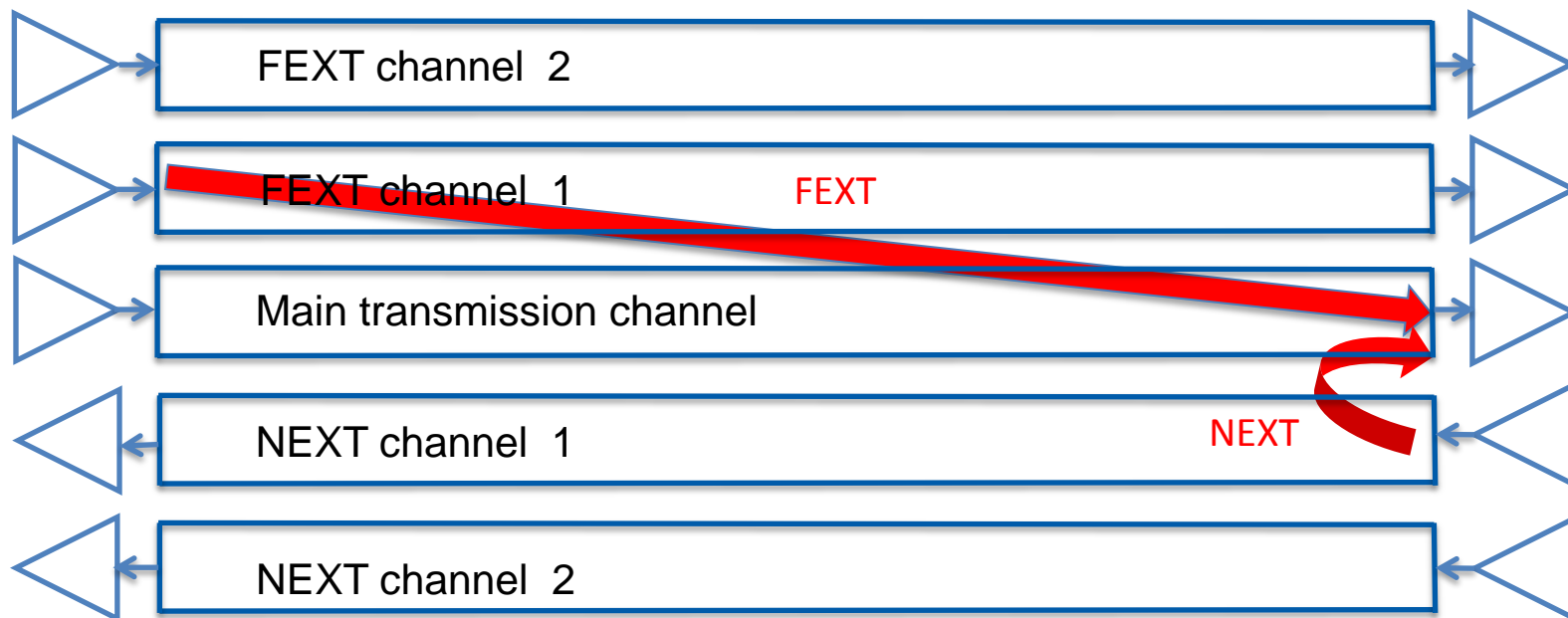
- Three ICR Simulation Results compare with ICR Requirement in IEEE 802.3ap.



# SNR & BER Simulation for Three Fanout Patterns

## ■ Crosstalk Simulation Setup

- Time domain simulation with SerDes buffer models.
- 10.3125Gbps, 64B66B.
- Crosstalk phase assumed to be worst-case aligned signal.



# Comparisons of Simulation Results

Sample Channel	Eye Height	Eye Width	SNR	BER
Fanout Pattern1 without crosstalk	16.37%	0.35UI	21.9	7.2E-36
Fanout Pattern2 without crosstalk	16.35%	0.35UI	21.9	5.4E-36
Fanout Pattern3 without crosstalk	16.42%	0.35UI	21.9	6.3E-36
Fanout Pattern1 with 1 time crosstalk	15.65%	0.35UI	21.6	1.2E-33
Fanout Pattern2 with 1 time crosstalk	15.95%	0.35UI	21.8	9.8E-35
Fanout Pattern3 with 1 time crosstalk	16.22%	0.35UI	21.8	3.0E-35
Fanout Pattern1 with 2 times crosstalk	14.92%	0.35UI	21.3	2.0E-31
Fanout Pattern2 with 2 times crosstalk	15.64%	0.35UI	21.6	1.8E-33
Fanout Pattern3 with 2 times crosstalk	16.05%	0.35UI	21.8	1.0E-34

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# Summary

- The crosstalk in BGA fanout area is not negligible but very important in 10Gbps+ SerDes links ,we need to select an optimized pattern for BGA fanout to improve the system performance.
- Connectors & pindrills, parallel traces and Vias are also very important parts to be analyzed.
- With carefully look into these crosstalk, we will do better work in serial links design.

 *Bringing you Closer*

**Thanks!**