An Effective Solution to Simulate Composite Current When Over-clocking

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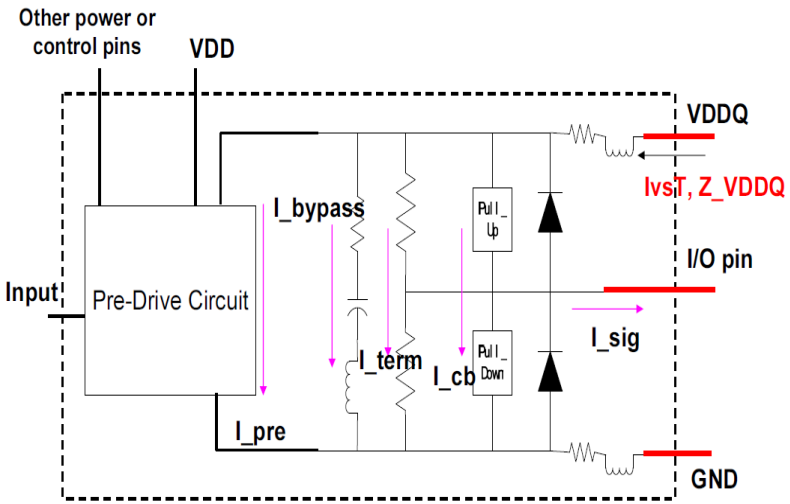
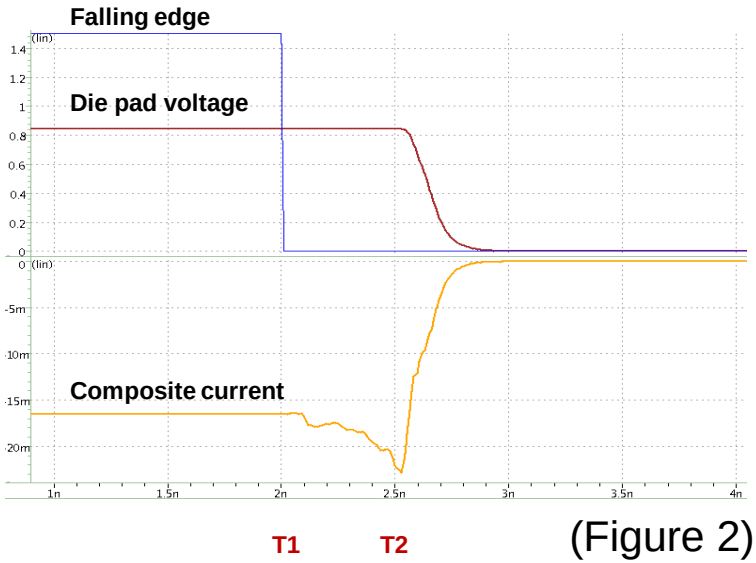
Outline

- Composite current simulation introduction
- Over-clocking introduction
- Accuracy issue with over-clocking
- Test superposition idea with R_fixture & V_fixture
- The solution of composite current simulation when over-clocking
- Accuracy test of over-clocking by the new method
- Summary

Composite Current Simulation Introduction



(Figure 1)



(Figure 2)

- Power integrity problem.
- Composite current means power terminal current of I(VDDQ) in figure 1.
- IT waveform looks like in figure 2.
- IBIS models(before 5.0) can get accurate simulation of voltage waveform at die pad, even for over-clocking situation. But it can't get an accurate result of I(VDDQ)
- IBIS5.0 model provides [composite current] data to simulate I(VDDQ) accurately.
- This presentation will describe one detailed effective method to simulate I(VDDQ) with [Composite Current] data, for over-clocking situation.

Over-clocking Introduction

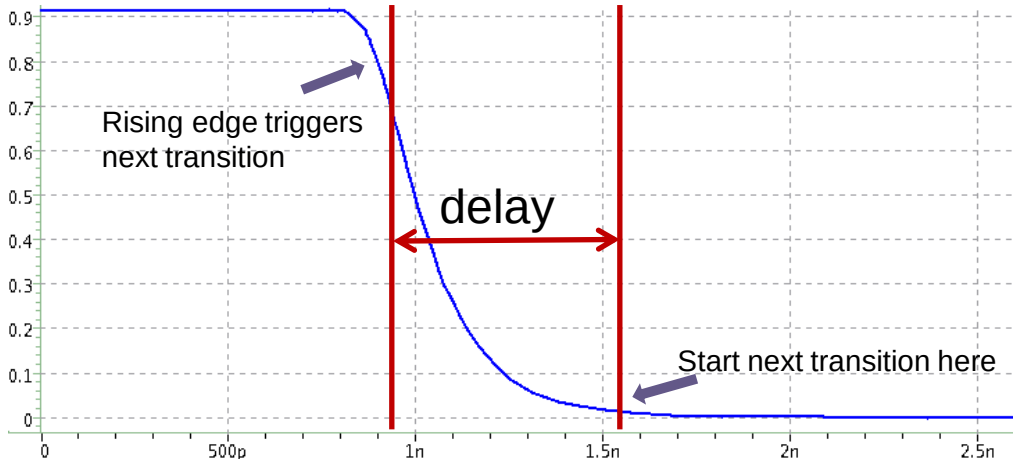
- Over-clocking:

  Next transition is triggered before current transition finishes.

- Transistor level buffer VT behavior for over-clocking:

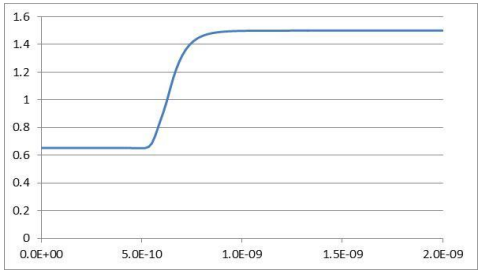
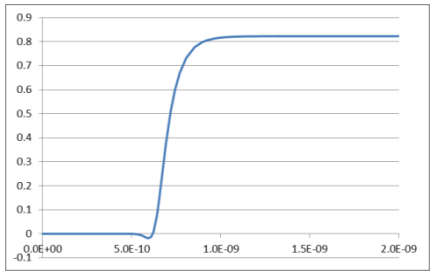
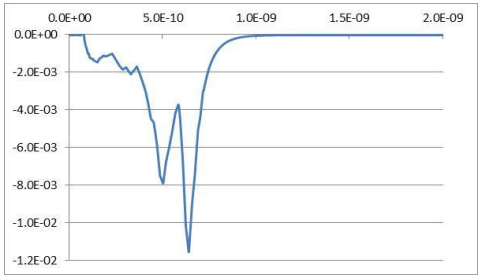
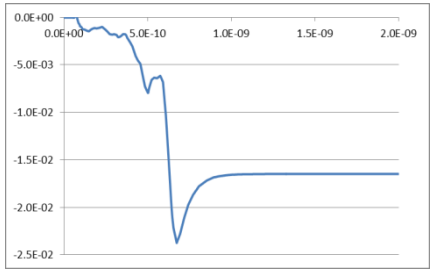
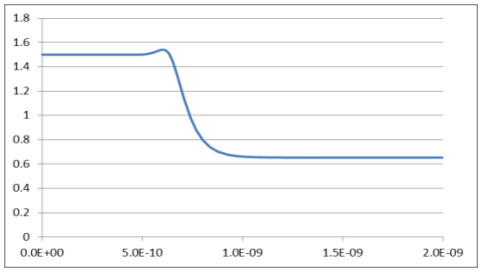
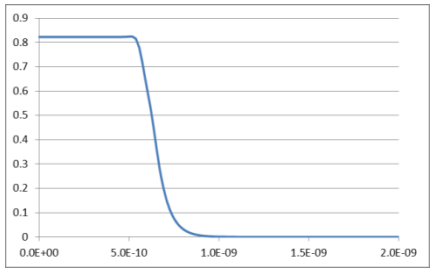
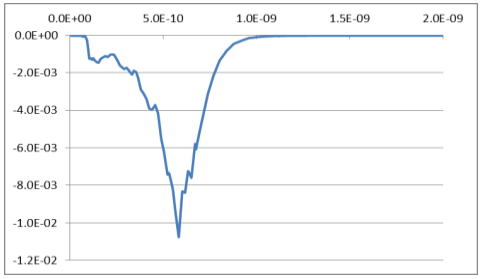
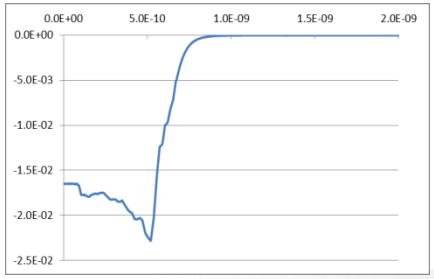
  This transition will continue with a delay time, and then start new transition.

  (Refer :http://www.vhdl.org/pub/ibis/summits/jun03b/muranyi2.pdf)



- With this observation, IBIS buffer works good for output voltage waveform.

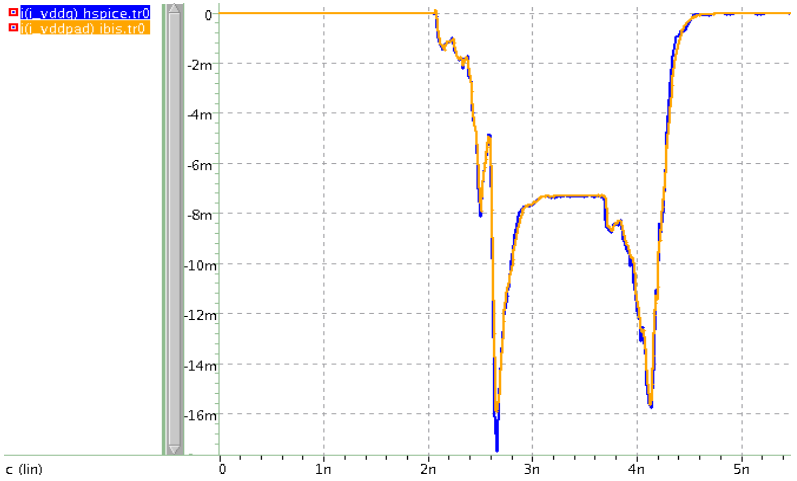
An Example of IBIS 5.0 model

	V_fixure=1.5v & R_fixture=50ohm	V_fixure=0v & R_fixture=50ohm
Rising VT		
Rising IT		
Falling VT		
Falling IT		

IBIS5.0 Accuracy without Over-Clocking

- Load the IBIS model with PKG, T line and voltage source
- IBIS5.0 model shows good accuracy by comparison with HSPICE transistor level model!

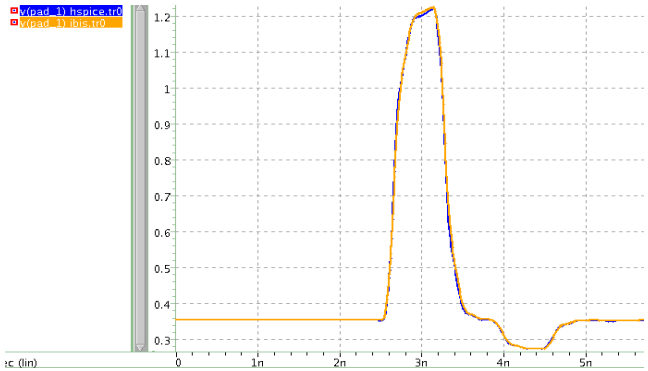
V(pad) waveform comparison



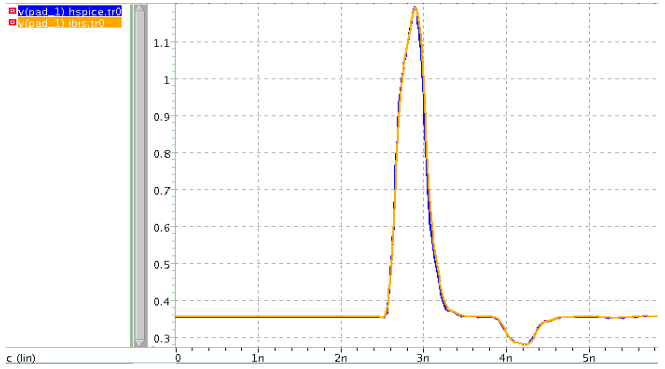
I(vddq) waveform comparison

IBIS5.0 Accuracy with Over-Clocking

- With the same loading, IBIS5.0 model still shows good accuracy for output voltage.
- But the accuracy of I(VDDQ) may be bad, especially when serious over-clocking happens !

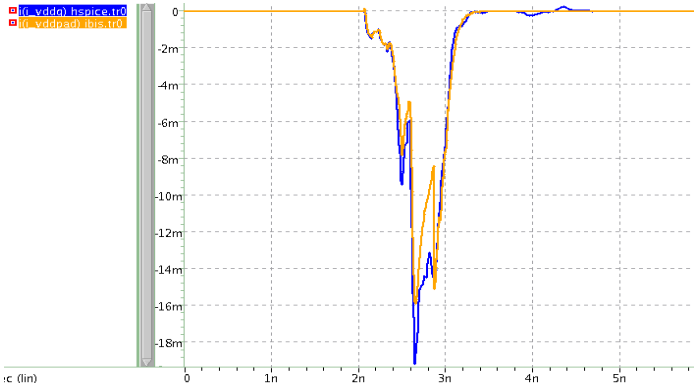


V(pad) comparison when over-clocking happens.



V(pad) comparison when **serious** over-clocking happens.

I(vddq) comparison when over-clocking happens.



I(vddq) comparison when **serious** over-clocking happens.

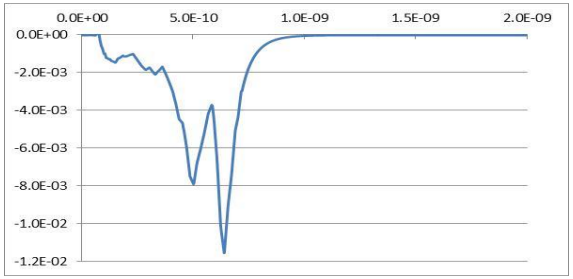
Test Superposition Idea with R_fixture & V_fixture

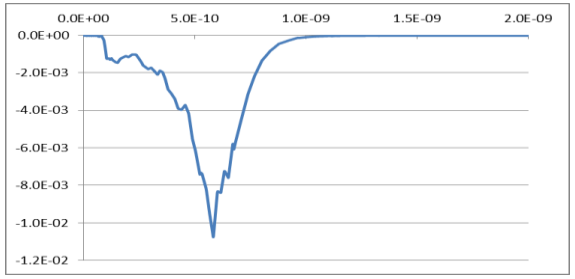
- To simplify the test, make both IBIS buffer and HSPICE transistor level buffer loaded with R_fixture and V_fixture from VT waveforms.
- For composite current simulation when over-clocking happens, the currents of last transition and this transition works together.
- A natural idea is to make a superposition of [Composite Current] at the overlap time span.

Test Result 1

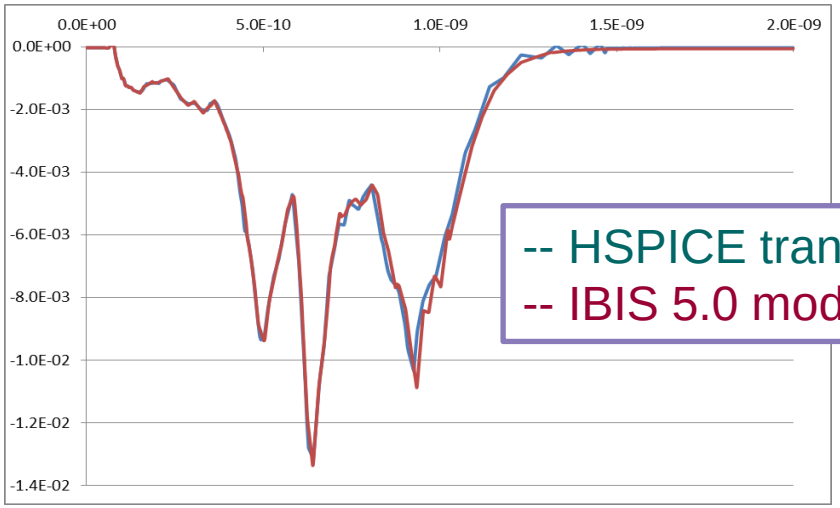
- Load the IBIS buffer with V_fixture=1.5v R_fixture=50ohm
- Input: rising edge and then falling edge.

Rising and falling [Composite Current] in IBIS model:





- Comparison of superposition result and golden: It's good match!

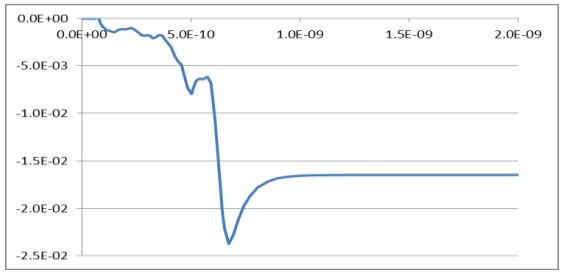


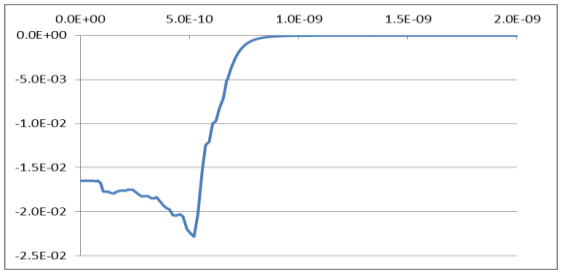
-- HSPICE transistor model (golden)
-- IBIS 5.0 model w/ superposition

Test Result 2

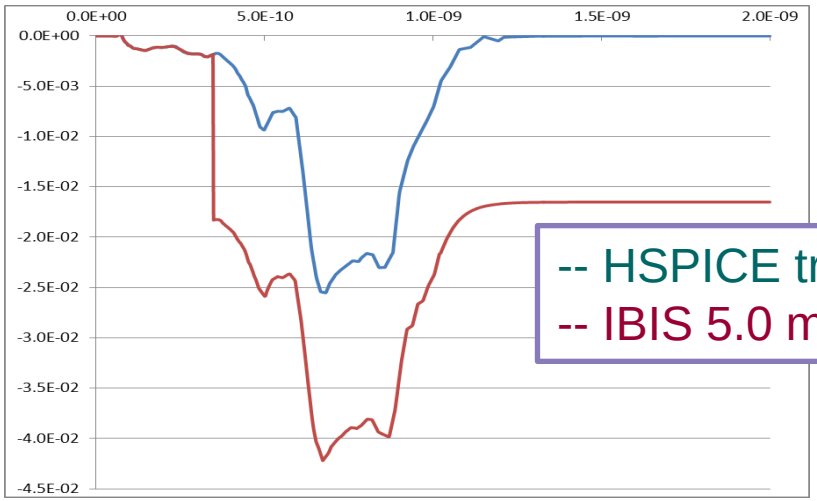
- Load the IBIS buffer with V_fixture=0v R_fixture=50ohm
- Input: rising edge and then falling edge

Rising and falling [Composite Current] in IBIS model:





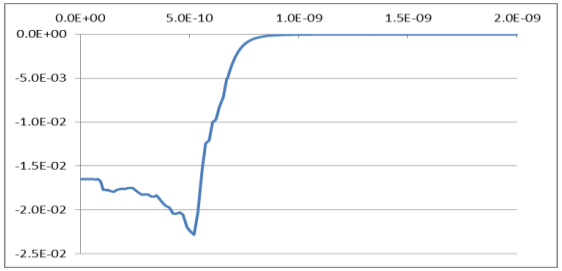
- Comparison of superposition result and golden: It's bad match!



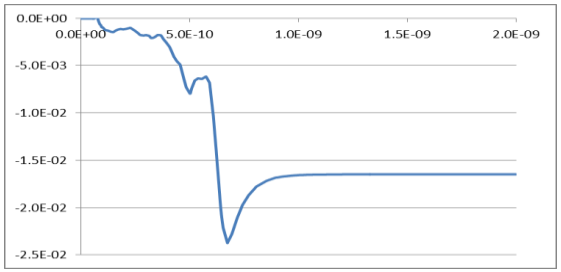
-- HSPICE transistor model (golden)
-- IBIS 5.0 model w/ superposition

Refine Superposition

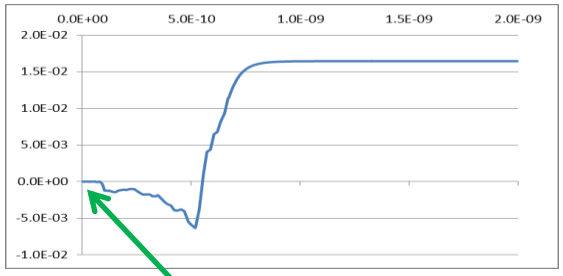
- When doing superposition of the rising and falling [Composite Current] in overlap time span, do not add the currents directly.
- Instead, modify the falling [Composite Current] happening later by
  I(T) = I(T) – I(0)
- And then do superposition with the new IT.



I(T) = I(T) – I(0)



+

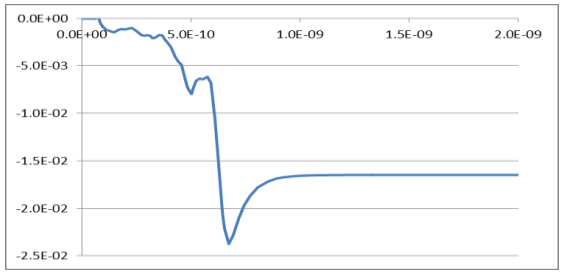


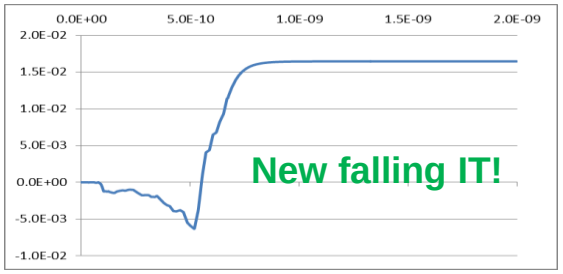
Now, the new IT starts from origin

Test Result 3(refined superposition)

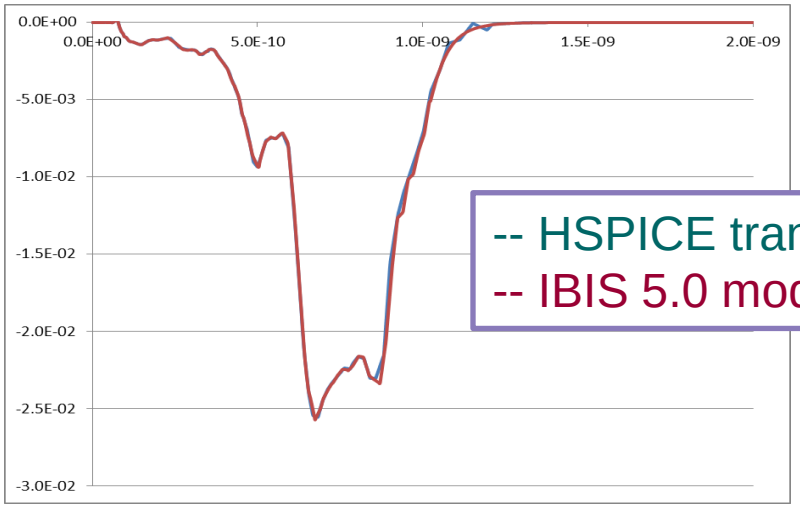
- Load the IBIS buffer with V_fixture=0v R_fixture=50ohm
- Input: rising edge and then falling edge

Rising and falling [Composite Current] in IBIS model:



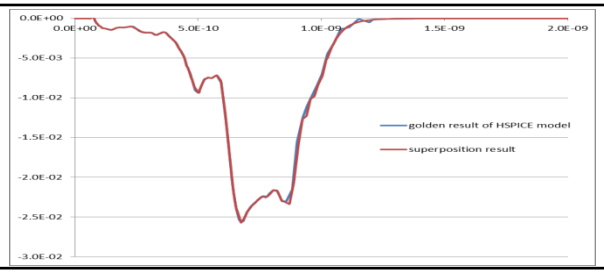
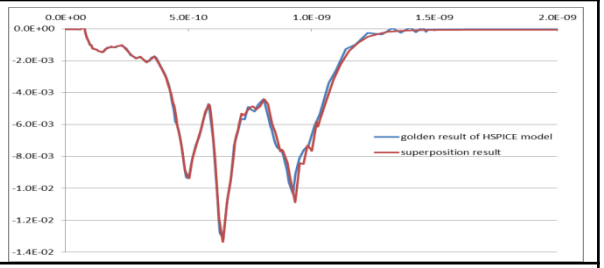
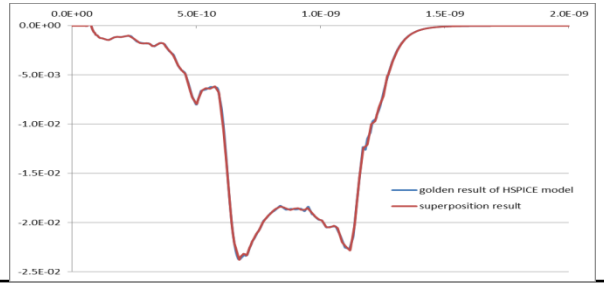
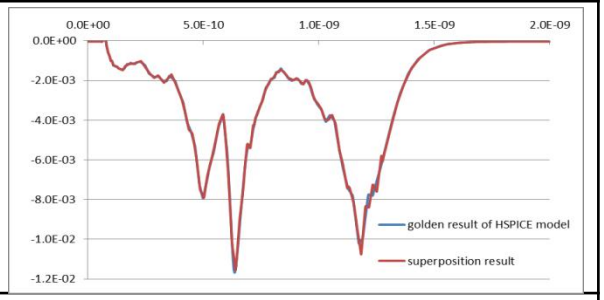
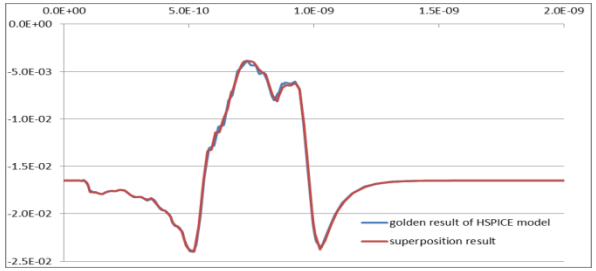
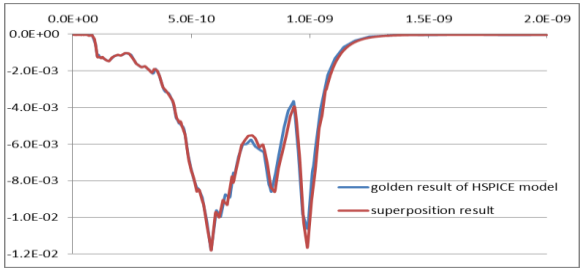
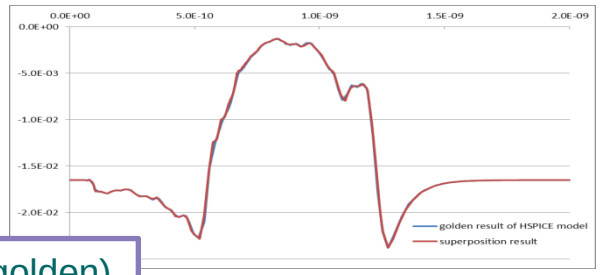
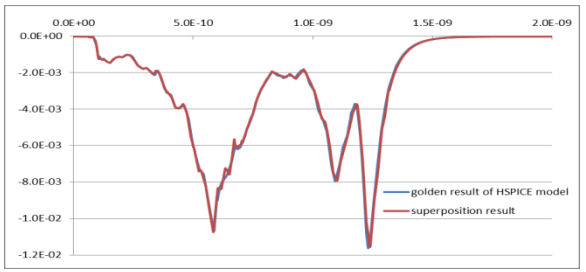


- Comparison of superposition result and golden: Now It's good match!



-- HSPICE transistor model (golden)
-- IBIS 5.0 model w/ superposition

All Test Results (refined superposition)

	Vfix=0v & Rfix=50ohm	Vfix=1.5v & Rfix=50ohm
Rising and falling Over-clocking at 0.35ns		
Rising and falling Over-clocking at 0.6ns		
Falling and rising Over-clocking at 0.35ns		
Falling and rising Over-clocking at 0.6ns		

-- HSPICE transistor model (golden)
-- IBIS 5.0 model w/ superposition

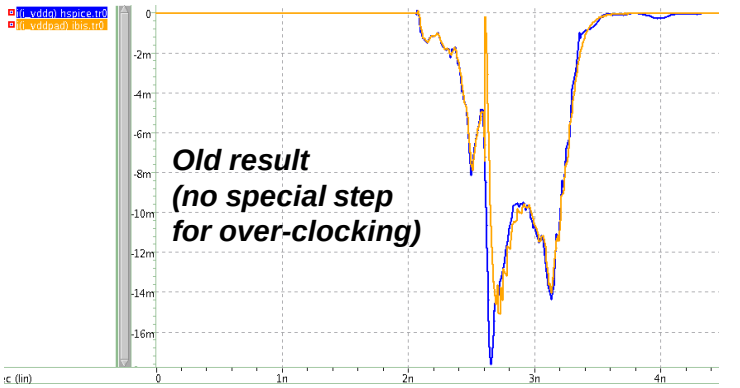
The Solution of Composite Current Simulation when Over-Clocking

- When over-clocking happens, construct superposition waveform of rising IT and falling IT (or falling IT and rising IT) for different R_fixture and V_fixture. For happening later falling IT (or rising IT), we should do I(T) = I(T) – I(0) before superposition step.

- Use the constructed IT waveforms to simulate current of I(VDDQ).

Accuracy Test of Over-Clocking by the Method

- Load the test case with PKG, T line and voltage source.
- Now, with the new method, IBIS5.0 model show good accuracy of I(VDDQ) even when serious over-clocking happens!

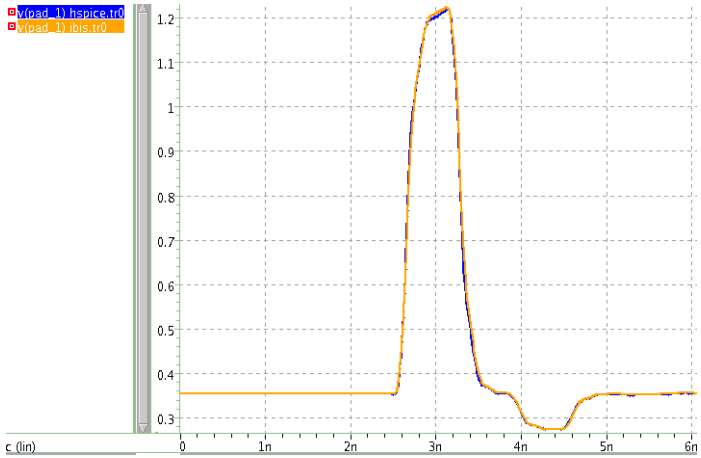


I(vddq) comparison with golden when over-clocking happens

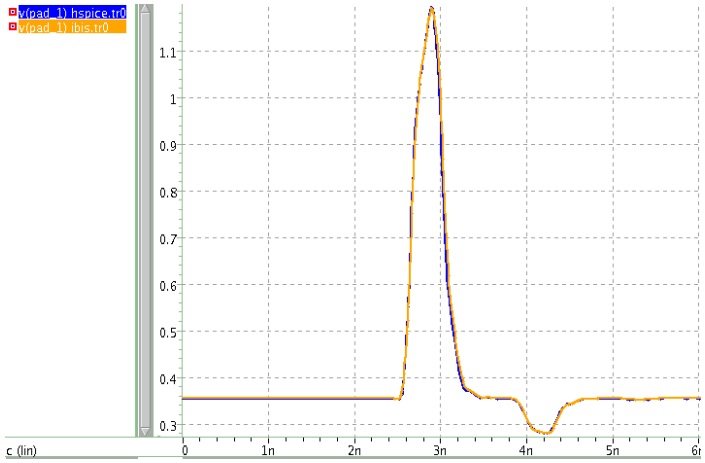
I(vddq) comparison with golden when serious over-clocking happens.

Accuracy Test of Over-Clocking by the Method (Cont.)

Check the output voltage waveform at die pad with the method:
Accuracy is still good!



V(pad) comparison when over-clocking happens.



V(pad) comparison when **serious** over-clocking happens.

Summary

- Discussed about accuracy problem due to over-clocking in IBIS 5.0 models.
- Proposed a novel superposition method for [Composite Current] of IBIS 5.0 to solve the problem.
- The new method is tested and validated under over-clocking with multiple load conditions.
  - ✓ obtained accurate results of I(VDDQ) when loaded with R_fixture & V_fixture.
  - ✓ obtained accurate results when buffer is loaded with practical loadings.
  - ✓ obtained very good result of the voltage output at die pad as before.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