#### IBIS Simulation Case Study: Unexpected Glitch and Using C\_fixture

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#### Outline

- Motivation
  - Unexpected glitch issue in the IBIS simulation
  - Seeking for solutions
- Case study and solutions
  - The root cause of glitch issue
  - Possible solutions
- Using C\_fixture in IBIS V-T curves
- Conclusions

#### Motivation

- An unexpected glitch found when doing an IBIS model validation (transient analysis simulations)
  - An unexpected glitch found when we used < 450ps time step setting (called resolution setting in some EDA tools)
  - Everything is correct when we used bigger time step in the simulations
- Want to find out the root cause of this issue and solutions

- IBIS buffer model
  - This is normal I<sup>2</sup>C pad buffer (Open Drain type)
  - It is relatively low speed buffer
    - About 60ns for rising and 300ns for falling to be settled with 4.7K ohm load and 3.3v to pull up



Simulation results with the same condition as V-T fixture settings



- A simulator bug?
  - We tried to use 5 different simulators and found all the results have the glitch issues. Only differences are the glitch levels



This is from another simulator



#### IBIS Model issue?

- IBIS curves are normal
- 0 error, 0 warning from IBISCHK
- Only Rising curve has a small "dip"

- We manually removed the "dip".
   The simulation results are normal for all simulators
- So, this is the root cause. But WHY?



#### The root cause

Simulator works fine when the time step is bigger than the "dip down" period. It produces only 1 or 0 step in the "dip down" region. It would be "skipped" when it leads to a wrong direction

Simulator got confused when the time step is less than the "dip down" period when it produces 2 or more steps in the "dip down" region. It leads to a wrong direction without any information from I-V curves The "dip" width is about 1.25ns. The dip down period is about 460ps.



#### Solutions

- Using large time step size in transient analysis
  - It could lead to an inaccurate result
  - The setting needs to be manually forced. A dynamic step setting feature might not work.
- Manually remove the "dip" area in IBIS Model
- Adding C\_fixture to reduce or make the "dip" area "lighter" or to disappear
  - This method leads to another discussion topic in this presentation

# C\_fixture setting in IBIS V-T section

- C\_fixture optionally can be used in IBIS V-T waveforms
- We normally do not recommend using C\_fixture in V-T curves



- We used the same Spice netlist to create 2 IBIS Models.
  All settings are the same except C\_fixture
  - Blue without C\_fixture (C\_fixture = 0)
  - Orange with C\_fixture (C\_fixture = 15pF)



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#### Use both Models with this topology



 Both cases correlate well with Spice simulations for C\_fixture=0 IBIS Model



 The result from the load with capacitance correlates well with Spice simulations for C\_fixture=15pF IBIS Model



 The slight difference in results from the load without capacitance for C\_fixture=15pF IBIS Model



- C\_fixture can be used in IBIS V-T curves
- Simulators need to use a de-capacitance algorithm when C\_fixture is present in the V-T curves. C\_fixture may reduce simulation accuracy
- It is better that IBIS V-T curves only have resistance load (linear load)

## Supporting C\_fixture in simulations

This is a surprise!

# 3 out of 6 major simulators don't support C\_fixture in IBIS Model. It got ignored!

## Summary

- In some simulations for a slow IBIS model, we found unexpected glitch in the result
  - It is due to a "dip down" area and it could be solved by using larger time step size (resolution value)
  - The "dip down" period could be removed manually or use C\_fixture to reduce "dip down" area (size)
- Be careful when using C\_fixture
  - It might cause some inaccurate simulation results
  - Some simulators do not support C\_fixture in IBIS model
  - Recommend using linear load for V-T curves in IBIS model.



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