WELCOME FROM MIKE LABONTE, IBIS OPEN FORUM

Ladies and Gentlemen,

As chair of the IBIS Open Forum it is my pleasure to welcome you to the 2016 Asian IBIS Summit in Shanghai, and to thank you for your presentations and participation. We are grateful to our sponsors Huawei Technologies, Cadence Design Systems, IO Methodology, SPISim, Synopsys, Teledyne LeCroy, Xpeedic Technology, and ZTE Corporation for making this event possible.

Since 1993 IBIS has provided the digital electronics industry with specifications to make signal, timing, and power integrity analyses much easier and faster. The challenges keep changing and the IBIS community keeps responding with new enhancements to the IBIS family of specifications, which the IC vendors, EDA tool companies, and system designers adopt readily.

Support for IBIS in Asia has been strong, and we are pleased to see the formation of an IBIS China Regional Forum. The IBIS Open Forum looks forward to continued innovation and contributions from technology companies around the world. Thank you!

Mike LaBonte
Signal Integrity Software (SiSoft)
Chair, IBIS Open Forum

WELCOME FROM MIKE LABONTE, IBIS OPEN FORUM

女士们，先生们，

作为 IBIS 开放论坛的主席我很高兴地欢迎大家来到 2015 年亚洲 IBIS 上海峰会，并感谢您的演讲和参与。我们特别要感谢我们的赞助商华为技术，Cadence Design Systems，IO Methodology Inc，SPISim , Synopsys，Teledyne LeCroy , Xpeedic Technology 和中兴通讯，是他们使本次活动成为可能。

从 1993 年至今，IBIS 为高速数字电路设计的信号，时序和功率完整性分析方面提供了更加容易和快捷电子模型行业规范。为适应不断变化的挑战，在 IC 供应商， EDA 工具公司和系统设计师的共同努力下， IBIS 正在继续不断加入新的功能和完善已有的 IBIS 系列规范。

在亚洲， IBIS 受到了更广泛的支持。 在这里我也要向大家宣布 IBIS 中国分会的正式成立，对此，IBIS 开放论坛期待着有更多的技术公司的参与和更多的技术创新和贡献。

谢谢！

Mike LaBonte (迈克 拉邦地)
SiSoft 公司
主席，IBIS 开放论坛

WELCOME FROM LIU SHUYAO, HUAWEI TECHNOLOGIES

Ladies and Gentlemen,

On behalf of Huawei Technologies, welcome to the 12th annual Asian IBIS Summit (China). I would like to express my appreciation to IBIS Open Forum and all the sponsors for co-organizing this event.

Since 2005, IBIS Asian Summit in China has been the top-level international conference in high speed digital design society in China. I am looking forward to work with IBIS members in China, and to expand our participations in the region.

Huawei has actively involved in all IBIS society's events. We hope to resolve high speed link issues with IBIS Open Forum, EDA vendors and IC vendors. Your comments and suggestions will be deeply appreciated !

Welcome all of you to Shanghai! Hope you will enjoy all the technical discussions and sharing throughout the meeting, and have a nice journey !

Thank you!
Shuyao Liu
Huawei Technologies

各位专家，各位来宾：

我代表华为公司，欢迎大家来参加第 12 届亚洲 IBIS 技术研讨会，衷心地感谢 IBIS 协会组织本次会议。

自从 2005 年以来，IBIS 技术研讨会已经成为了中国高速设计领域的一次盛会。我很高兴有机会与 IBIS 协会一起促进和扩大在该领域的分享。

华为积极参与各项 IBIS 活动，希望与 IBIS 协会、EDA 软件、芯片公司一道来共同解决许多高速链路设计上的挑战，欢迎大家会上讨论和建议。

欢迎 IBIS 专家来到上海，希望你们能够喜欢所有的技术讨论和会议分享，度过美好一天。

谢谢大家
华为公司 **柳**树**要**

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 **SIGN IN**
- Vendor Tables Open at 8:30

8:45 **WELCOME**
- Liu, Shuyao
  (Huawei Technologies, China)
- LaBonte, Mike (Chair, IBIS Open Forum)
  (Signal Integrity Software (SiSoft), USA)

9:00 **IBIS Chair's Report** **7**
LaBonte, Mike (Signal Integrity Software (SiSoft), USA)

9:25 **IBIS Model Simulation with RLC_dut** **16**
Chen, Xuefeng (Synopsys, China)

9:55 **Case Study: Modeling IBIS for Open_drain True Differential Pair Buffer** **22**
Wang*, Lance; Liang**, Yan
(*IO Methodology; **Maxim Integrated, USA)

10:20 **BREAK** (Refreshments and Vendor Tables)

10:40 **Differential Modeling Flow with Series Model in Verilog-A** **30**
Huang*, Wei-hsing; Gupta**, Sanjeev
(*SPISim, USA; **Sigintegrity Solutions, India)

11:10 **IBIS-AMI Model Generation with Quality** **40**
Liang, Skipper (Cadence Design Systems, China)

12:00 **FREE BUFFET LUNCH** (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

13:30 **Suggestion on Issuing VSR/CAUI-4 Based on IBIS-AMI Model 59**
Xu, Zhengrong (Huawei Technologies, China)

13:50 **Necessity for Integrating FEC Functionality for PAM4 in 64**
IBIS-AMI Model
Dong*, Xiaoqing; Huang**, Nick
(*Huawei Technologies;
**Shenzhen Zhongzeling Elecronics, China)

14:10 **The Impact of Channel Performance to 56G PAM4 Simulation 70**
Yin, Changgan; Zhu, Shunlin (ZTE Corporation, China)

15:00 **BREAK** (Refreshments and Vendor Tables)

15:20 **Achieving Full System Signal Integrity for High Speed 90**
Backplane Simulation
Dai, Wenliang (Xpeedic Technology, China)

15:50 **On-Die Decoupling Model Improvements for IBIS Power Aware 101**
Models
Wolff#, Randy; Viscardi##, Aniello
(Micron Technology; #USA, ##Italy)

16:15 **IBISCHK6 V6.1.3 and Executable Model File Checking 108**
Ross, Bob (Teraspeed Labs, USA)

15:40 **Touchstone Conversion Wrapper 117**
Ekholm, Anders (Ericsson, Sweden)

17:05 **DISCUSSION**

17:20 **CONCLUDING ITEMS**

17:30 **END OF IBIS SUMMIT MEETING**

IBIS Chair's Report

http://www.ibis.org/

Mike LaBonte
Signal Integrity Software
Chair, IBIS Open Forum

Asian IBIS Summit
Shanghai, China
November 11, 2016

Specification Development

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models

Other Work

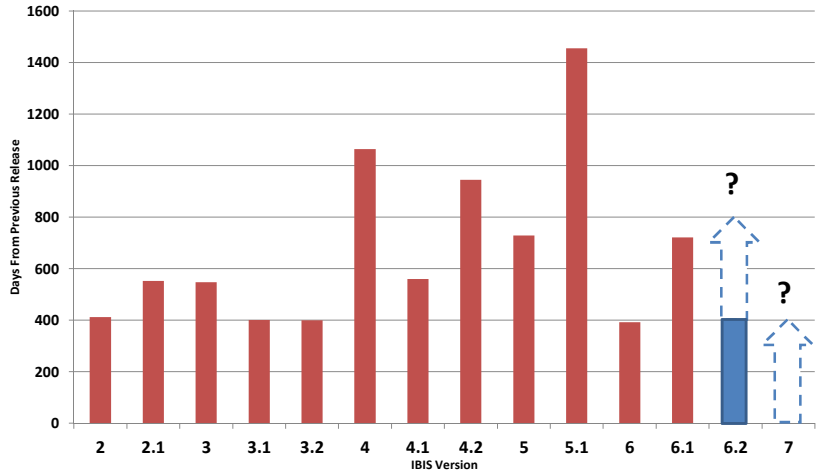
- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone® 2.0***
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

**Touchstone® is a registered trademark of Agilent Technologies, Inc.*

Specification Development

IBIS Version Development

As of 23-Oct-2016



Specification Development

Work In Progress

- Advanced Technology Modeling Task Group
  - IBIS 6.2 dedicated to reference node clarifications
  - Back-channel support (BIRD147.3)
  - C_comp model enhancements
  - Redriver flow enhancements
- Interconnect Task Group
  - External Package/on-die models using IBIS-ISS and Touchstone®
- IBIS Quality Task Group
  - IBISCHK enhancements and documentation

Specification Development

In Progress: IBIS 6.2

- Purpose: Clarify reference terminal conventions in IBIS
- BIRDs submitted, discussed in ATM Task Group
- Editorial Task Group will resume after BIRDs passed

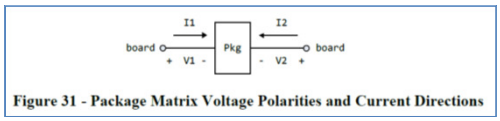


Figure 31 - Package Matrix Voltage Polarities and Current Directions

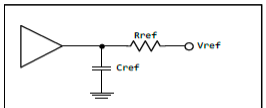


Figure 1 - Reference Load Connections

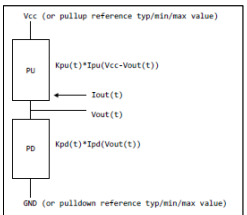
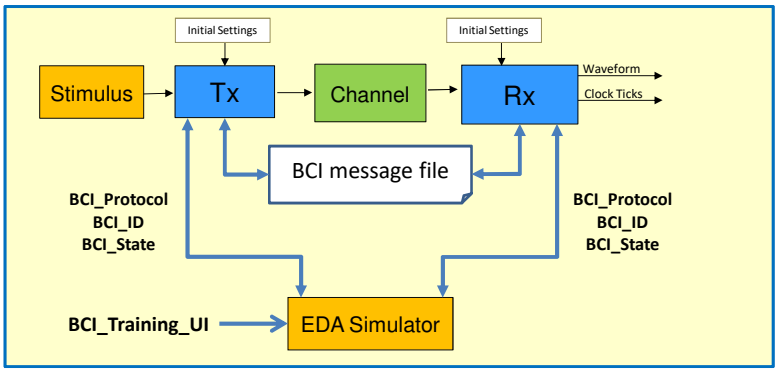


Figure 9 - Reference Data Collection

Specification Development

In Progress: Backchannel support

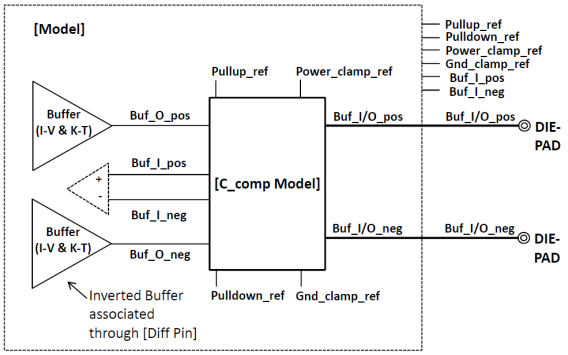
- Purpose: Backchannel to model time domain link training
- BIRD 147.3 recommended by ATM Task Group for acceptance



Specification Development

In Progress: C_comp Model Enhancements

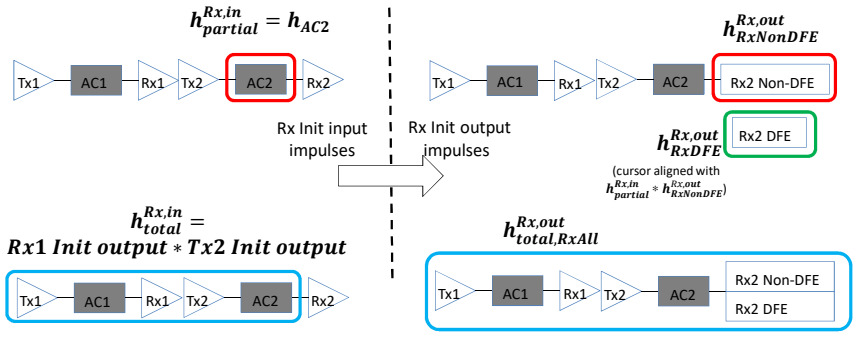
- Purpose: Accurate C_comp model supporting frequency and voltage dependence, using IBIS-ISS and Touchstone®
- In ATM Task group, BIRD not yet submitted



Specification Development

In Progress: Redriver Flow Enhancements

- Purpose: Provide full redriver channel impulse to Rx Init for optimization, eliminate the need for deconvolution
- In ATM Task group, BIRD not yet submitted



Specification Development

In Progress: Interconnect BIRD

- Purpose: External Package/on-die models using IBIS-ISS
- In Interconnect Task Group, BIRD (draft 42) not yet submitted

```
[Interconnect Model Set]      Full_ISS_PDN_sn_2
[Interconnect Model]          Full_ISS_buf_pin_2
File_IBIS-ISS   full_buf_pin.iss              full_buf_pin_2_typ
Number_of_terminals = 14
1  Pin_I/O      pin_name      A1    |  DQ1          DQ
2  Pin_I/O      pin_name      A2    |  DQ2          DQ
3  Pin_I/O      pin_name      A3    |  DQ3          DQ
4  Pin_I/O      pin_name      D1    |  DQS+         DQS
5  Pin_I/O      pin_name      D2    |  DQS-         DQS
6  Pin_Rail     signal_name   VDD   |  VDD          POWER
7  Pin_Rail     signal_name   VSS   |  VSS          GND
8  Buf_I/O      pin_name      A1    |  DQ1          DQ
9  Buf_I/O      pin_name      A2    |  DQ2          DQ
10 Buf_I/O      pin_name      A3    |  DQ3          DQ
11 Buf_I/O      pin_name      D1    |  DQS+         DQS
12 Buf_I/O      pin_name      D2    |  DQS-         DQS
13 Buf_Rail     signal_name   VDD   |  VDD          POWER
14 Buf_Rail     signal_name   VSS   |  VSS          GND
|
[End Interconnect Model]
[End Interconnect Model Set]
```


Specification Development

In Progress: Approved BIRDs

- All are targeted for IBIS 6.2

BIRD	Title
179	New IBIS-AMI Reserved Parameter Special_Param_Names
180	Require Unique Pin Names in [Pin]
182	POWER and GND [Pin] signal_name as [Pin Mapping] bus_label
183	[Model Data] Matrix Subparameter Terminology Correction

Specification Development

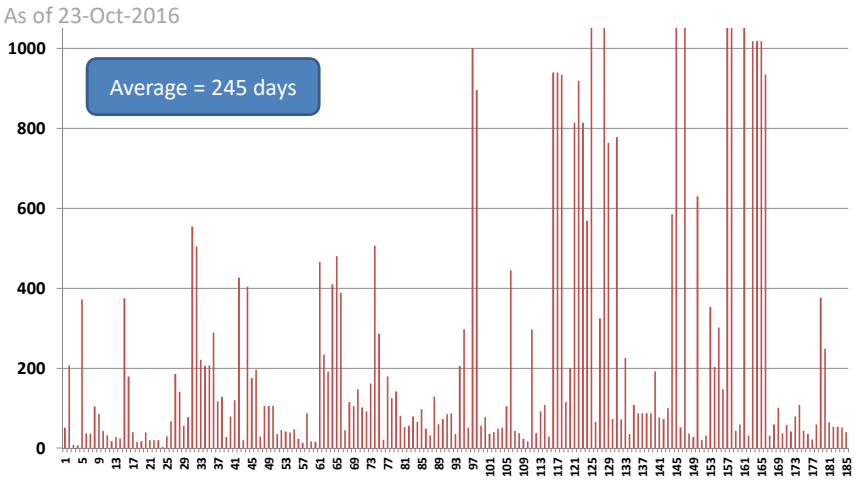
In Progress: Open BIRDs

- Some are targeted for IBIS 6.2
- Some are superseded by new BIRDs and will be rejected

125.1	Make IBIS-ISS Available for IBIS Package Modeling
145.3	Cascading IBIS I/O buffers with [External Circuit]s using the [Model Call] keyword
157	Parameterize [Driver Schedule]
158.3	AMI Touchstonefile (R) Analog Buffer Models
161.1	Supporting Incomplete and Buffer-only [Component] Descriptions
163	Instantiating and Connecting [External Circuit] Package Models with [Circuit Call]
164	Allowing Package Models to be defined in [External Circuit]
165	Parameter Passing Improvements for [External Circuit]s
166	Resolving problems with Redriver Init Flow
181	I-V Table Clarifications
184.1	Model_name and Signal_name Restriction for POWER and GND Pins
185.1	Section 3 Reserved Word Guideline Update

Specification Development

Days To Resolve BIRDs

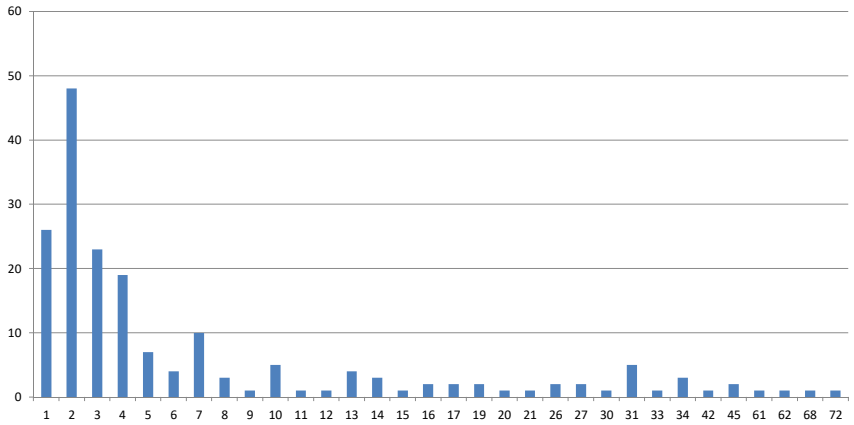


Specification Development

Most BIRDs Resolved < 9 Months

As of 23-Oct-2016

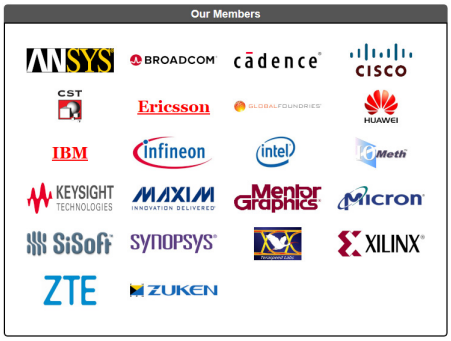
Number of BIRDs by Months Considered



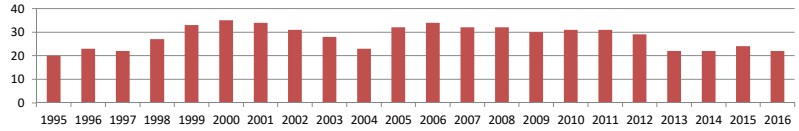
IBIS Chair's Report 13

Organization

22 IBIS Members



Number of Members by Year



IBIS Chair's Report 14

Organization

IBIS Officers 2016-2017

Chair:	*Mike LaBonte, Signal Integrity Software*
Vice-Chair:	*Lance Wang, IO Methodology Inc.*
Secretary:	*Randy Wolff, Micron Technology*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Anders Ekholm, Ericsson*
Webmaster:	*Mike LaBonte, Signal Integrity Software*
Postmaster:	*Curtis Clark, ANSYS*

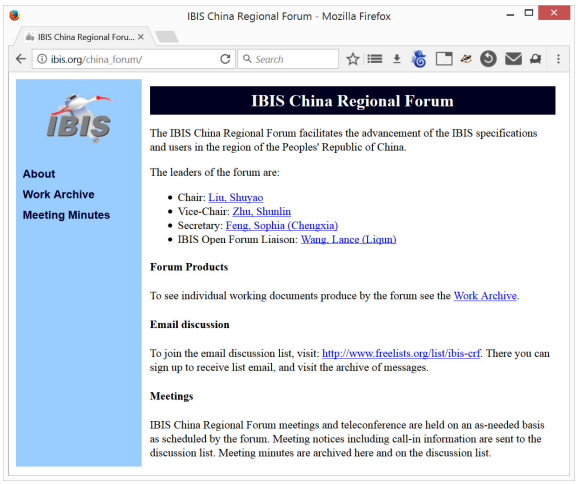
Organization

IBIS Meetings

- Teleconferences every week
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays, now suspended)
- IBIS Open Forum teleconference every 3 weeks
- IBIS Summit meetings: DesignCon, SPI, Shanghai, Taipei, Tokyo, EPEPS (2015)

Organization

New: China Regional Forum



[Thank You]

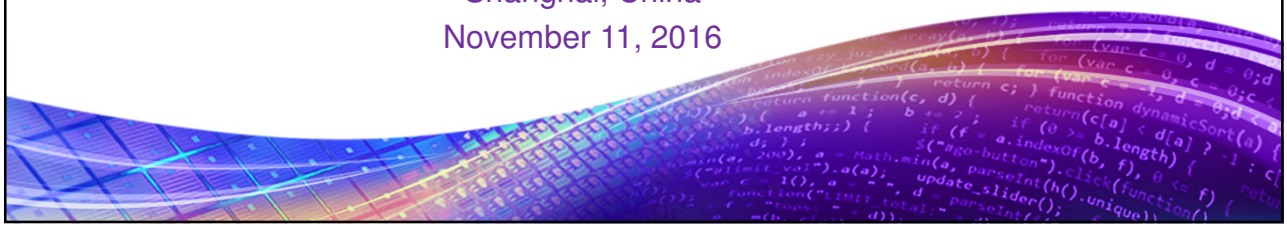
IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.

SYNOPSYS®
Silicon to Software™

IBIS Model Simulation with R/L/C_dut

Xuefeng Chen
Asian IBIS Summit Meeting
Shanghai, China
November 11, 2016



Outline

- Introduction of IBIS R/L/C_dut subparameters
- IBIS algorithm enhancement for R/L/C_dut
- Accuracy test of complete IBIS model with R/L/C_dut
- Summary

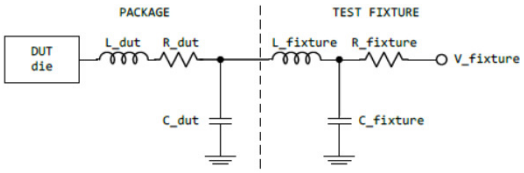
SYNOPSYS®

Introduction of IBIS R/L/C_dut subparameters

IBIS 3.2:

V-T waveform subparameters

The R_dut, C_dut, and L_dut subparameters are analogous to the package parameters R_pkg, C_pkg, and L_pkg and are used if the waveform includes the effects of pin inductance/capacitance



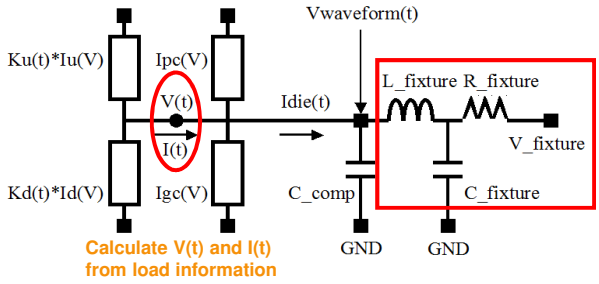
Example:

```
[Rising Waveform]
R_fixture = 50
V_fixture = 0.0
| C_fixture = 50p
| L_fixture = 2n
| C_dut = 7p
| R_dut = 1m
| L_dut = 1n
| Time              V(typ)
```

 3

SYNOPSYS

IBIS Algorithm Without R/L/C_dut



Two steps to get scaling coefficients of PU, PD (Ku,Kd)

1. Get $I_{die}(t)$ by V-T waveforms, C_comp and R/L/C_fixture : apply i=C*dv(t)/dt and v=L*di(t)/dt
2. Use the well known 2EQ/2UK algorithm:

0 = Ku(t) * Iu(Vwfm1(t)) + Ipc(Vwfm1(t)) - Kd(t) * Id(Vwfm1(t)) - Igc(Vwfm1(t)) - Idie(Vwfm1(t))
0 = Ku(t) * Iu(Vwfm2(t)) + Ipc(Vwfm2(t)) - Kd(t) * Id(Vwfm2(t)) - Igc(Vwfm2(t)) - Idie(Vwfm2(t))

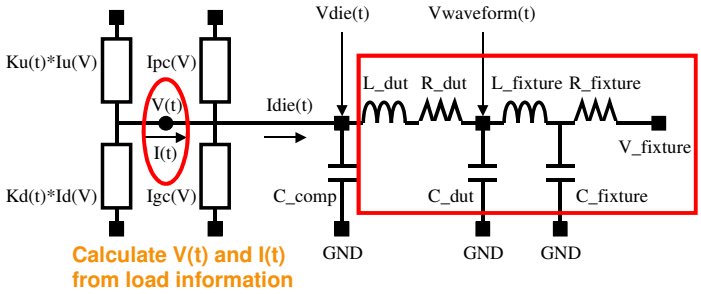
For details , please refer:

"IBIS Algorithm Including Reactive Loads", Xuefeng Chen, Asian IBIS Summit (China), September 11, 2007.

 4

SYNOPSYS

IBIS algorithm enhancement for R/L/C_dut



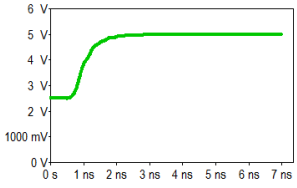
The step 1 of Vdie(t) & Idie(t) calculation extends to:

a) get I(L_fixture) by Vwaveform(t) and L/R/C/V_fixture.
b) get I(C_dut) by Vwaveform(t) and C_dut.
c) get I(L_dut) by above I(L_fixture) and I(C_dut).
d) get Vdie(t) by I(L_dut) , L_dut, R_dut and Vwaveform(t).
e) get I(C_comp) by Vdie(t) and C_comp
f) get Idie(t) by I(C_comp) and I(L_dut).

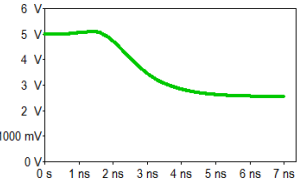
SYNOPSYS

A Complete IBIS Model with R/L/C_dut

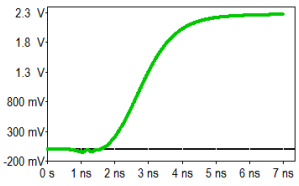
```
Model_type        I/O
C_comp            0.92pF
[Voltage Range]   5.000V
[Pulldown]
  …
[GND Clamp]
  …
[Pullup]
  …
[POWER Clamp]
  …
[Rising Waveform]
V_fixture = 5
R_fixture = 50
L_fixture = 2n
C_fixture = 3p
R_dut=5
L_dut=2n
C_dut=3p
  …
…
```



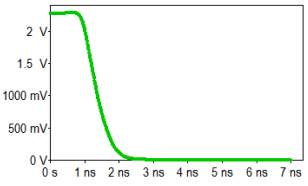
rising waveform (VCC)



falling waveform (VCC)



rising waveform (GND)

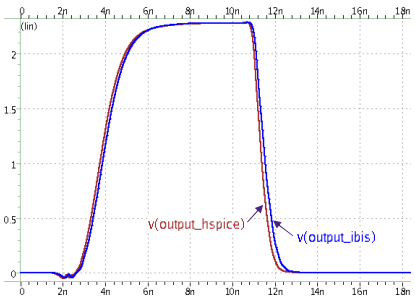


falling waveform (GND)

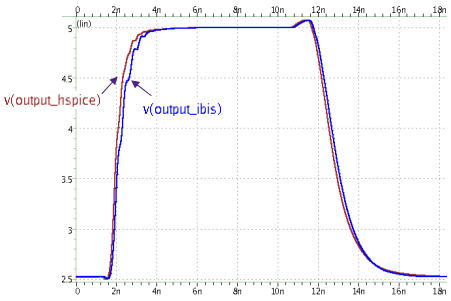
SYNOPSYS

Accuracy Test of the Complete IBIS Model with R/L/C_dut

The output result by original IBIS algorithm (ignore R/L/C_dut)
when the buffer is loaded with R/L/C/V_fixtures:



The buffer is loaded with fixtures to GND
(R=50, L=2n, C=3p, V=0)



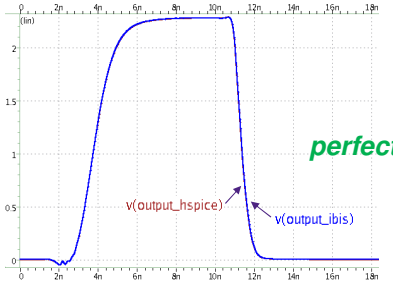
The buffer is loaded with fixtures to VCC
(R=50, L=2n, C=3p, V=5)

v(output_ibis): *IBIS output* v(output_hspice): *HSPICE transistor level buffer output*

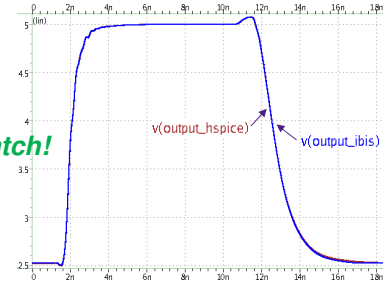
SYNOPSYS

Accuracy Test of the Complete IBIS Model with R/L/C_dut (Cont.)

The output result by enhanced IBIS algorithm (consider R/L/C_dut in V-T solving)
when the buffer is loaded with R/L/C/V_fixtures:



perfect match!



The buffer is loaded with fixtures to GND
(R=50, L=2n, C=3p, V=0)

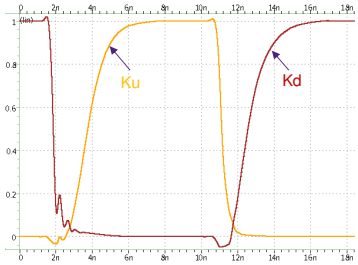
The buffer is loaded with fixtures to VCC
(R=50, L=2n, C=3p, V=5)

v(output_ibis): *IBIS output* v(output_hspice): *HSPICE transistor level buffer output*

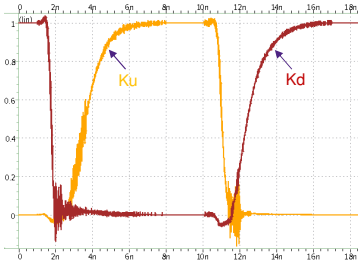
SYNOPSYS

Accuracy Test of the Complete IBIS Model with R/L/C_dut (Cont.)

Ku, Kd comparison between original IBIS algorithm and enhanced IBIS algorithm:



original algorithm



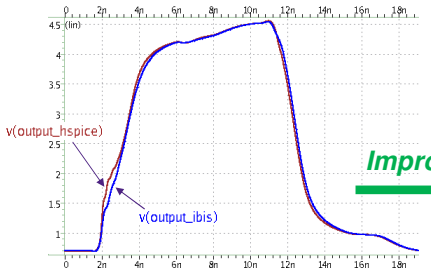
enhanced algorithm

Due to R/L/C_dut, the Ku, Kd results look more noisy.
But it contributes for much better accuracy of output waveform!

SYNOPSYS

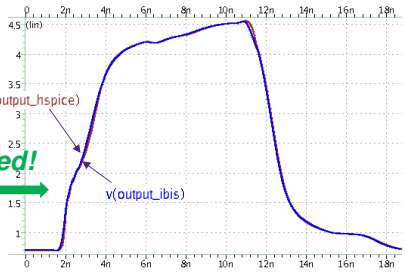
Accuracy Test of the Complete IBIS Model with R/L/C_dut (Cont.)

The output result comparison between original and enhanced IBIS algorithms when the buffer is loaded with W element and IBIS terminators:



Original IBIS algorithm result

Improved!



Enhanced IBIS algorithm result

v(output_ibis) : *IBIS output* v(output_hspice): *HSPICE transistor level buffer output*

SYNOPSYS

Summary

- Enhanced IBIS algorithm is provided to support the R/L/C_dut subparameters in V-T tables.
- The algorithm can get perfect match to transistor level buffer under the loading conditions of V-T extraction, and shows obvious accuracy improvement when the buffer is loaded with W element and IBIS terminator.
- The Ku & Kd results of V-T solving is very sensitive to R/L/C_dut. So IBIS model extractors need be cautious to use such subparameters.
- In fact, based on the algorithm, R/L/C_dut provides a solution to describe a little more complicated “C_comp” circuit due to below common situations:
  - ✓ *located between V-T extraction point and die pad*
  - ✓ *involved in V-T solving to get Vdie(t) & Idie(t)*
  - ✓ *the values are constant for different V-T tables.*
  - ✓ *need to be added in circuit during buffer simulation*

 11

SYNOPSYS®

SYNOPSYS®
Silicon to Software™

 12

SYNOPSYS®

Case Study:
Modeling IBIS for Open_drain True Differential Pair Buffer

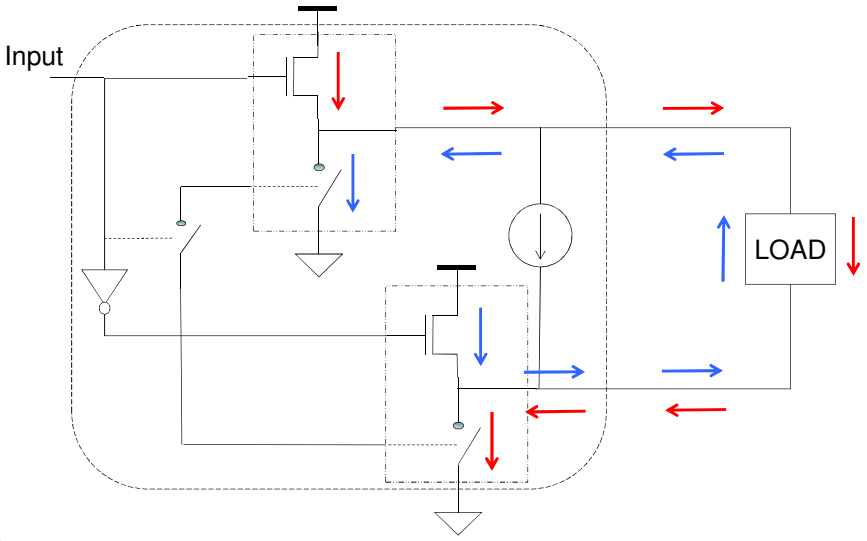
Lance Wang, IO Methodology Inc.
Yan Liang, Maxim Integrated

Asian IBIS Summit – Shanghai, China November 11th, 2016

Outline

- Open_drain Differential Pair Buffer Structure
- Review IBIS Modeling Method
  - Differential Pair Modeling Method
  - Output Type Buffer
  - Open_drain Type Buffer
- Practical Method for Open_drain Differential Pair Buffer
- Conclusions

Open_drain Differential Pair Buffer Structure

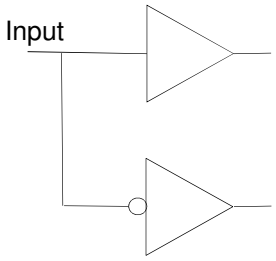


Review IBIS Modeling Method

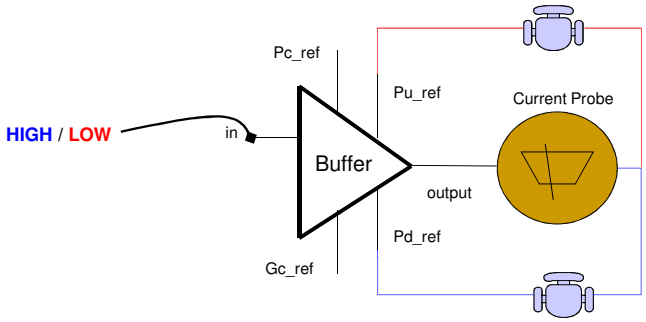
- Differential Pair Modeling Method
- Output Type Buffer
- Open_drain Type Buffer

Differential Pair Modeling Method

- IBIS uses two single-end models to be a differential pair
- IBIS uses [Diff Pin] to define two pins to be a differential pair pins
- Uses two opposite inputs as required

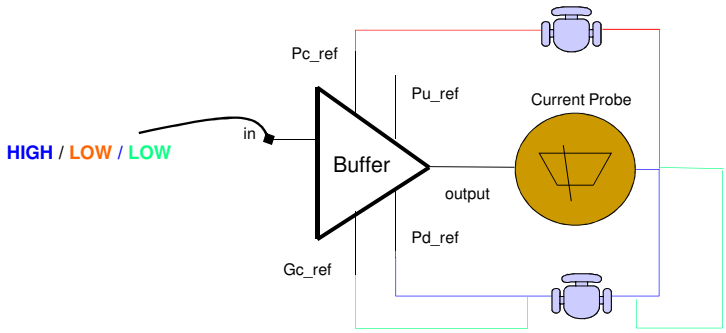


Output Type Buffer (non-inverting)



Set Input LOW to extract Pullup curve
Set Input HIGH to extract Pulldown curve

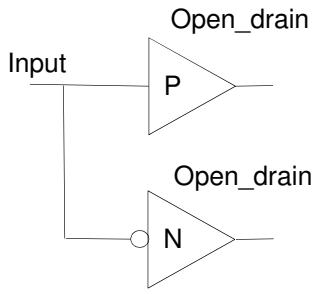
Open_drain Type Buffer



Set Input HIGH to extract Pulldown curve
Set Input LOW to extract PowerClamp curve
Set Input LOW to extract GroundClamp curve

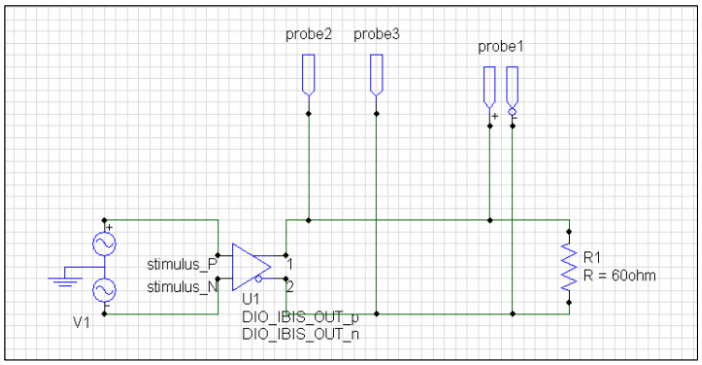
Practical Method for Open_drain Differential Pair Buffer

- As the normal method, we will use two Open_drain type IBIS models for Positive and Negative pins.

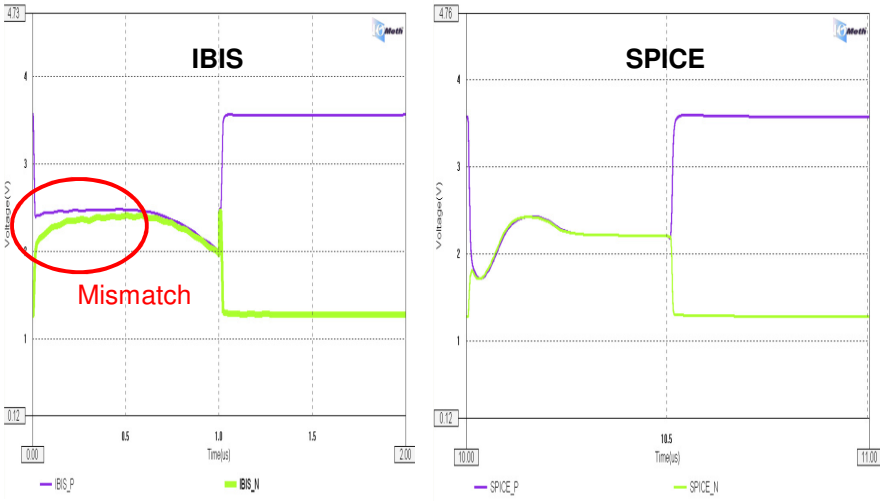


Let's validate

The Topology for Validation



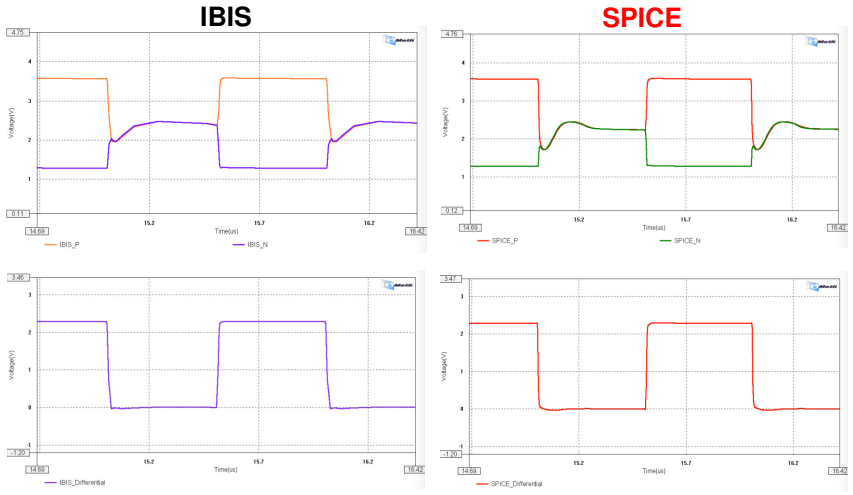
Validation Results



Root cause for mismatch and solution

- We missed some currents in the IBIS models
  - There is some current between P and N pins
  - IBIS Open_drain type model without Pullup curve. Assuming Pullup current is Zero
- Solution
  - We can use Output type model to capture all curve data
  - However, we need to use Open_drain type setting to capture the data

New solution validation result

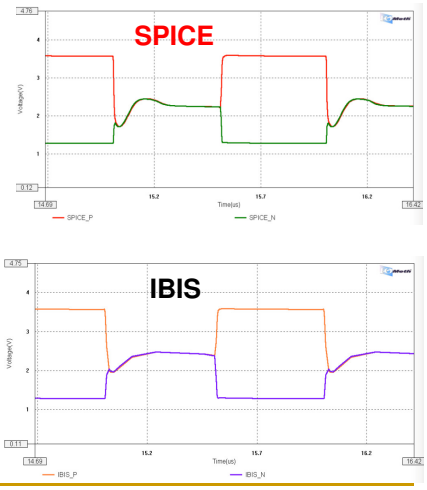


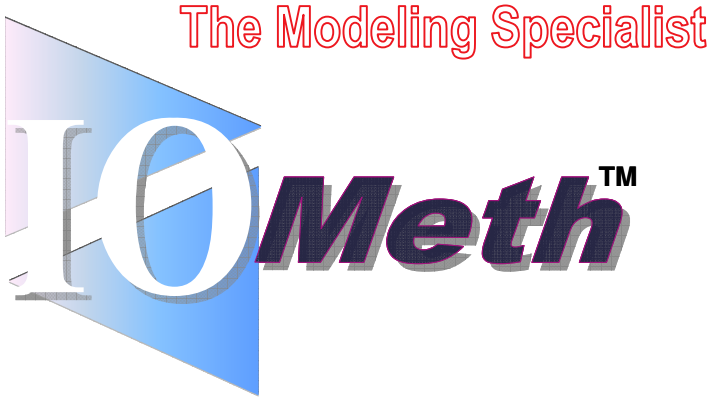
Conclusion

- Open_drain differential pair is a special case for IBIS modeling
  - IBIS Open_drain model is without the Pullup data
  - We need to use Output/IO type IBIS model to capture the Pullup data for this kind of differential pair buffer
    - However we need to IBIS Open_drain modeling setting for extractions
- IBIS C_comp needs to improve to be matched better

C_comp

- Currently, IBIS Spec only allows 4 values at the most
- We might need to have more C_comp values according DC levels and frequency changes
- Study is in process …





http://www.iometh.com

Differential Modeling Flow with Series Model in Verilog-A

Asian IBIS Summit
Shanghai, China
November 11, 2016

Wei-hsing Huang, SPISim
Wei-hsing.Huang@spisim.com
Sanjeev Gupta, SigIntegrity-Solutions
sanjeev@sigintegrity-solutions.com

1

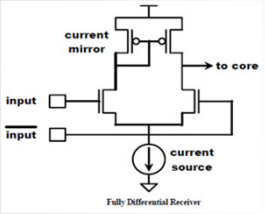
Agenda:

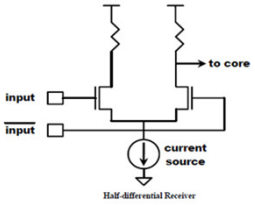
- Background & Motivation
- Verilog-A based modeling
  - Differential current
  - External model
- Flow & Validation
- Summary
- Q & A

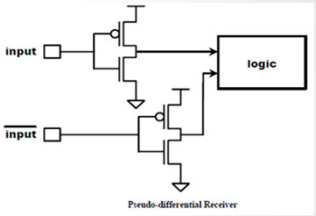
2

Background: (1, IBIS CookBook V4)

- Differential buffer: True/Half/Pseudo differential.







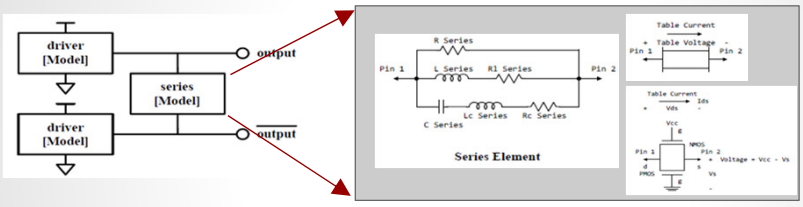
- [Diff Pin]: describe differential behavior between two pins.

```
[Diff Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
|
2      3      NA     NA     0ns    5ns
6      5      NA     NA     0ns    5ns
```

3

Method 1 for Half/True differential:

- [Series pin mapping]/Series Model:(2)(3)




```
[Diff_Pin]   inv_pin    vdiff   tdelay_typ tdelay_min tdelay_max
1       2       0.25    0       NA              NA
3       4       0       0       NA              NA
|
|*****************************************************************
|
[Series Pin Mapping]  pin_2    model_name      function_table_group
  1       2         R_SERIES_100
  3       4         R_SERIES_100
|
|*****************************************************************
|                           Model R_SERIES_100
|*****************************************************************
|
[Model]             R_SERIES_100
Model_type          Series
```

4

Method 2 for Half/True differential:

- [External Model]: Spice/VHDL-AMS/Verilog-AMS/IBIS-ISS**(4)**

```
[Model]          VHDLAMS-DRV
Model_type       Output
Polarity         Non-Inverting
C_comp           4.60pF              3.50pF              6.00pF
Vmeas = 1.15V
Cref  = 1pF
Rref  = 50ohms
Vref  = 0V
|
[External Model]
Language VHDL-AMS
|
| Corner corner_name file_name          circuit_name entity(architecture)
Corner   Typ         ideal_driver.vhd   driver_ideal(linear)
Corner   Min         ideal_driver.vhd   driver_ideal(linear)
Corner   Max         ideal_driver.vhd   driver_ideal(linear)
|
| Ports List of port names (in same order as in VHDL-AMS)
Ports D_drive A_puref A_pdref A_signal
|
[End External Model]
```

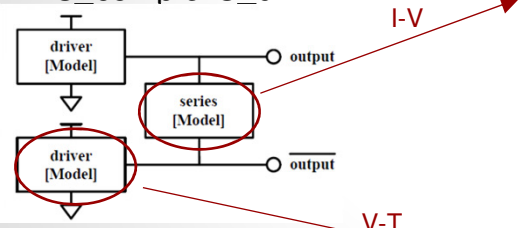
Input_diff Output_diff I/O_diff 3-state_diff	These model types specify that the model defines a true differential model available directly through the [External Model] keyword documented in Section 6.3.

Method 1 & 2 can be used together!

5

Background:

- Data extraction:
  - Common-mode current
  - Differential current
  - C_comp & C_diff



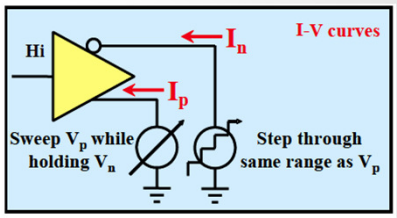


Figure 4.13 – I-V Table Extraction Fixture for a Differential Buffer

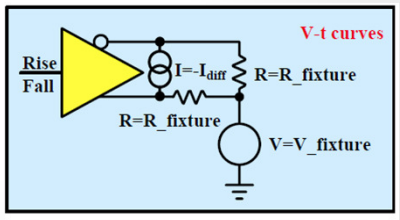
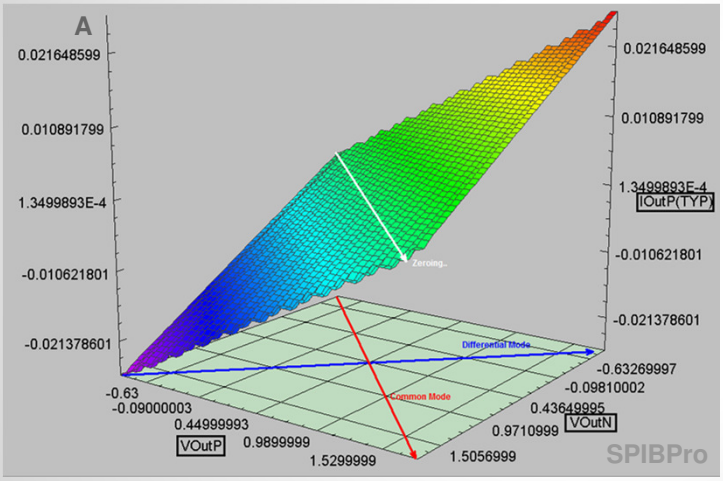
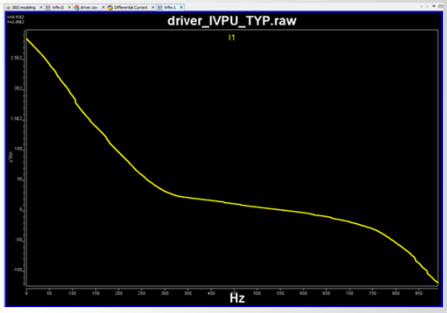


Figure 4.18 – V-T Table Extraction Fixture for a Differential Buffer

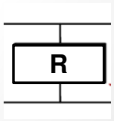
6

Design 1:





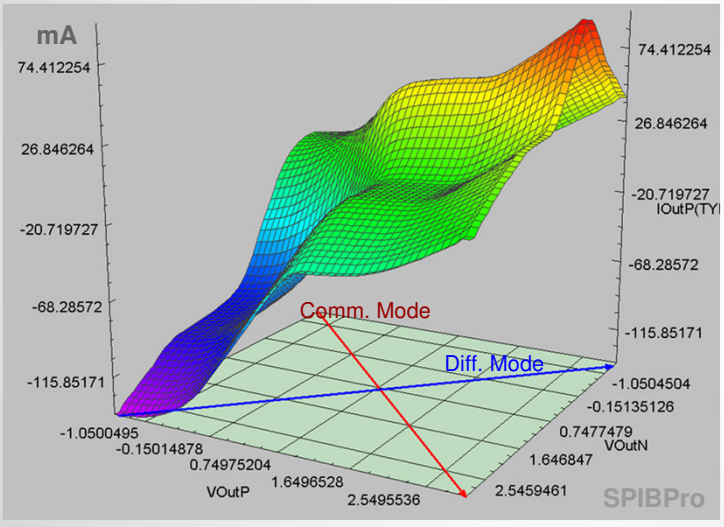
I Comm. Mode as PU/PD, PC/GC



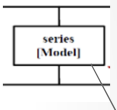
A simple “Series R” can describe this particular design

Shifted surface as differential series elem.

Design 2:



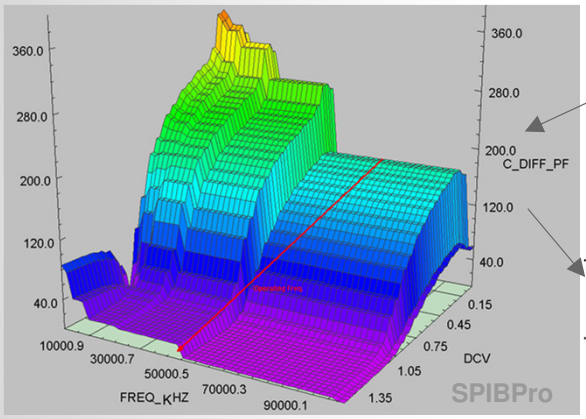
Need to describe this surface data in design 2 for V-T extraction
Affect DC steady states (e.g. mismatch)

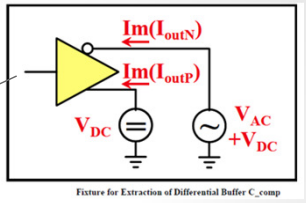


Options:

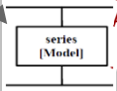
- Surface fit in MSE sense:
  - Need to check residue
  - Translate to EFGH elements
- Series MOSFET
  - Or Series current
- **Behavioral model?**

Design 2 C_diff:





Need to describe this surface data for V-T extraction as well
Affects final transient accuracy

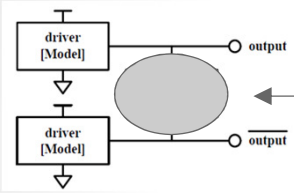


Options:
- Summarize and add single Series C
- **Behavioral model?**

9

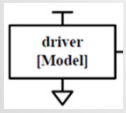
Motivations:

- Limitation of “Generic” series model:

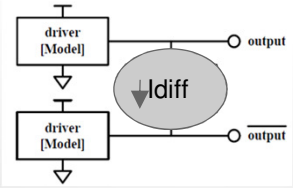


Series Elements:
1. Rigid syntax
2. Condition is fixed (e.g. no polarity)
3. Modeling flow interruption
   a. Surface fit ?
   b. Generate tentative series-elem?

- Accuracy of transient data for V-T extraction:



=



+

Inaccurate TR data will pollute waveform...

?

10

Verilog-A based Diff. current model:

```
// Disclaimer:
// This Verilog-A model is to subtract differential current for
// true/half differential IBIS modeling.
//
// [Usage]
//
//   O------+-------------+-------O OutP
//   InpP   |             |
//          |  Diff       |  +-----+
//          |  Drv.  >    |  VA-MODEL
//          |             |  +-----+
//   O------+-------------+-------O OutN
//   InpN   |             |
//
// 1. Please refer to IBIS cook book. Differential model's VT extraction
// 2. Connect this VA model like the schematic above
// 3. Prepare corner specific differential_current table using IV data
// 4. Differential current will be subtracted during VT simulation
// 5. Resulting transient waveform can be used for VT data table
//
// HSpice Verilog-A Syntax:
// .HDL "SPIBPro_DiffI.va"
// XDiffI NODEN NODEP SPIDiffI
//=============================================================

//============================== TYP ==============================
module SPIDiffI_TYP(nodeP, nodeN);
electrical nodeP, nodeN;
inout      nodeP, nodeN;
parameter real cDiff = 1.000E-11;

real       cDifI; // differential current due to c_diff
real       rDifI; // differential current due to resistance
real       voltP; // P node voltage and slew rate
real       voltN; // N node voltage and slew rate

analog begin
  voltP = V(nodeP);
  voltN = V(nodeN);

  // differential current due to DC steady state
  rDifI = $table_model(voltN, voltP, "driver_TYP.csv", "1L,1L");

  // differential current due to c_diff
  cDifI = ddt(voltP - voltN) * cDiff;

  // current flow between P and N
  I(nodeP, nodeN) <+ -(rDifI + cDifI);
end
endmodule
```

A Verilog-A device can be used in differential V-T extraction.

- Behavioral device is very versatile
- Support operator like ddt, if .. else
- Supports 1/2D look-up table **(5), (6)**

```
#Differential current in mA
#VOutN   VOutP   IDiff_Typ
-1.50E+00  -1.50E+00   0.00E+00
-1.50E+00  -1.46E+00  -7.83E+00
-1.50E+00  -1.41E+00  -1.59E+01
-1.50E+00  -1.37E+00  -2.41E+01
-1.50E+00  -1.32E+00  -3.25E+01
-1.50E+00  -1.28E+00  -4.13E+01
-1.50E+00  -1.23E+00  -5.03E+01
-1.50E+00  -1.19E+00  -5.95E+01
-1.50E+00  -1.14E+00  -6.91E+01
-1.50E+00  -1.10E+00  -7.89E+01
-1.50E+00  -1.05E+00  -8.90E+01
-1.50E+00  -1.01E+00  -9.94E+01
-1.50E+00  -9.60E-01  -1.10E+02
```

11

Verilog-A for V-T extraction:

```
//============================== TYP ==============================
module SPIDiffI_TYP(nodeP, nodeN);
electrical nodeP, nodeN;
inout      nodeP, nodeN;

parameter real freq = 1.0E9;

real       cDifI; // differential current due to c_diff
real       rDifI; // differential current due to resistance
real       voltP; // P node voltage and slew rate
real       voltN; // N node voltage and slew rate
real       cDiff; // differential capacitance

analog begin
  voltP = V(nodeP);
  voltN = V(nodeN);

  // differential current due to DC steady state
  rDifI = $table_model(voltN, voltP, "driver_TYP.csv", "1L,1L");

  // differential current due to c_diff
  cDiff = $table_model(voltN, freq, "driver_CDIF.csv", "1L,1L");
  cDifI = ddt(voltP - voltN) * cDiff;

  // current flow between P and N
  I(nodeP, nodeN) <+ -(rDifI + cDifI);
end
endmodule
```

Voltage & freq. Dependent C_Diff
(or use cross() to find freq. dynamically)

```
//============================== TYP ==============================
module SPIDiffI_TYP(nodeP, nodeN);
electrical nodeP, nodeN;
inout      nodeP, nodeN;

parameter real freq  = 1.0E9; // current working frequency
parameter real freq1 = 5.0E8; // cdiff at frequency 1
parameter real freq2 = 2.0E9; // cdiff at frequency 2

real       cDifI; // differential current due to c_diff
real       rDifI; // differential current due to resistance
real       voltP; // P node voltage and slew rate
real       voltN; // N node voltage and slew rate
real       cDif1, cDif2, cDiff; // differential capacitance

analog begin
  voltP = V(nodeP);
  voltN = V(nodeN);

  // differential current due to DC steady state
  rDifI = $table_model(voltN - voltP, "driver_TYP.csv", "1L,1L");

  // differential current due to c_diff
  cDiff1 = $table_model(voltN, "driver_CDIF1.csv", "1L,1L"); // at freq1 = 500M
  cDiff2 = $table_model(voltN, "driver_CDIF2.csv", "1L,1L"); // at freq2 = 2G
  cDiff  = (cDiff2 - cDiff1) / (freq2 - freq1) * (freq - freq1) + cDiff1;
  cDifI  = ddt(voltP - voltN) * cDiff;
```

Simulator only supports 1D table?
2D bi-linear look-up can still be done

12

Completed Series model:

```
[Pin]  signal_name          model_name          R_pin      L_pin      C_pin
1      out_p                driver              65.00m     4.50nH     0.85pF
2      out_n                driver              65.00m     4.50nH     0.85pF
|
[Series Pin Mapping]    pin_2    model_name  function_table_group
|
1 2       seriesmdl
```

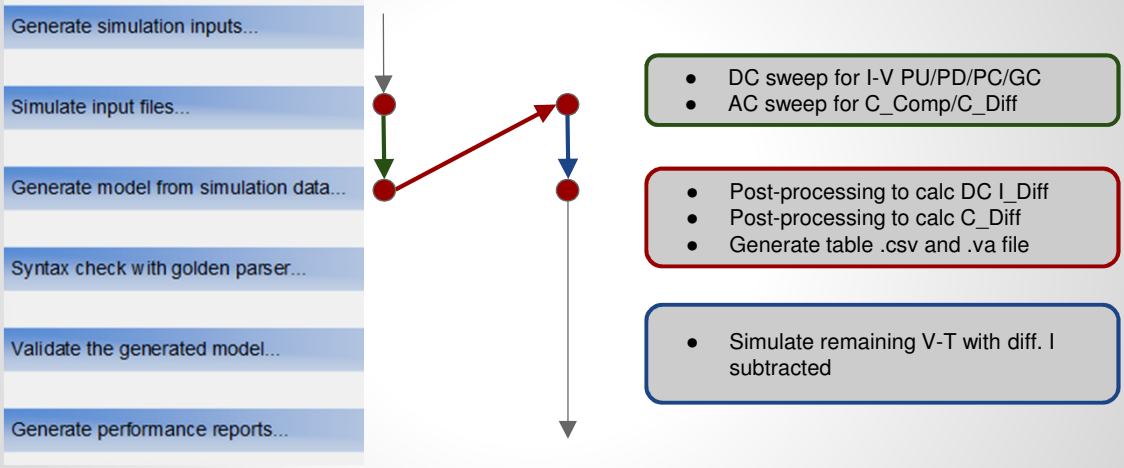
```
[Model]        seriesmdl
Model_type     Series
|                          typ                 min                 max
C_comp           4.60pF          3.50pF          6.00pF
|                          typ                 min                 max
|                          typ                 min                 max
[External Model]
Language Verilog-AMS
|
|  Corner corner_name file_name          circuit_name entity(architecture)
Corner   Typ          series_typ.va     series_va
Corner   Min          series_min.va     series_va
Corner   Max          series_max.va     series_va
|
|  Ports List of port names
Ports A_pos A_neg
|
[End External Model]
|
|
[Temperature Range]       27.00               70.00               0.000
[Voltage Range]           3.30V               3.13V               3.46V
```

```
[Model]        seriesmdl
Model_type     Series
|                          typ                 min                 max
C_comp           4.60pF          3.50pF          6.00pF
|                          typ                 min                 max
|                          typ                 min                 max
[External Model]
Language Verilog-AMS
|
|  Corner corner_name file_name          circuit_name entity(architecture)
Corner   Typ          series_typ.va     series_va
Corner   Min          series_min.va     series_va
Corner   Max          series_max.va     series_va
|
|  Ports List of port names
Ports A_pos A_neg
|
[End External Model]
|
|
[Temperature Range]       27.00               70.00               0.000
[Voltage Range]           3.30V               3.13V               3.46V
|
|*************************************************************************
[R Series] 100ohm 90ohm 110ohm
[C Series] 5pF 4pF 6pF
```

- Verilog-A as external model for model type “Series”
- Verilog-A can work with existing (generic) series model to provide extra accuracy if needed.

13

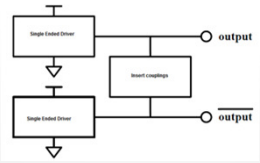
Differential modeling flow:



14

Modeling flow validation:

- Use an existing single-ended driver for P and N
- Insert approximate non-linear behavioral R/L/C elements between P and N outputs
- Flow should recreate same PU/PD/PC/GC as driver
- I-V surface plot should reveal inserted resistance
- C_Diff/C_Comp surface should reveal inserted cap
- Correlations of V-T table depends on I_Diff accuracies.



15

Summary:

- Verilog-A for differential V-T extraction
  - Versatile, supports many operators
    - E.g. ddt(Vx), $table_model for 1D/2D lookup
    - Streamlines modeling flow
  - Extract transient differential current
    - Improve V-T extraction accuracies
    - Use Verilog-A to remove rigid series syntax
- External model for “Series”:
  - [External model] supports “Series” type model
  - Can work with generic series model

16

References:

1. IBIS Cookbook V4
   https://ibis.org/cookbook/cookbook-v4.pdf
2. IBIS summit Jan/Mar 2001 by Hazem Hegazy (Mentor)
   https://ibis.org/summits/jan01/hegazy.zip
   https://ibis.org/summits/mar01/hegazy.zip
3. IBIS summit 2002 ~ 2004 by Arpad Muranyi (Intel)
   https://ibis.org/summits/oct02/muranyi.pdf
   https://ibis.org/summits/oct03/muranyi.pdf
   https://ibis.org/summits/feb04a/muranyi2.pdf
4. IBIS summit 2014 ~ 2015 by Shivani Shama et. al. (Cadence)
   https://ibis.org/summits/nov14b/sharma.pdf
   https://ibis.org/summits/nov15b/liang.pdf
5. Verilog A Language Reference Manual (LRM, Vendor Specific)
   http://accellera.org/images/downloads/standards/v-ams/VAMS-LRM-2-3-1.pdf
6. HSpice User's Manual

17

Q & A

18


SPISIM
EDA Expertise in Signal, Power Integrity & Simulation
19
SPISim is an InSync member.
SYNOPSYS
Integrated with
HSPICE®
Learn More >>

IBIS-AMI Model Generation -With Quality

Skipper Liang
Asian IBIS Summit, Shanghai, China
November 11, 2016

cadence

Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
  2. RX – An Input Buffer + AGC + CTE
  3. A System – TX + Channel + RX
- Conclusion

cadence

1

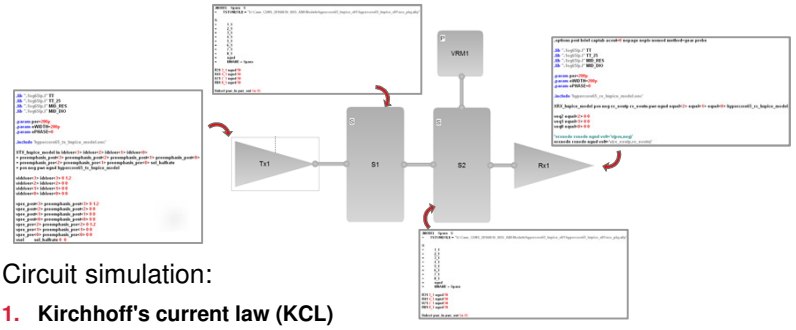
Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
  2. RX – An Input Buffer + AGC + CTE
  3. A Serdes – TX + Channel + RX
- Conclusion

cadence

Circuit Simulation–

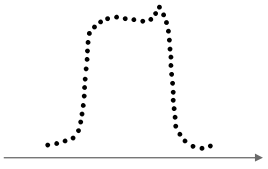
Using transistor **SPICE netlist** model



- Circuit simulation:
  1. **Kirchhoff's current law (KCL)**

     At any node (junction) in an electrical circuit, the sum of current flowing into that node is equal to the sum of currents flowing out of that node
  2. **Kirchhoff's voltage law (KVL)**

     The directed sum of the electrical potential differences (voltage) around any closed network is zero



cadence

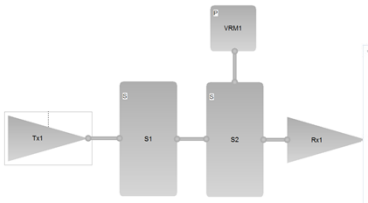
Traditional signoff flow –
Using transistor **SPICE netlist** model (con't)

Advantages:

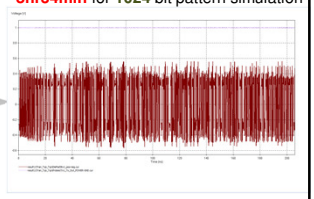
- Accurate PI prediction under **limited** bits transmission
- Accurate jitter prediction under **limited** bits transmission

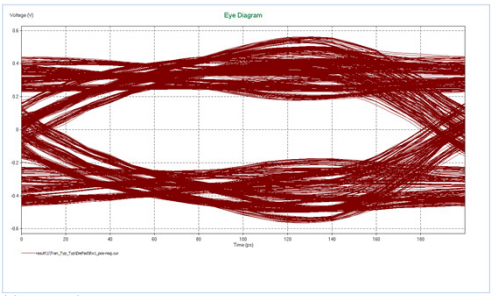
Disadvantages:

- Very slow for SPICE netlist model - Takes weeks/months to get bit error-rate (BER) prediction
- Can't model the adaptive mechanism in RX



8hr34min for **1024** bit pattern simulation





cadence

Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
  2. RX – An Input Buffer + AGC + CTE
- Conclusion

cadence

LTI – Linear time invariant (con't.)

- Signal expressed in an impulse-train format:
  - Impulse:

$$\delta(t) = \begin{cases} 0, other\ than\ t = 0 \\ \infty, t = 0 \end{cases}$$

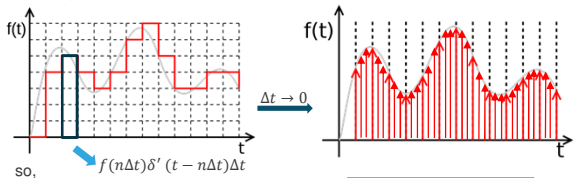
so, $\int_{-\infty}^{\infty} \delta(t)dt = 1$

  - Quasi-Impulse:

$$\delta'(t) = \begin{cases} 0, |t| > \frac{\Delta t}{2} \\ \frac{1}{\Delta t}, |t| \le \frac{\Delta t}{2} \end{cases}$$

so, $\int_{-\infty}^{\infty} \delta'(t)dt = 1$

  - Any Signal:



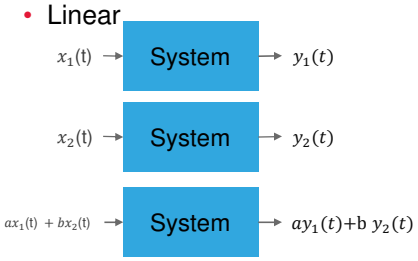
so, $f(nΔt)δ'(t - nΔt)Δt$

$$f(t) = \sum_{n=-\infty}^{\infty} f(n\Delta t)\delta'(t - n\Delta t)\Delta t \rightarrow f(t) = \int_{-\infty}^{\infty} f(\tau)\delta(t - \tau)d\tau$$

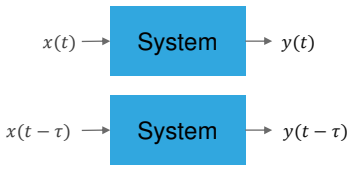
cadence

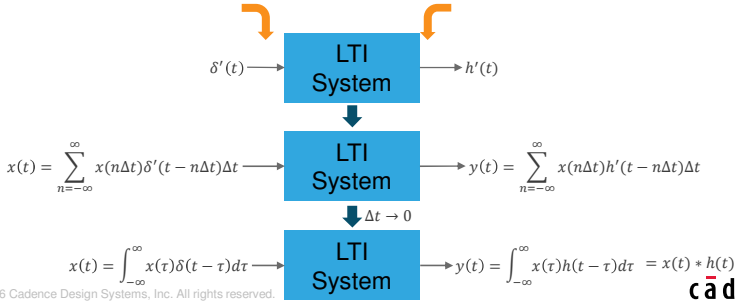
LTI – Linear time invariant (Con't.)

- Linear



- Time Invariant

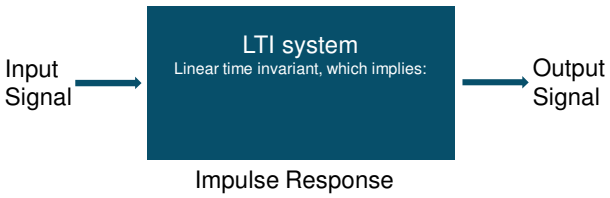


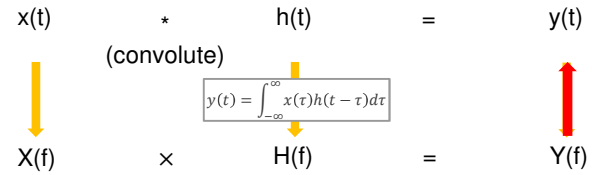


cadence

Channel-Simulation

- Channel simulation :





Multi-times faster than circuit simulation!!

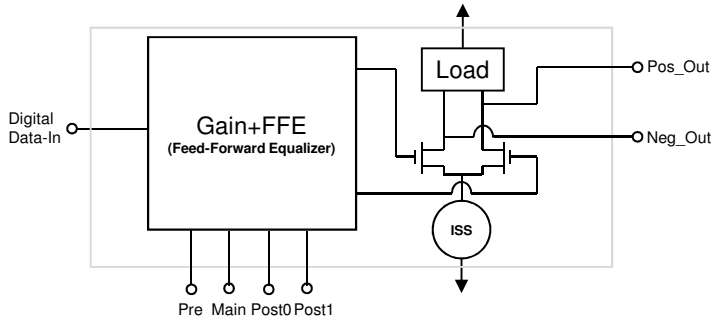
cadence

Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
  2. RX – An Input Buffer + AGC + CTE
- Conclusion

cadence

What is IBIS+AMI model (Example: TX)

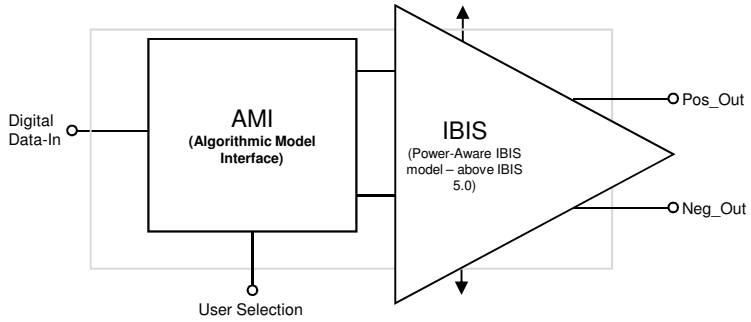


Accompanied with channel simulator:

- PI prediction with good accuracy without limits on transmission bits
- Jitter prediction with good accuracy without limits on transmission bits
- Very fast for IBIS+AMI netlist model - Takes minutes to get BER prediction
- Can model the adaptive mechanism in RX

cadence

What is IBIS+AMI model (Example: TX)



Accompanied with channel simulator:

- PI prediction with good accuracy without limits on transmission bits
- Jitter prediction with good accuracy without limits on transmission bits
- Very fast for IBIS+AMI netlist model - Takes minutes to get BER prediction
- Can model the adaptive mechanism in RX

But you might be concerned:

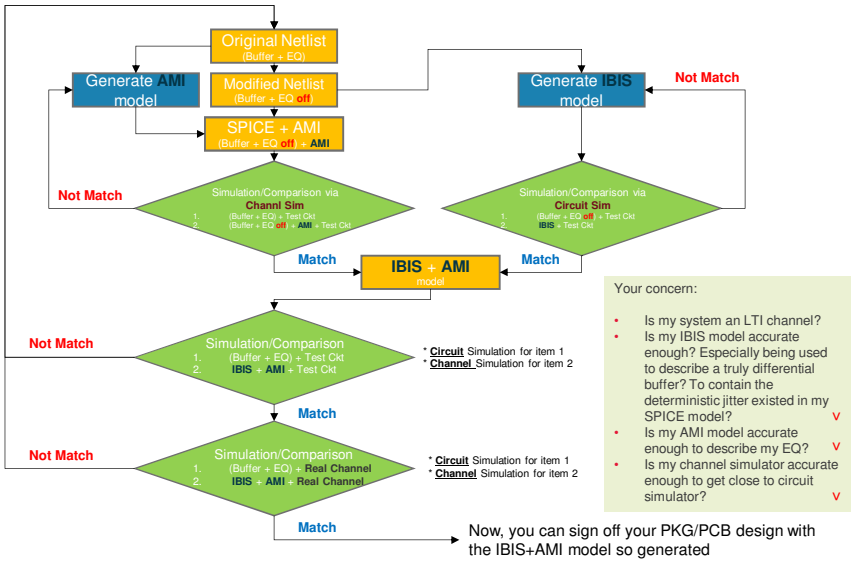
cadence

Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – **Validation** is the **KEY**!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
  2. RX – An Input Buffer + AGC + CTE
  3. A System: TX + Channel + RX
- Conclusion

cadence

IBIS+AMI model generation flow

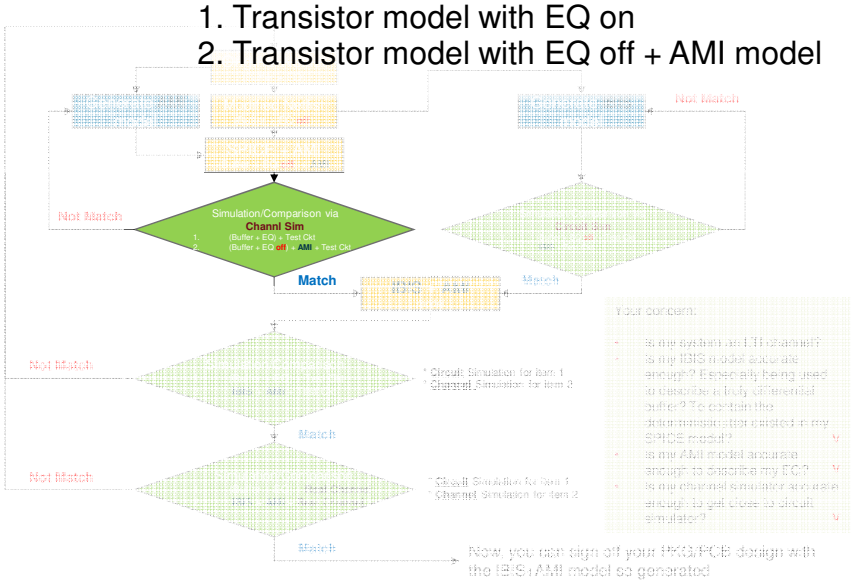


cadence

7

Validation 1: Channel Simulation for

1. Transistor model with EQ on
2. Transistor model with EQ off + AMI model



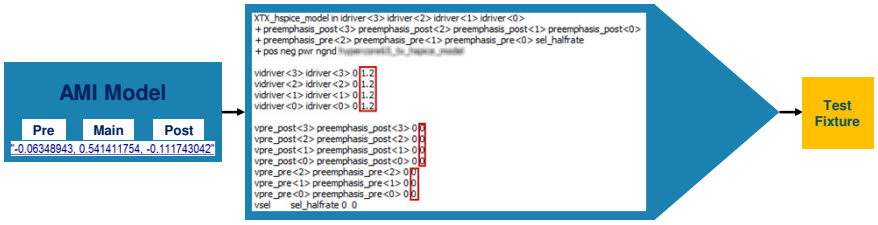
cadence

Validation 1: Channel Simulation for

1. Transistor model with EQ on

To qualify the AMI model so generated.

2. Transistor model with EQ off + AMI model

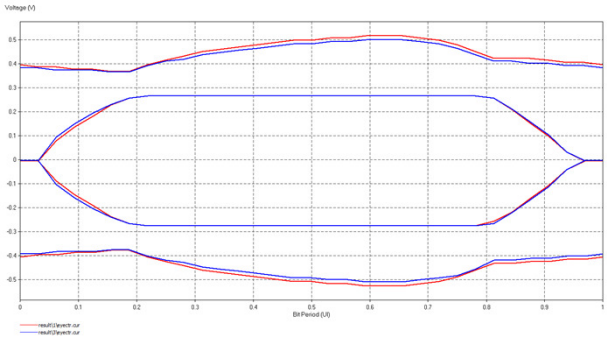


cadence

Validation 1: Channel Simulation for

1. Transistor model with EQ on
2. Transistor model with EQ off + AMI model

To qualify the AMI model so generated.

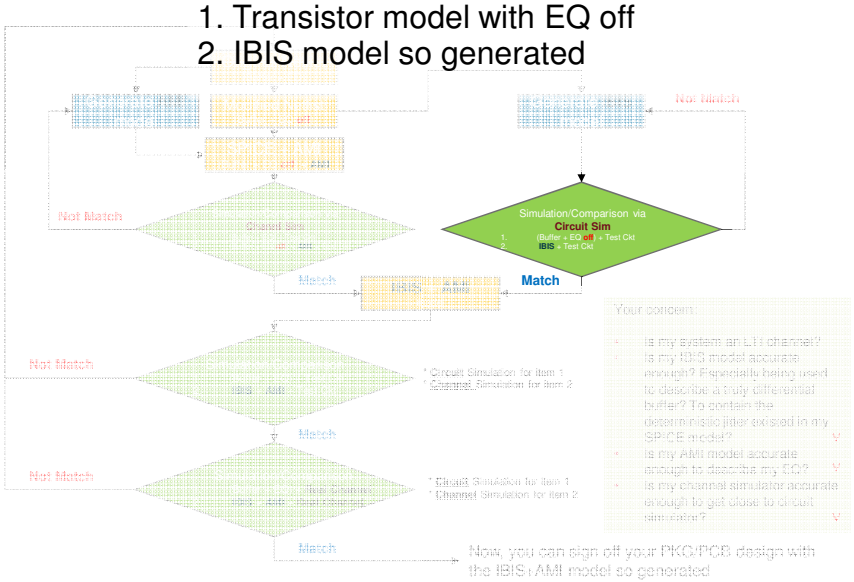


Why **Channel Simulation**?:
1. AMI model can only be used in **Channel Simulation**
2. Put transistor models under **Channel Simulation** will narrow down the possible cause for any difference happened here to the AMI model so generated.

cadence

Validation 2: Circuit Simulation for

1. Transistor model with EQ off
2. IBIS model so generated

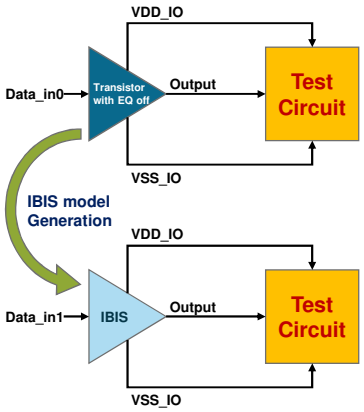


cadence

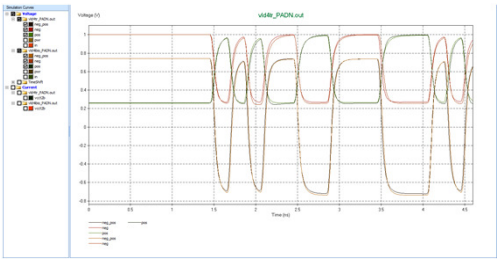
Validation 2: Circuit Simulation for

To qualify the IBIS model so generated.

1. Transistor model with EQ off
2. IBIS model so generated



Validated by Circuit Simulator

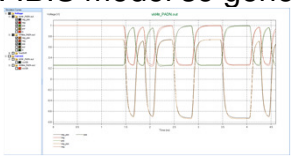


cadence

Validation 2: Circuit Simulation for

To qualify the IBIS model so generated.

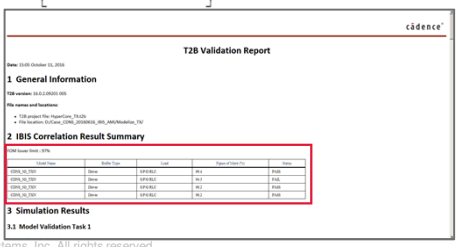
1. Transistor model with EQ off
2. IBIS model so generated



Define a "mark" and a "target" to tell the quality of the IBIS model so generated

$$FOM = 100 \bullet \left[1 - \frac{\sum_{i=1}^{N} |Y_i(LAB) - Y_i(IBIS)|}{\Delta Y \bullet N}\right]$$

ΔY: (Max-Min) of Circuit Simulation Waveform



cadence

T2B Validation Report

1 General Information

2 IBIS Correlation Result Summary

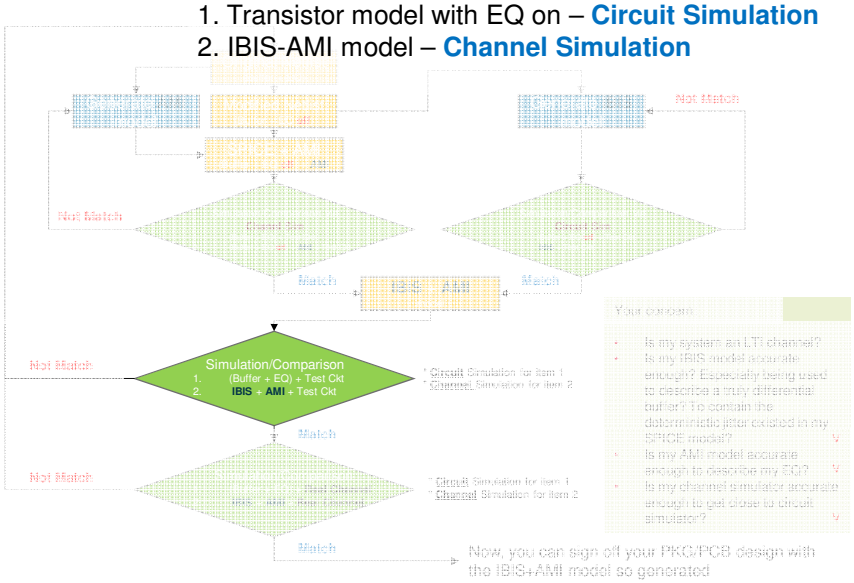
3 Simulation Results

3.1 Model Validation Task 1

cadence

Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

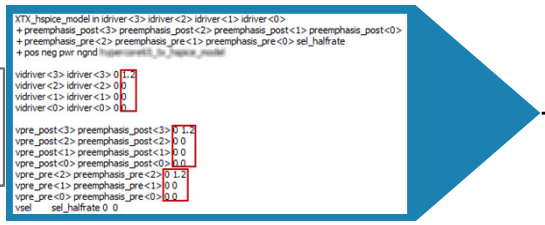


cadence

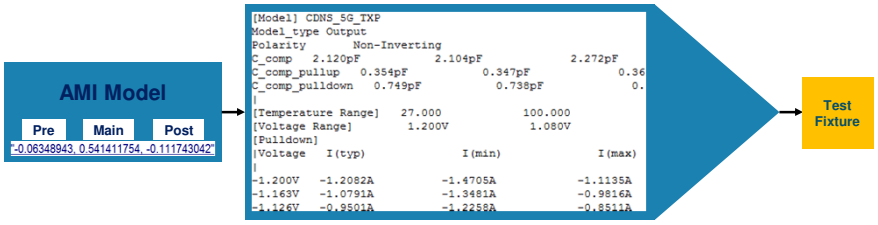
Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**

To qualify the IBIS-AMI model so generated.



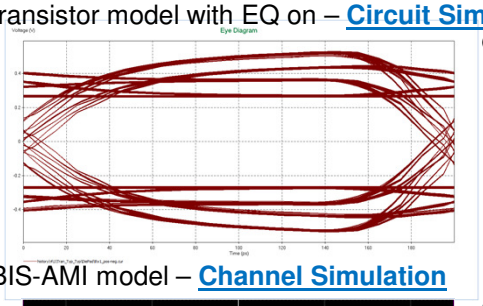
2. IBIS-AMI model – **Channel Simulation**



cadence

Validation 3: **Test Circuit** follows

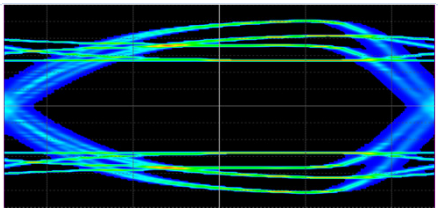
1. Transistor model with EQ on – **Circuit Simulation**



(1,024 bits transmitted)

To qualify the IBIS-AMI model so generated.

2. IBIS-AMI model – **Channel Simulation**



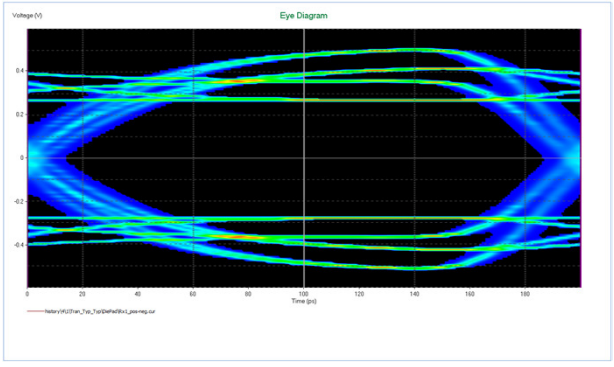
(1e+16 bits transmitted)

cadence

Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

To qualify the IBIS-AMI model so generated.

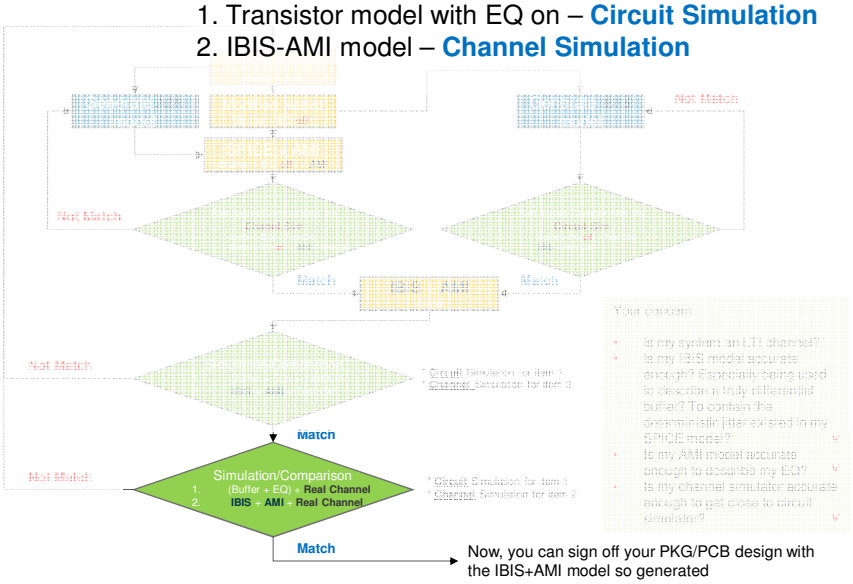


Also, to qualify the Channel Simulator – if the Channel Simulator behavior close enough to the Circuit Simulator.

cadence

Validation 4: **Real Channel** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**



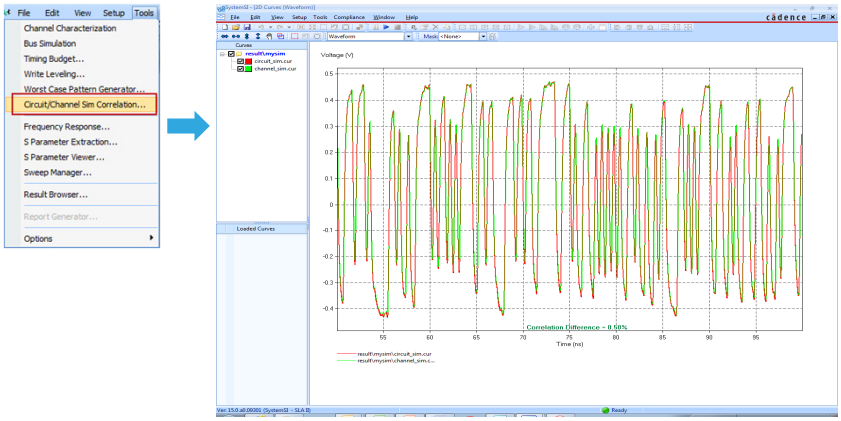
Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated

cadence

Validation 4: Real Channel follows

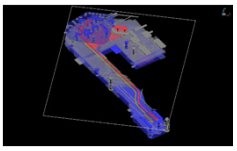
1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

- First of all, check if your system/channel to be analyzed can be treated as LTI or not:

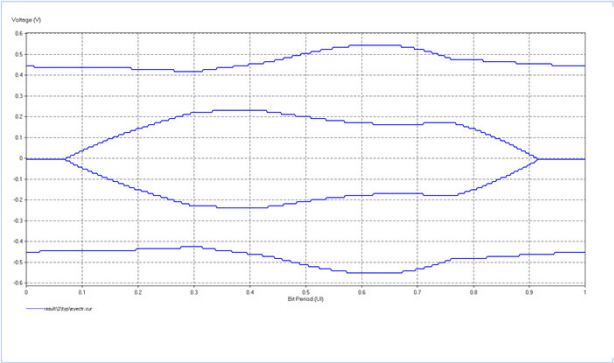


cadence

Validation 4: Real Channel follows



1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**



Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated

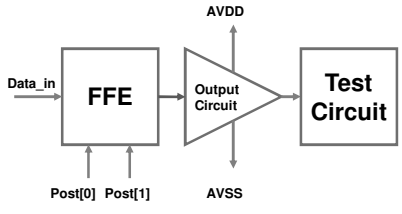
cadence

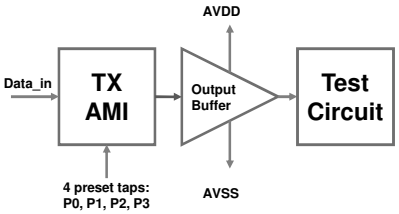
Agenda

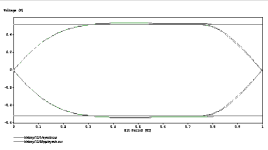
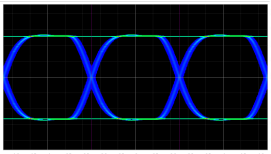
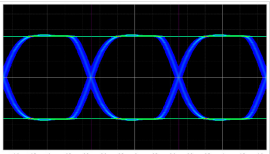
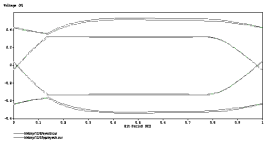
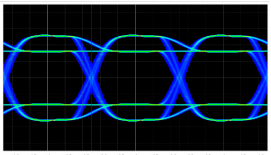
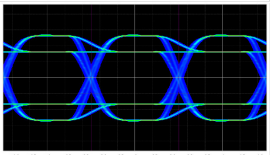
- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. USB 3.0 TX – An Output Buffer + FFE
  2. USB 3.0 RX – An Input Buffer + AGC + CTE
  3. A System – USB 3.0 TX + Channel (PCB+Conn+3m Cable) + USB 3.0 RX
- Conclusion

cadence

USB 3.0 TX

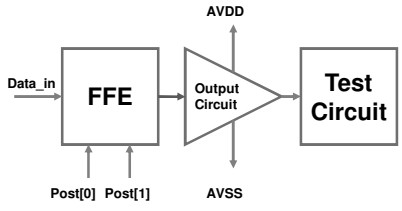


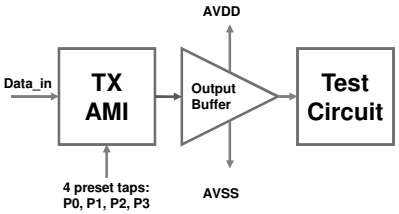


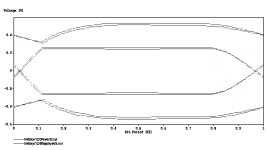
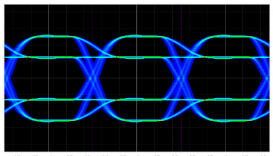
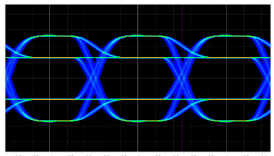
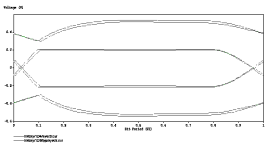
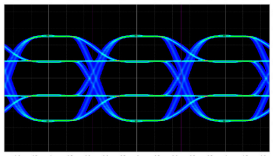
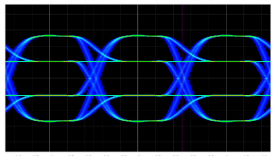
	Eye Contour	Distribution Eye – Circuit Netlist	Distribution Eye – IBIS+AMI model
0dB			
3dB			

cadence

USB 3.0 TX



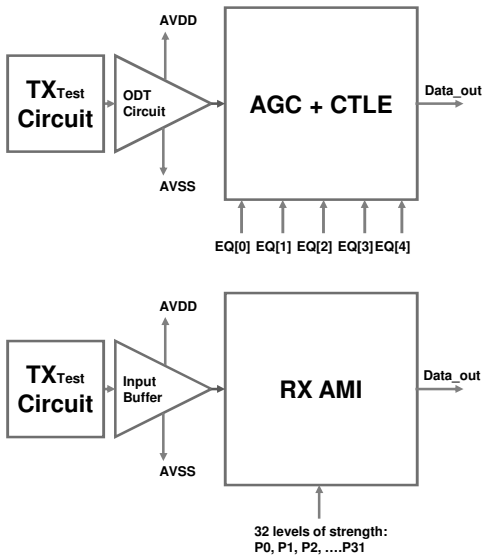


	Eye Contour	Distribution Eye – Circuit Netlist	Distribution Eye – IBIS+AMI model
6dB			
8dB			

cadence

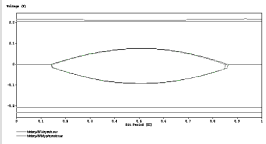
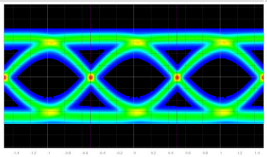
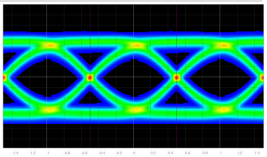
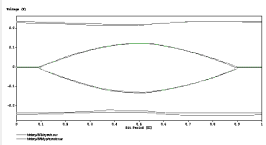
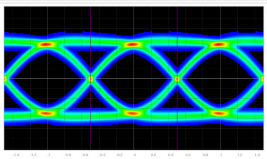
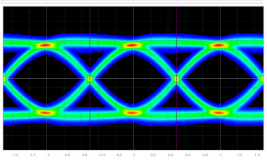
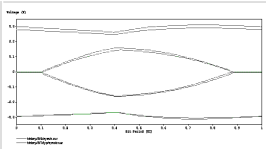
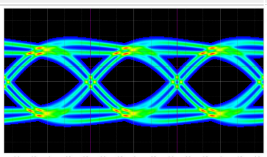
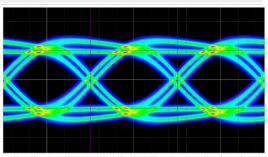
15 .

USB 3.0 RX



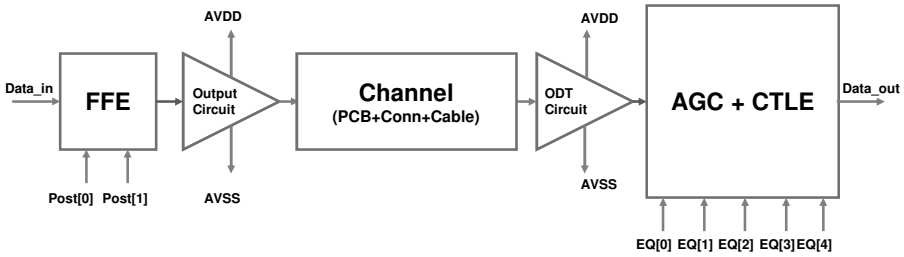
cadence

USB 3.0 RX

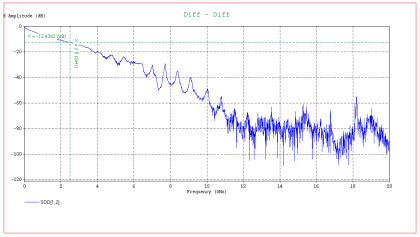
	Eye Contour	Distribution Eye – Circuit Netlist	Distribution Eye – IBIS+AMI model
00100			
00110			
01010			

cadence

A System – USB 3.0 TX + Channel + USB 3.0 RX

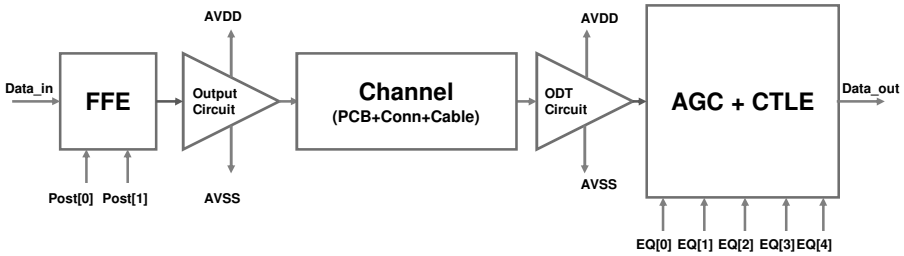


- Channel Insertion Loss

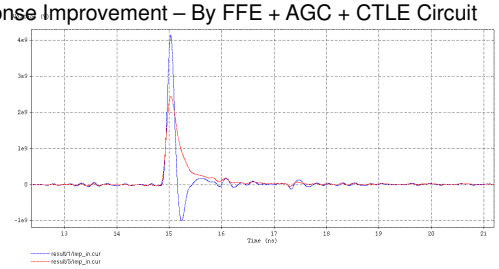


cadence

A System – USB 3.0 TX + Channel + USB 3.0 RX

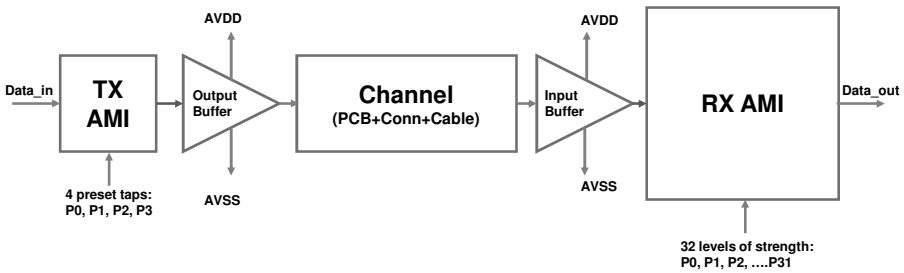


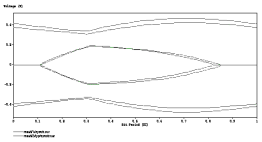
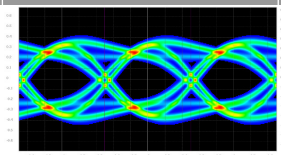
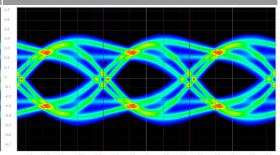
- Impulse Response Improvement – By FFE + AGC + CTLE Circuit



cadence

A System –
USB 3.0 TX + Channel + USB 3.0 RX



	Eye Contour	Distribution Eye – Circuit Netlist	Distribution Eye – IBIS+AMI model
TX=3dB RX= 00110			

cadence

Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
  2. RX – An Input Buffer + AGC + CTE
  - A System – USB 3.0 TX + Channel + RX
- Conclusion

cadence

Conclusion

- An accurate IBIS+AMI model could be an alternative approach to validate your “system” design versus a transistor netlist model
- An accurate IBIS-AMI model consists of two parts – an **accurate IBIS model** and **an accurate AMI model** – **validation** is the key
- An accurate IBIS should be generated by a tool which can well describe a **truly differential pair** in all V/I, V/T and I/T curves.
- An accurate AMI model should be generated by a tool with a rich library such that the generation tool can use all available means in the library to describe all your possible designs.
- A simulation environment which supports transistor netlist models is fundamental for IBIS+AMI model generation/validation.

cadence

cadence®

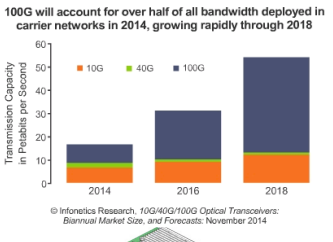
Suggestion on Issuing VSR/CAUI-4 Based IBIS-AMI Model

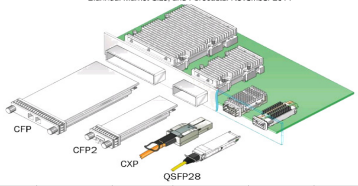
Asian IBIS Summit (Shanghai), November 11, 2016
Zhengrong Xu, Huawei Technologies

www.huawei.com

HUAWEI TECHNOLOGIES CO., LTD.

Industry Trend: Optical Module with CDR Inside Becomes a Standard Beyond 25Gbps/lane



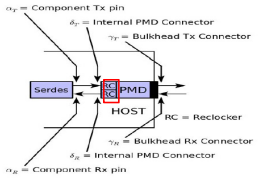


MODULE	CXP	QSFP28	CFP	CFP2	CFP4	CPAK
Line Rates	12x12G or 10x12G	4x 25-28G	40/100G (4*25G)	40/100G (4*25G)	40/100G (4*25G)	40/100G (4*25G)

FIBRE CHANNEL
Physical Interface-6
REV 3.10

OIF OPTICAL INTERNETWORKING FORUM

IEEE



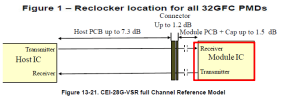
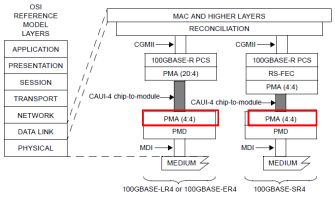


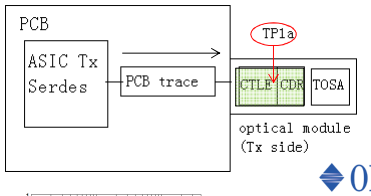
Figure 13-21. CEI-28G-VSR full Channel Reference Model



Electrical interface between chip and module becomes a SerDes to SerDes connection.

Electrical Interface Compliance Test Defined in OIF CEI-28G-VSR / IEEE 802.3bm CAUI-4

- TP1a is the test point after CTLE inside CDR device. The real eye diagram at TP1a can't be measured
- A standard "Reference CTLE" and "Golden PLL" model is defined for compliance test instead



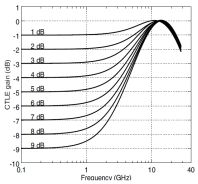


Figure 13-14. Host output Reference receiver equalizer (CTLE) transfer function for gains of 1 dB to 9 dB

Table 13-8. Reference equalizer coefficients for rate of 28 GBd.

Peaking (dB)	G	P1/2π (GHz)	P2/2π (GHz)	Z1/2π (GHz)
1	0.891	18.6	14.1	8.31
2	0.794	18.6	14.1	7.10
3	0.708	15.6	14.1	5.68
4	0.631	15.6	14.1	4.98
5	0.562	15.6	14.1	4.35
6	0.501	15.6	14.1	3.82
7	0.447	15.6	14.1	3.43
8	0.398	15.6	14.1	3.00
9	0.355	15.6	14.1	2.67

$$H(s) = \frac{(G)(P1)(P2)}{Z1} \frac{(S+Z1)}{(S+P1)(S+P2)}$$

Table 13-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage pk-pk	-	900	mV	
Common Mode Noise RMS	-	17.5	mV	See Section 13.3.5
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz See Section 13.3.6
Differential Return Loss (SDD22)	-	See Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)	-	See Equation 13-21	dB	
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to 30 GHz
Transition Time, 20 to 80%	10	-	ps	See Section 13.3.10
Common Mode Voltage	-0.3	2.8	V	Referred to host ground
Eye Width at 10^{-15} probability (EW15)[1]	0.46	-	UI	See Section 13.3.11
Eye Height at 10^{-15} probability (EH15)[1]	95	-	mV	See Section 13.3.11

1. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE)

Note: a reference clock recovery unit (CRU) with a first order transfer function with a 3 dB tracking bandwidth of fb/2578.

Oscilloscope Measurement Solution for TP1a

- Post-process the measurement waveform with software reference CTLE and golden PLL based on formula
- Use the noise and jitter extrapolation to get the EH / EW @ BER=1e-15

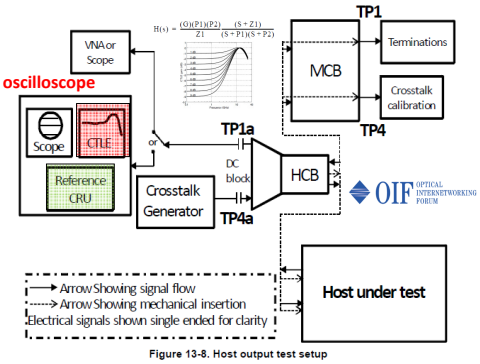
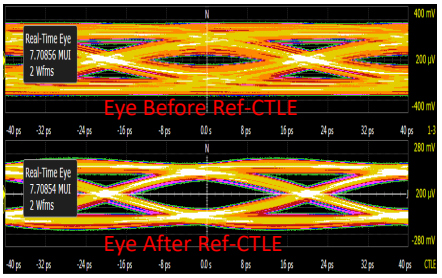
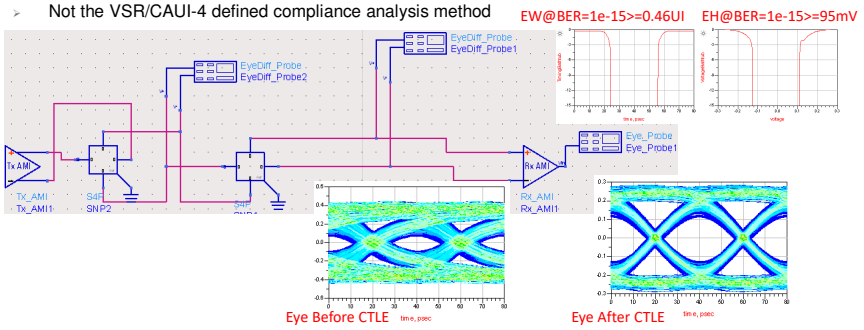


Figure 13-8. Host output test setup



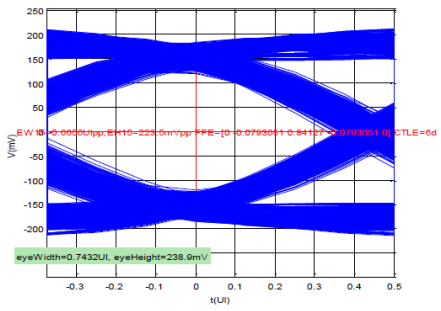
Simulation Solution for TP1a (1): Acquire Certain Module's CDR IBIS-AMI Model

- Advantage:
  - Display real performance of certain optical module's CDR
  - Supported by commercial EDA tools
- Disadvantage:
  - Not all vendors can provide their CDR's IBIS-AMI model
  - Not the VSR/CAUI-4 defined compliance analysis method



Simulation Solution for TP1a (2): Waveform Post-processing Based on VSR/CAUI-4 Spec

- Similar to measurement, current simulation has to be done with self-programmed data post-processing script
- Without reference CTLE IBIS-AMI model, VSR/CAUI-4 electrical interface simulation can't be achieved in EDA tools



Suggest IBIS Organization Issue the IBIS-AMI Model of Standard Reference CTLE for Customers

- Suggest IBIS Organization issue the standard VSR/CAUI-4 compliant IBIS-AMI model including reference CTLE and golden PLL
  - As reference CTLE is a definite formula and fully meets LTI system, it's not difficult to generate such a standard model

OIF OPTICAL INTERNETWORKING FORUM

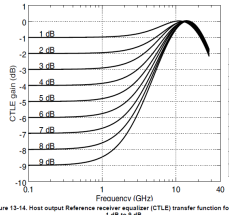
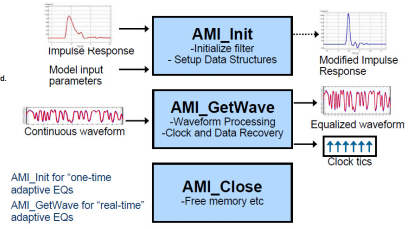


Figure 13-14. Host output Reference receiver equalizer (CTLE) transfer function for gains of 1 dB to 9 dB

$$H(s) = \frac{(G)(P1)(P2)}{Z1}\frac{(S+Z1)}{(S+P1)(S+P2)}$$

Table 13-8. Reference equalizer coefficients for rate of 28 GBd.

Peaking (dB)	G	P1/2π (GHz)	P2/2π (GHz)	Z1/2π (GHz)
1	0.891	18.6	14.1	8.31
2	0.794	18.6	14.1	7.10
3	0.708	15.6	14.1	5.68
4	0.631	15.6	14.1	4.98
5	0.562	15.6	14.1	4.35
6	0.501	15.6	14.1	3.82
7	0.447	15.6	14.1	3.43
8	0.398	15.6	14.1	3.00
9	0.355	15.6	14.1	2.67



Further Discussion

- The issue of the VSR/CAUI-4 based IBIS-AMI model may provide a way for optical CDR vendor to do the correlation between their setting and MSA EQ setting
  - Although MSA defined the unified I2C EQ setting, different optical module vendor uses different CDR and different CTLE, which may have different mapping relationship between MSA EQ and CDR's CTLE.
  - Without a unified correlation method, how to keep the reliability that passing the reference CTLE test of TP1a can pass the error test

SFF Committee

SFF-8636

Specification for

Management Interface for Cabled Environments

TABLE 6-34 INPUT EQUALIZATION (PAGE 03H BYTES 234-235)

Value	Transmitter Input Equalization	
	Nominal	Units
11xxb	Reserved	
1011b	Reserved	
1010b	10	dB
1001b	9	dB
1000b	8	dB
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2	dB
0001b	1	dB
0000b	0	No EQ

- CTLE non-linearity feature should be considered in future
  - Currently formula-based model without considering the non-linearity

Thank you

www.huawei.com

Asian IBIS Summit
Shanghai, China
November 11, 2016

Necessity for integrating FEC functionality for PAM4 in AMI simulations

Xiaoqing Dong (dongxiaoqing82@huawei.com), Huawei Technologies
Chunxing Huang (nickhuang168@163.com), Shenzhen Zhongzeling Electronics

HUAWEI TECHNOLOGIES CO., LTD.

HUAWEI

Agenda

- Review of AMI simulation methodology
- FEC simulation introduction for PAM4 link
- Summary and suggestion

General AMI simulation methodology

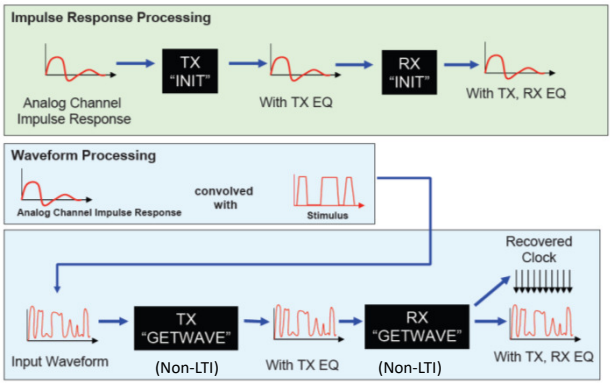
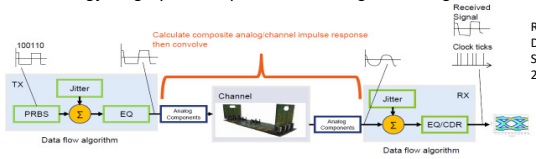


Figure cited from IBIS summit proposal archive

- TX FFE, RX linear equalization is processed in *AMI_Init* function;
- RX CDR, DFE are mostly modeled in *AMI_GetWave* function;
- Converged equalization parameters can be output using *AMI_parameters_out;*
- BER targets are set by users to monitor link qualities.

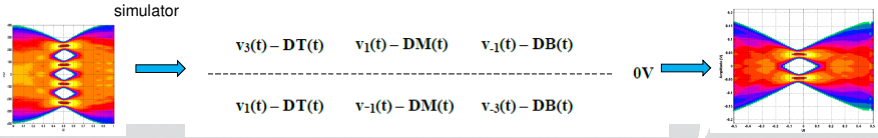
PAM4 simulations in AMI

- AMI defines SerDes behavioral modeling interface and an efficient channel simulation methodology. A graphical representation is given in Figure below.



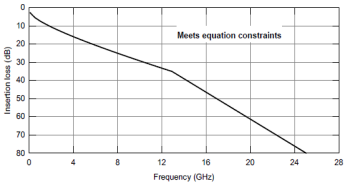
Reference: Hongtao Zhang , Fangyi Rao, Xiaoqing Dong, Geoff Zhang, IBIS-AMI Modeling and Simulation of 56G PAM4 Link Systems, Designcon 2015

- Minimum modifications are proposed in order for the current AMI model to handle PAM4 signal simulations:
  - It is proposed that {0.5V, 0.5/3V, -0.5/3V, -0.5V} are used to represent the 4 levels in PAM4, {3, 1, -1 and -3}.
  - It is proposed to add RX slicer levels to the reserved parameter list in *AMI_GetWave* with Usage Out.
  - It is proposed that a merged NRZ-equivalent eye can be formulated through post processing in a simulator



The industry existing/emerging PAM4 standards

- 28G generation: IEEE-802.3bj-KR4



1.4.53b 100GBASE-KR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding, Clause 91 RS-FEC, and 2-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 35 dB at 12.9 GHz. (See IEEE Std 802.3, Clause 93.)

The receive path of the RS-FEC sublayer may have the option to perform error detection without correction to reduce the data delay (see 91.5.3.3). When the receive path of the RS-FEC sublayer performs error correction, the link is required to operate with a BER of 10^{-5} or better. When the RS-FEC sublayer is configured to bypass error correction, the link is required to operate with a BER of 10^{-12} or better. In this

FEC is mandatory in major PAM4 standards to assure basic link BER target!

- 56G generation: OIF-CEI-56G

A raw BER better than or equal to 1E-4 is required per lane. A compliant receiver, when receiving from a compliant transmitter over a compliant channel, shall deliver the specified raw BER to the subsequent FEC decoder, including burst errors. The burst error length delivered to the PAM4 decoder having more than 65 PAM4 symbol errors shall have a probability of less than 1E-20. (see, 18.A Appendix -, 18.B Appendix -)

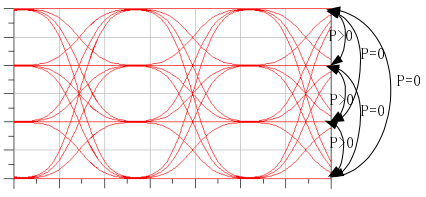
- Emerging commercial simulators support BER simulations up to no better than 1e-5 or 1e-4 for PAM4, according to industry standards. This works for NRZ, but considering FEC has become crucial to enable basic link performance for PAM4, and error propagation of different SerDes makes different error distribution features in an actual link, it is suggested that FEC functionalities be integrated in AMI for PAM4.

PAM4 vs. NRZ: error propagation mechanism

- Given span-symbol error has very low occurrence probability, symbol error is assumed to occur across adjacent levels in PAM4. This approach simplifies the calculation of erroneous voltages, and makes an uniform calculation procedure of PAM4 and NRZ.
- For PAM4, errors only occur between (1,1/3), (1/3,-1/3) and (-1/3,-1). The scaling factor for erroneous voltage offset is 2/3 x DFE coefficients.
- $1+Z^{-1}$ coding scheme can't solve the error propagation issue introduced from DFE.

	Linear	Gray
11		10
10		11
01		01
00		00

Binary bits to PAM4 mapping

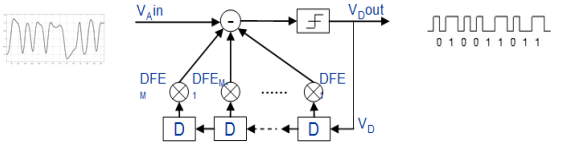


FEC simulation methodologies

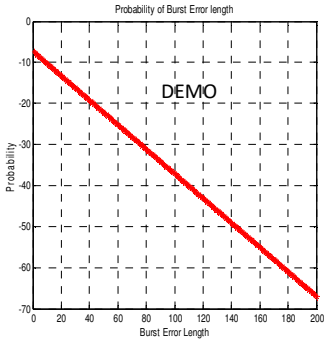
- There are multiple approaches to enable FEC simulation in industry. The one we implemented, is based on burst error probability calculation, where burst error length is set to be long enough to assure calculation accuracy, given converged DFE coefficients and error propagation probabilities.

$$BER = \sum_{i=1}^{rll_{max}} \sum_{all\,E} p(rll = i, E) \cdot W(E) \cdot p_1 \cdot (1 - p_1)^{n - rll_{max} - i}$$

- p_1: random error probability
- i: the probability that i bits in error among a n bit block
- E: all the combinations of the error pattern when error propagation length is i
- rll_{max}: maximum error propagation length

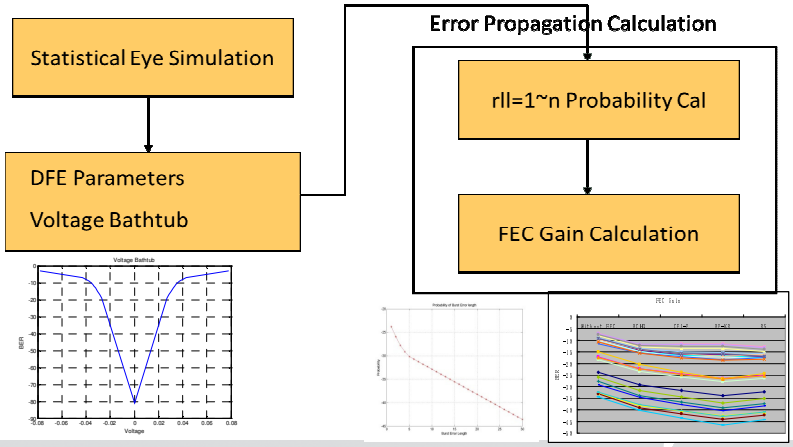


$$V_D out(t_0) = V_A in(t_0) - DFE_1 \cdot V_D(t_{-1}) - DFE_2 \cdot V_D(t_{-2}) - \ldots - DFE_M \cdot V_D(t_{-M})$$



FEC simulation methodologies – cont'd

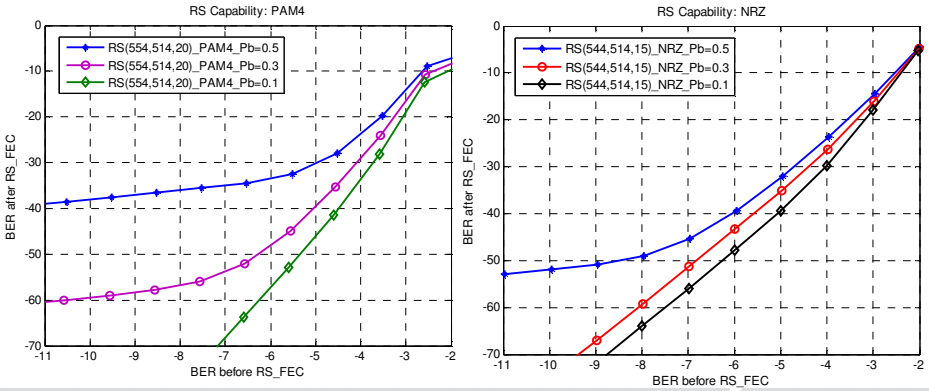
- The proposed methodology supports one-tap DFE error propagation simulation that is routinely used in standards, it also supports multi-tap DFE, multi-type RS codes simulation scenarios, which are more practical for engineering applications.



System simulation case study: PAM4 vs. NRZ

Simulation condition:

- One-tap DFE model adopted;
- One symbol error causes error propagation spanning two-bit length. RS(544,514) defined in KP4 standard does not gain much compared to RS(528,514) in KR4 standard.



System simulation case study: RS solutions

PAM4 link information:

- 29.877dB, ICN=2mV,
- DFE=[0.5;0.0105591419033788;-0.0838646291817282;-0.0411341054292222;-0.0330967146894018;-0.0126712251463267;-0.00584431523805114;-0.00244702521890698;0.00384402448806175;-0.0240163300157797;-0.00748279553106418;0.0522180947613083]];

Performance comparison for different PAM4 RS solutions:

RS Type	RS(544，514)	RS(528，514)	RS(544，504)
BER	6.0e-6	6.0e-6	1.3350e-39
SER after FEC	1.7073e-29	3.7614e-14	1.3350e-39
BER after FEC	5.0247e-31	5.7090e-16	5.1558e-41

Summary

- Conventional AMI simulation does not take into account FEC functionalities.
- Industry standards on PAM4 requires FEC to achieve basic BER targets (1e-12/15 for example), given same/similar channel insertion loss as NRZ systems.
- FEC gain can be modeled using error propagation theories.
  - Burst error length should be long enough to assure calculation accuracy(≥200 bits for RS(544,514) solution)
  - FEC simulation algorithm should support multi-tap DFE, multi-type RS codes simulation scenarios.
- Concept has been proved for feasibility of PAM4 simulation to integrate FEC functionalities through two case studies.
- From system application's perspective, it is recommended that IBIS-AMI to consider integrating FEC simulation functionality for PAM4.

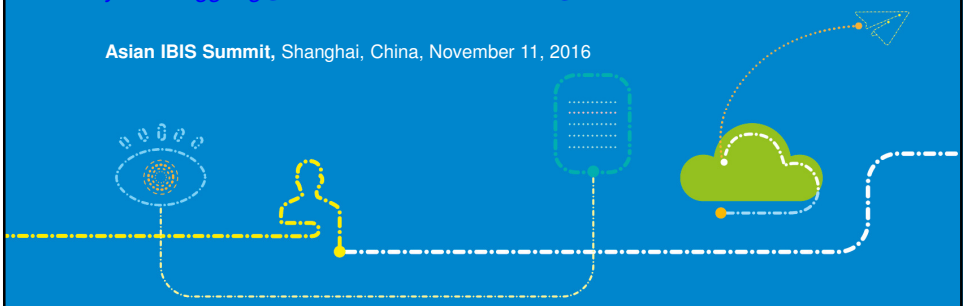
Thank you

ZTE
Tomorrow never waits

The Impact of Channel Performance to 56G PAM4 Systems

Yin Changgang，Zhu Shunlin
yin.changgang@zte.com.cn， zhu.shunlin@zte.com.cn

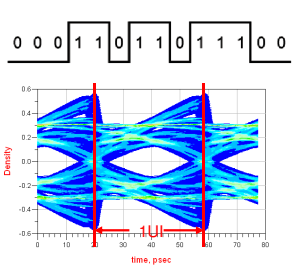
Asian IBIS Summit, Shanghai, China, November 11, 2016



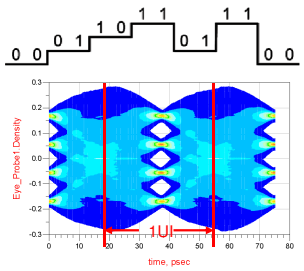
Agenda

- Introduction to PAM4 Modulation
- OIF CEI-56G-LR-PAM4 Specifics
- IBIS-AMI Model Simulation for 56G PAM4 Signals
- The Impact of Channel Characteristics to 56G PAM4 Systems
- Summary

Introduction to PAM4 Modulation



- NRZ(PAM2):
  - ✓ 2 amplitude levels
  - ✓ 1 bit = 1 symbol, one eye in each UI
  - ✓ 56Gbaud for 56 Gbps
    - -Nyquist frequency = 28GHz
  - ✓ BER=1E-15

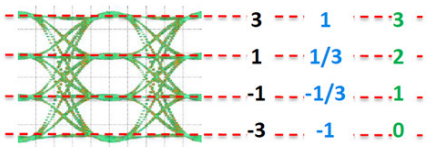


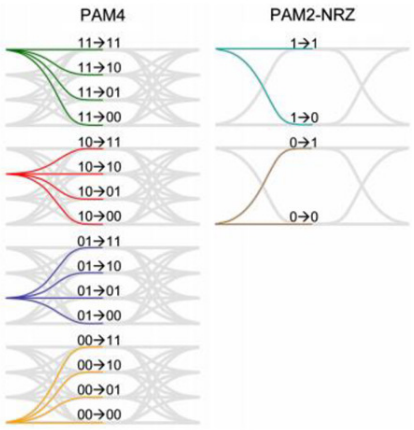
- PAM4:
  - ✓ 4 amplitude levels
  - ✓ 2 bit = 1 symbol, 3 eye in each UI
  - ✓ 28Gbaud for 56 Gbps
    - -Nyquist frequency = 14GHz
  - ✓ BER=1E-15

ZTE

Introduction to PAM4 Modulation

- Transition Density(TD)
  - 16 traces between 2 symbols
  - Average TD=75%
  - For PAM2,TD is 50%
- Three common amplitude level naming patterns





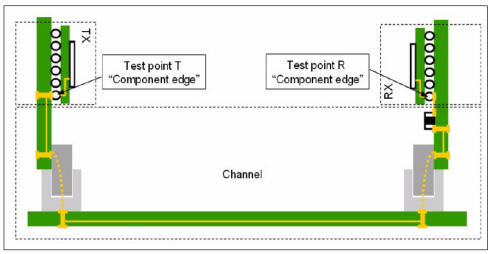
ZTE

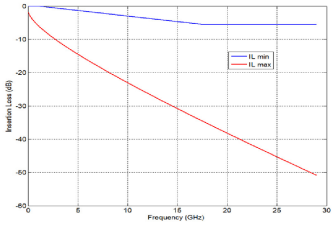
Agenda

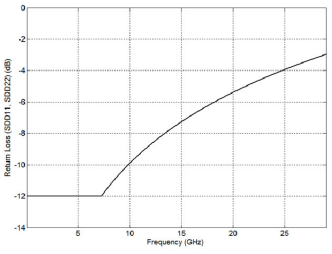
- Introduction to PAM4 Modulation
- OIF CEI-56G-LR-PAM4 Specifics
- IBIS-AMI Model Simulation for 56G PAM4 Signals
- The Impact of Channel Characteristics to 56G PAM4 Systems
- Summary

OIF CEI-56G-LR-PAM4 Specifics

- OIF-CEI-4.0（drafting）
- This paper based on OIF CEI-56G-LR-PAM4 (contribute number：OIF2014.380.03)







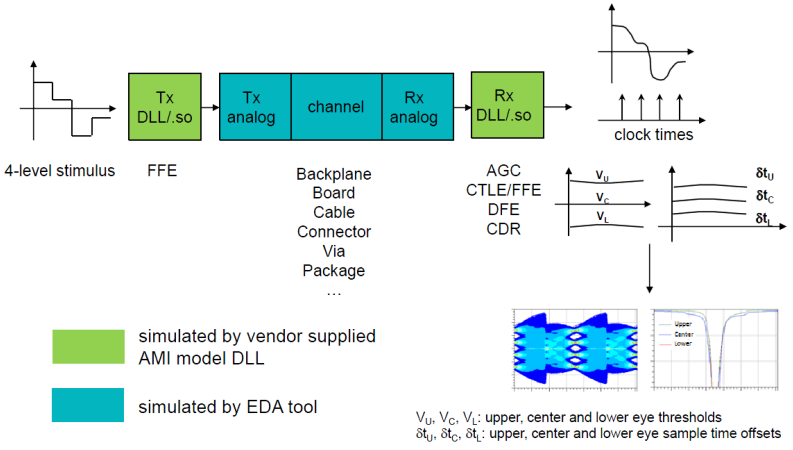
ZTE

Agenda

- Introduction to PAM4 Modulation
- OIF CEI-56G-LR-PAM4 Specifics
- IBIS-AMI Model Simulation for 56G PAM4 Signals
- The Impact of Channel Characteristics to 56G PAM4 Systems
- Summary

IBIS-AMI Model Simulation for 56G PAM4 Signals

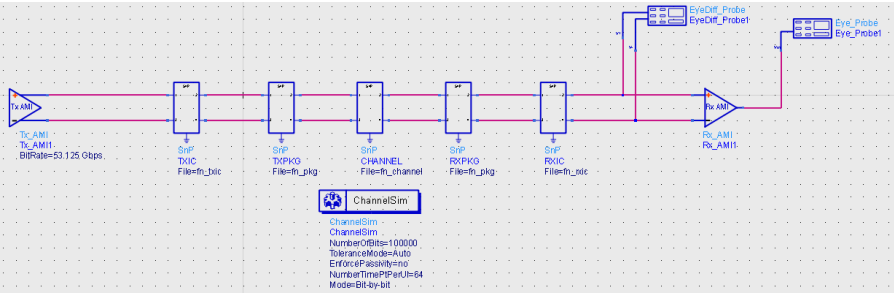
- IBIS-AMI model used for NRZ simulation is widely applied today
- IBIS-AMI model used for PAM4 simulation is still new
- SI engineers are facing new challenges

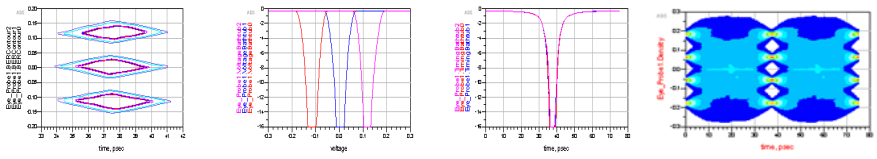


V_U, V_C, V_L: upper, center and lower eye thresholds
δt_U, δt_C, δt_L: upper, center and lower eye sample time offsets

ZTE

IBIS-AMI Model Simulation for 56G PAM4 Signals





BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList2.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList
1.000E-12	0.047	0.046	0.041	4.618E-12	3.963E-12	4.141E-12
1.000E-11	0.050	0.049	0.044	4.694E-12	4.141E-12	4.618E-12
1.000E-10	0.054	0.053	0.048	5.003E-12	4.200E-12	4.694E-12
1.000E-9	0.071	0.071	0.069	6.008E-12	5.468E-12	6.008E-12
1.000E-8	0.077	0.076	0.075	7.153E-12	6.008E-12	7.341E-12

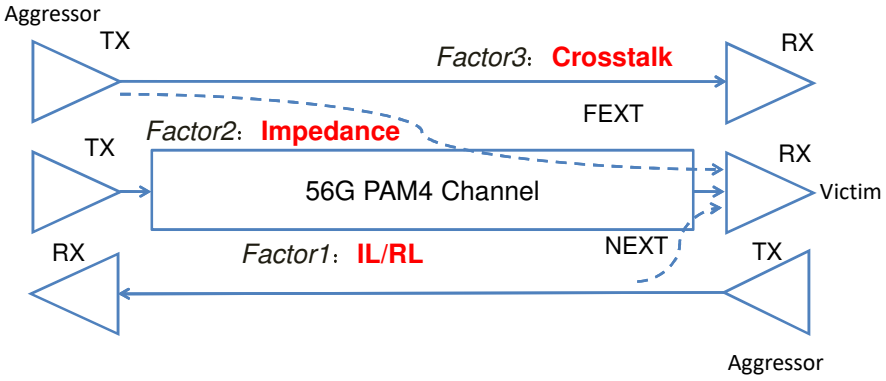
ZTE

Agenda

- Introduction to PAM4 Modulation
- OIF CEI-56G-LR-PAM4 Specifics
- IBIS-AMI Model Simulation for 56G PAM4 Signals
- The Impact of Channel Characteristics to 56G PAM4 Systems
- Summary

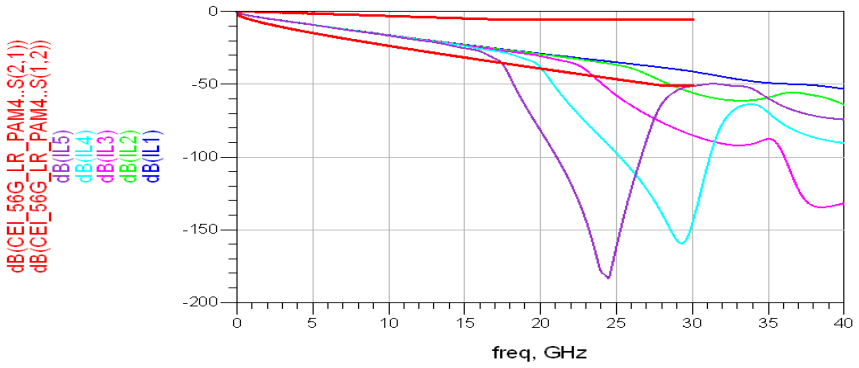
The Impact of Channel Characteristics

➢ 56G-PAM4 systems performance depends on the channel characteristics including IL/RL, crosstalk, impedance, etc.



ZTE

The Impact of Resonance Frequency of Insertion Loss

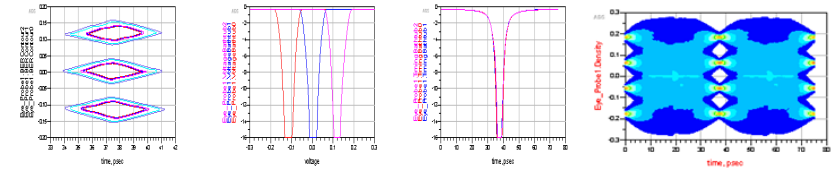


	case1	case2	case3	case4	case5
Resonance f/GHz	98	49	32	29	24

ZTE

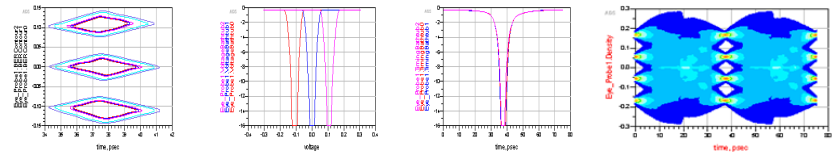
Case Simulations for Different Resonance Frequencies

- Case1



BER	BERHeightList0 Eye_Probe1 HeightAtBERList	BERHeightList1 Eye_Probe1 HeightAtBERList	BERHeightList2 Eye_Probe1 HeightAtBERList	BERWidthList0 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList	BERWidthList2 Eye_Probe1 WidthAtBERList
1.0000E-12	0.047	0.046	0.041	4.5085E-12	3.9053E-12	4.1461E-12
1.0000E-11	0.050	0.049	0.044	4.8946E-12	4.1461E-12	4.5116E-12
1.0000E-10	0.054	0.053	0.048	5.0853E-12	4.5116E-12	4.8946E-12
1.0000E-9	0.071	0.071	0.069	6.5085E-12	6.4085E-12	6.5085E-12
1.0000E-8	0.077	0.079	0.075	7.3461E-12	7.7085E-12	7.3461E-12

- Case2

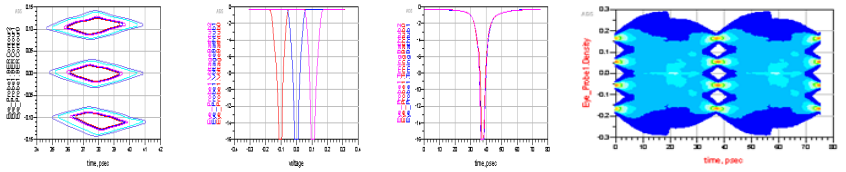


BER	BERHeightList0 Eye_Probe1 HeightAtBERList	BERHeightList1 Eye_Probe1 HeightAtBERList	BERHeightList2 Eye_Probe1 HeightAtBERList	BERWidthList0 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList	BERWidthList2 Eye_Probe1 WidthAtBERList
1.0000E-12	0.041	0.040	0.037	4.1461E-12	3.5078E-12	4.1461E-12
1.0000E-11	0.043	0.043	0.040	4.3216E-12	3.9053E-12	4.5116E-12
1.0000E-10	0.046	0.045	0.043	4.7085E-12	4.2238E-12	4.8946E-12
1.0000E-9	0.062	0.062	0.060	6.4085E-12	6.0246E-12	6.4085E-12
1.0000E-8	0.068	0.067	0.069	7.1635E-12	6.7785E-12	7.1635E-12

ZTE

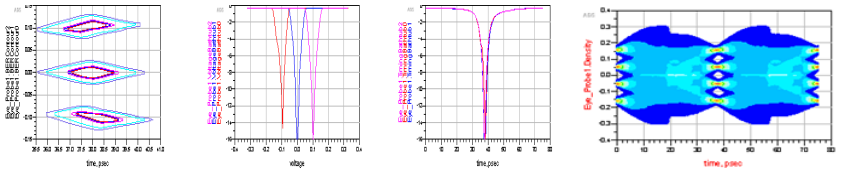
Case Simulations for Different Resonance Frequencies

- Case3



BER	BERHeightList0 Eye_Probe1 HeightAtBERList	BERHeightList1 Eye_Probe1 HeightAtBERList	BERHeightList2 Eye_Probe1 HeightAtBERList	BERWidthList0 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList	BERWidthList2 Eye_Probe1 WidthAtBERList
1.0000E-12	0.030	0.032	0.033	2.3065E-12	2.5078E-12	3.3868E-13
1.0000E-11	0.034	0.036	0.036	3.5078E-12	3.7085E-12	3.3868E-13
1.0000E-10	0.039	0.039	0.040	3.9053E-12	4.1461E-12	3.7085E-12
1.0000E-9	0.059	0.059	0.059	5.9461E-12	6.0461E-12	5.9461E-13
1.0000E-8	0.065	0.065	0.065	6.7085E-12	6.4085E-12	6.7215E-12

- Case4

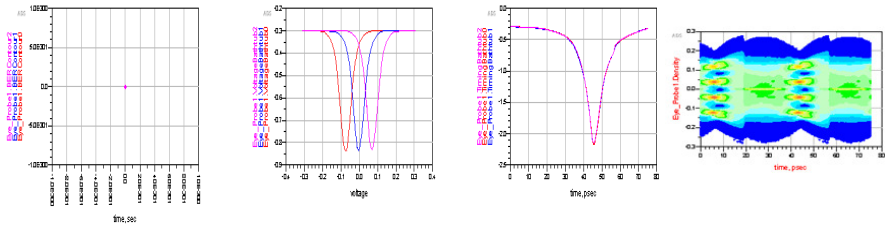


BER	BERHeightList0 Eye_Probe1 HeightAtBERList	BERHeightList1 Eye_Probe1 HeightAtBERList	BERHeightList2 Eye_Probe1 HeightAtBERList	BERWidthList0 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList	BERWidthList2 Eye_Probe1 WidthAtBERList
1.0000E-12	0.019	0.023	0.019	2.0715E-12	1.9053E-12	2.0715E-12
1.0000E-11	0.019	0.027	0.019	2.0715E-12	2.2096E-12	2.2096E-12
1.0000E-10	0.023	0.030	0.023	2.4475E-12	2.4475E-12	2.4475E-12
1.0000E-9	0.040	0.040	0.040	4.1461E-12	4.2238E-12	4.1461E-12
1.0000E-8	0.059	0.063	0.063	4.8946E-12	4.7085E-12	4.8946E-12

ZTE

Case Simulations for Different Resonance Frequencies

- Case5

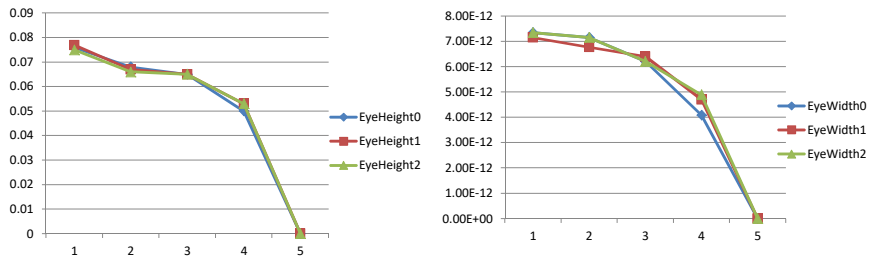


BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList2.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList
1.000E-12	-0.617	-0.607	-0.607	0.000	0.000	0.000
1.000E-11	-0.617	-0.607	-0.607	0.000	0.000	0.000
1.000E-10	-0.617	-0.607	-0.607	0.000	0.000	0.000
1.000E-9	-0.617	-0.607	-0.607	0.000	0.000	0.000
1.000E-8	-0.617	-0.607	-0.607	0.000	0.000	0.000

ZTE

Factor Analysis for Resonance Frequency of Insertion Loss

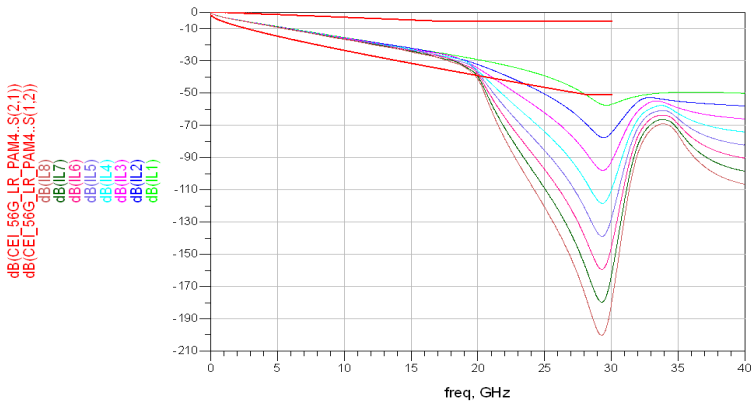
- The resonance frequency affect all the three EyeHeights and EyeWidths
  - -The more close to the Nyquist frequency , the eye getting worse until completely closed
- The resonance frequency should be more than 29GHz in our cases



@BER=1E-5

ZTE

The Impact of Resonance Depth of Insertion Loss

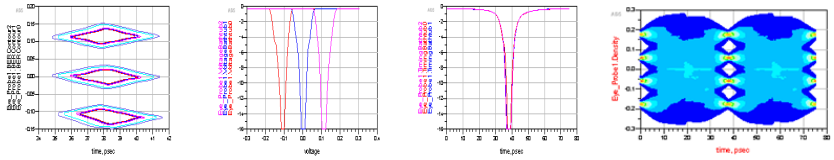


@29.4GHz/dB	case1	case2	case3	case4	case5	case6	case7	case8
Resonance depth	57	78	98	118	139	159	180	200

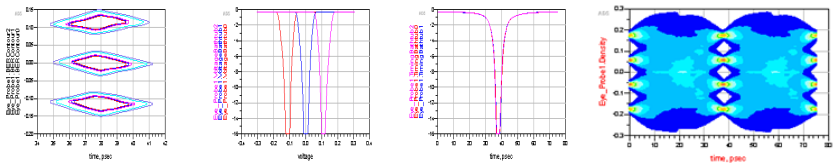
ZTE

Case Simulations for Different Resonance Depths

- Case1



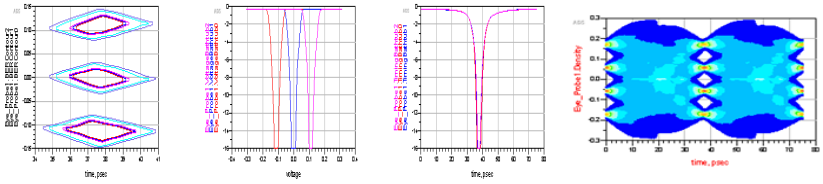
- Case2



ZTE

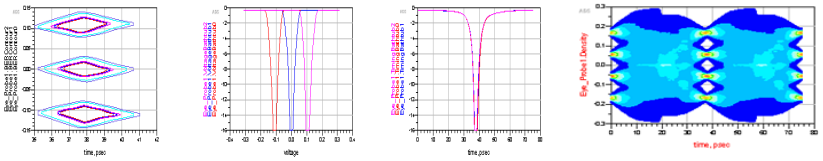
Case Simulations for Different Resonance Depths

- Case3



BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList2.Eye_Probe1.WidthAtBERList
1.000E-12	0.036	0.036	0.033	3.982E-12	2.824E-12	3.012E-12
1.000E-11	0.038	0.038	0.036	4.141E-12	3.220E-12	3.369E-12
1.000E-10	0.042	0.041	0.038	4.230E-12	3.479E-12	3.573E-12
1.000E-09	0.060	0.058	0.056	6.024E-12	5.464E-12	5.493E-12
1.000E-08	0.067	0.066	0.064	6.566E-12	6.024E-12	6.217E-12

- Case4

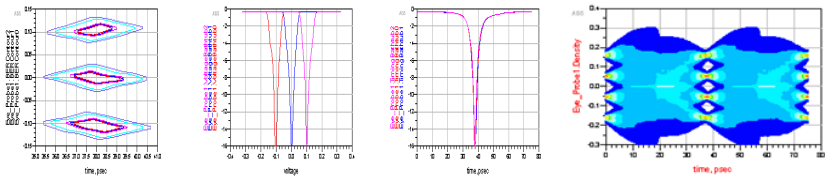


BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList2.Eye_Probe1.WidthAtBERList
1.000E-12	0.037	0.033	0.034	3.206E-12	3.012E-12	2.835E-12
1.000E-11	0.041	0.039	0.036	3.676E-12	3.220E-12	3.012E-12
1.000E-10	0.044	0.039	0.039	3.795E-12	3.479E-12	3.369E-12
1.000E-09	0.060	0.059	0.056	5.493E-12	5.464E-12	4.894E-12
1.000E-08	0.066	0.063	0.063	6.024E-12	6.024E-12	6.047E-12

ZTE

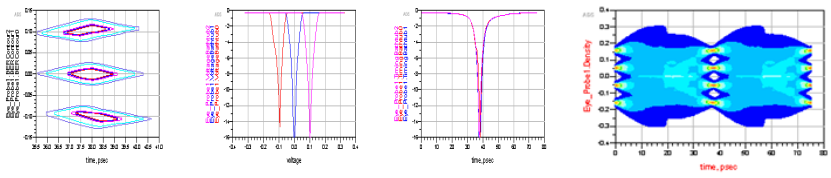
Case Simulations for Different Resonance Depths

- Case5



BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList2.Eye_Probe1.WidthAtBERList
1.000E-12	0.021	0.019	0.019	2.447E-12	1.802E-12	2.447E-
1.000E-11	0.024	0.024	0.023	2.824E-12	1.802E-12	2.835E-
1.000E-10	0.027	0.027	0.026	3.206E-12	2.206E-12	3.024E-
1.000E-09	0.047	0.051	0.046	4.230E-12	4.141E-12	4.706E-
1.000E-08	0.058	0.059	0.054	5.493E-12	4.894E-12	5.271E-

- Case6

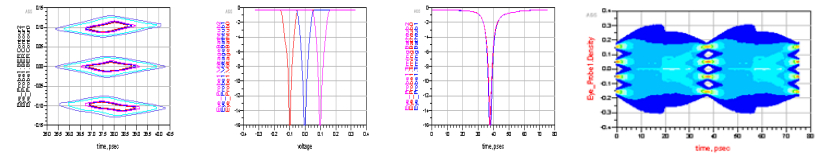


BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList2.Eye_Probe1.WidthAtBERList
1.000E-12	0.019	0.020	0.019	2.071E-12	1.802E-12	2.071E-12
1.000E-11	0.019	0.027	0.019	2.071E-12	2.206E-12	2.206E-12
1.000E-10	0.023	0.030	0.022	2.447E-12	2.442E-12	2.447E-12
1.000E-09	0.041	0.047	0.040	4.141E-12	4.230E-12	4.141E-12
1.000E-08	0.059	0.063	0.053	4.894E-12	4.706E-12	4.894E-12

ZTE

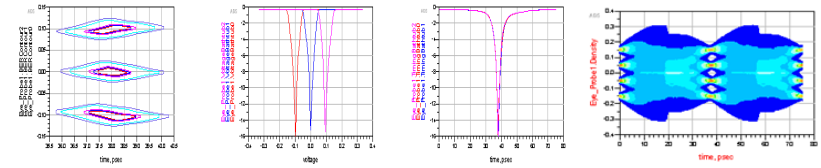
Case Simulations for Different Resonance Depths

- Case7



BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList2.Eye_Probe1.WidthAtBERList
1.000E-12	0.016	0.021	0.019	2.209E-12	1.882E-12	2.071E-12
1.000E-11	0.017	0.025	0.023	2.209E-12	2.209E-12	2.447E-12
1.000E-10	0.020	0.028	0.027	2.603E-12	2.447E-12	2.824E-12
1.000E-09	0.042	0.047	0.046	4.324E-12	4.229E-12	4.229E-12
1.000E-08	0.061	0.064	0.061	4.804E-12	4.804E-12	5.081E-12

- Case8

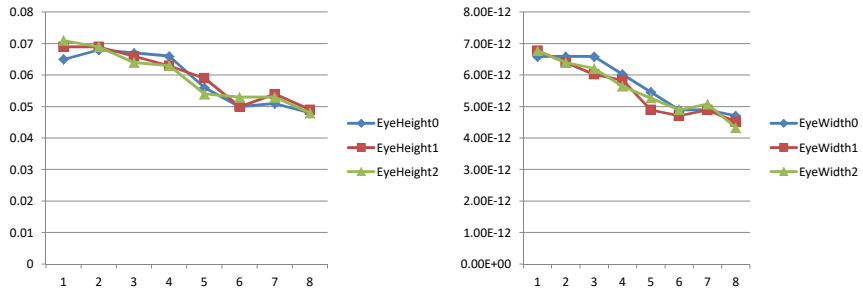


BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList2.Eye_Probe1.WidthAtBERList
1.000E-12	0.014	0.016	0.013	1.507E-12	1.694E-12	1.319E-12
1.000E-11	0.016	0.018	0.017	2.071E-12	1.882E-12	1.694E-12
1.000E-10	0.022	0.022	0.021	2.447E-12	2.259E-12	1.882E-12
1.000E-09	0.038	0.041	0.041	4.141E-12	3.776E-12	3.776E-12
1.000E-08	0.048	0.048	0.048	4.700E-12	4.512E-12	4.229E-12

ZTE

Factor Analysis for Resonance Depth of Insertion Loss

- The deeper of the resonance, the eye getting worse
- The depth of the resonance is less impact to the eye diagram than the frequency of the resonance



@BER=1E-5

ZTE

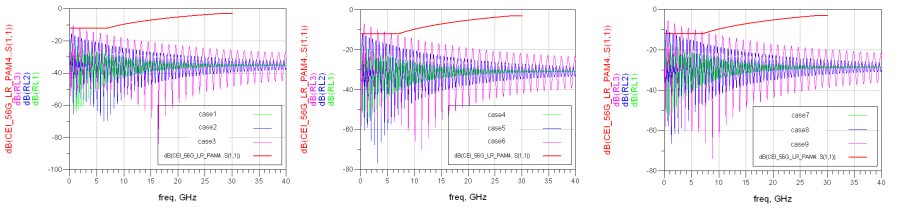
The Impact of Impedance Discontinuity

- Channel length：20in, differential impedance：100ohm

Case1-10in 105ohm +10 in 95ohm
Case2-(5in 105ohm +5 in 95ohm)*2
Case3-(2.5in 105ohm +2.5 in 95ohm) *4

Case4-10in 108ohm +10 in 92ohm
Case5-(5in 108ohm +5 in 92ohm)*2
Case6-(2.5in 108ohm +2.5 in 92ohm) *4

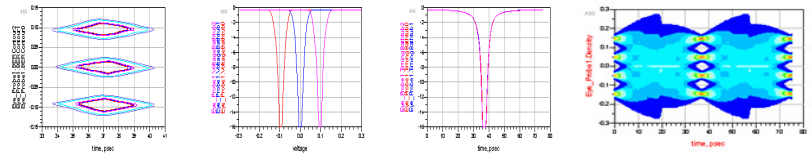
Case7-10in 110ohm +10 in 90ohm
Case8-(5in 110ohm +5 in 90ohm)*2
Case9-(2.5in 110ohm +2.5 in 90ohm) *4



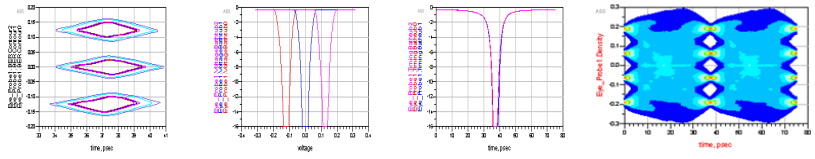
ZTE

Case Simulations for Impedance Discontinuity

- Case1



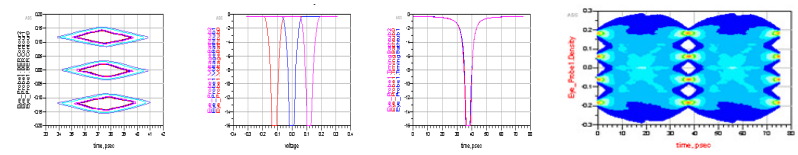
- Case2



ZTE

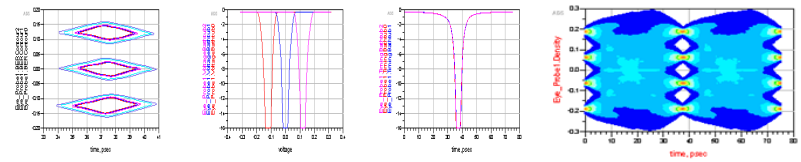
Case Simulations for Impedance Discontinuity

- Case3



BER	BERHeightList0 Eye_Probe1 HeightAtBERList	BERHeightList1 Eye_Probe1 HeightAtBERList	BERHeightList2 Eye_Probe1 HeightAtBERList	BERWidthList0 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList
1.000E-12	0.044	0.045	0.043	4.591E-12	4.329E-12	3.961E-12
1.000E-11	0.047	0.045	0.046	4.591E-12	4.591E-12	4.141E-12
1.000E-10	0.050	0.047	0.050	4.984E-12	4.984E-12	4.511E-12
1.000E-9	0.060	0.053	0.060	6.560E-12	6.560E-12	6.211E-12
1.000E-8	0.071	0.070	0.070	7.741E-12	7.741E-12	8.779E-12

- Case4

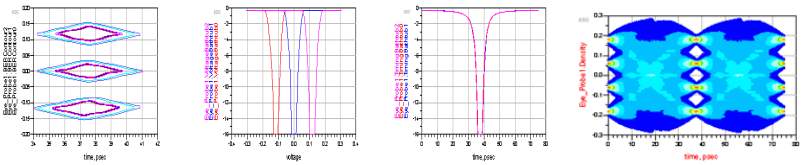


BER	BERHeightList0 Eye_Probe1 HeightAtBERList	BERHeightList1 Eye_Probe1 HeightAtBERList	BERHeightList2 Eye_Probe1 HeightAtBERList	BERWidthList0 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList
1.000E-12	0.049	0.046	0.043	4.330E-12	3.799E-12	3.961E-12
1.000E-11	0.053	0.047	0.048	4.591E-12	4.141E-12	4.141E-12
1.000E-10	0.059	0.053	0.049	4.984E-12	4.511E-12	4.511E-12
1.000E-9	0.071	0.059	0.057	6.560E-12	6.211E-12	6.211E-12
1.000E-8	0.077	0.074	0.074	7.783E-12	8.779E-12	8.965E-12

ZTE

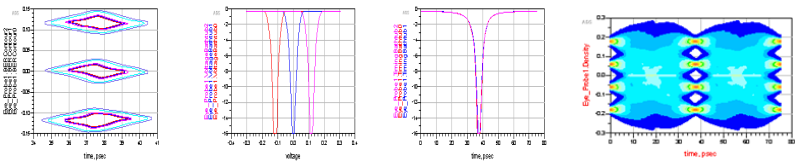
Case Simulations for Impedance Discontinuity

- Case5



BER	BERHeightList0 Eye_Probe1 HeightAtBERList	BERHeightList1 Eye_Probe1 HeightAtBERList	BERHeightList2 Eye_Probe1 HeightAtBERList	BERWidthList0 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList
1.000E-12	0.041	0.039	0.042	4.191E-12	3.799E-12	4.141E-12
1.000E-11	0.044	0.042	0.045	4.511E-12	4.511E-12	4.511E-12
1.000E-10	0.048	0.046	0.048	4.984E-12	4.511E-12	4.511E-12
1.000E-9	0.064	0.057	0.057	6.560E-12	6.560E-12	6.560E-12
1.000E-8	0.070	0.068	0.070	8.965E-12	8.779E-12	8.965E-12

- Case6

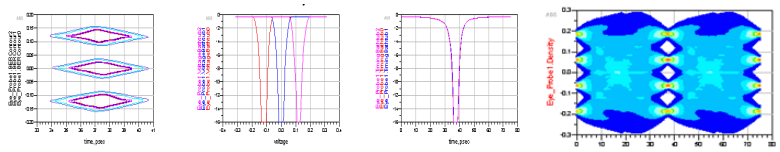


BER	BERHeightList0 Eye_Probe1 HeightAtBERList	BERHeightList1 Eye_Probe1 HeightAtBERList	BERHeightList2 Eye_Probe1 HeightAtBERList	BERWidthList0 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList	BERWidthList1 Eye_Probe1 WidthAtBERList
1.000E-12	0.032	0.027	0.028	3.476E-12	3.610E-12	3.330E-12
1.000E-11	0.035	0.031	0.033	3.803E-12	3.398E-12	3.398E-12
1.000E-10	0.039	0.035	0.036	3.803E-12	3.729E-12	3.729E-12
1.000E-9	0.052	0.043	0.050	5.035E-12	5.460E-12	5.460E-12
1.000E-8	0.057	0.059	0.058	6.460E-12	6.024E-12	6.024E-12

ZTE

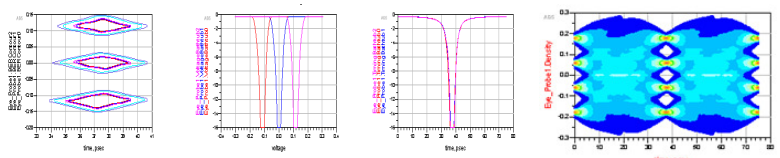
Case Simulations for Impedance Discontinuity

- Case7



BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList
1.000E-12	0.047	0.045	0.044	3.795E-12	4.141E-12	3.951E-12
1.200E-11	0.051	0.048	0.047	4.141E-12	4.226E-12	4.226E-12
1.000E-10	0.054	0.048	0.053	4.015E-12	4.226E-12	4.015E-12
1.000E-9	0.060	0.060	0.064	6.213E-12	6.213E-12	6.024E-12
1.000E-8	0.074	0.071	0.070	6.966E-12	6.966E-12	6.776E-12

- Case8

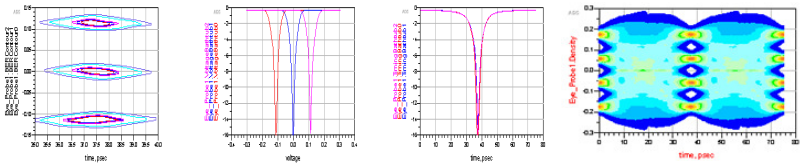


BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList
1.000E-12	0.039	0.034	0.037	4.226E-12	3.679E-12	3.679E-12
1.000E-11	0.043	0.037	0.040	4.141E-12	3.951E-12	3.795E-12
1.000E-10	0.045	0.041	0.044	4.226E-12	4.141E-12	4.141E-12
1.000E-9	0.051	0.050	0.051	6.466E-12	6.213E-12	6.024E-12
1.000E-8	0.067	0.065	0.064	6.966E-12	6.466E-12	6.776E-12

ZTE

Case Simulations for Impedance Discontinuity

- Case9

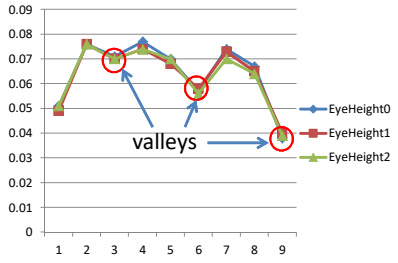


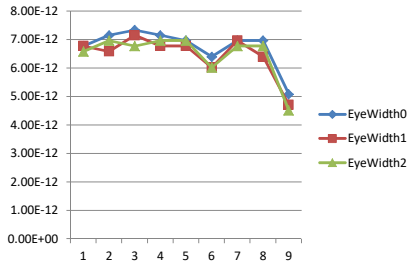
BER	BERHeightList0.Eye_Probe1.HeightAtBERList	BERHeightList1.Eye_Probe1.HeightAtBERList	BERHeightList2.Eye_Probe1.HeightAtBERList	BERWidthList0.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList	BERWidthList1.Eye_Probe1.WidthAtBERList
1.000E-12	0.015	0.013	0.013	1.266E-11	1.319E-12	1.688E-12
1.000E-11	0.017	0.015	0.015	1.467E-12	1.899E-12	1.982E-12
1.000E-10	0.020	0.017	0.017	1.855E-12	2.278E-12	2.321E-12
1.000E-9	0.033	0.033	0.032	4.519E-12	3.963E-12	3.795E-12
1.000E-8	0.038	0.040	0.039	5.802E-12	4.700E-12	4.911E-12

ZTE

Factor Analysis for Impedance Discontinuity

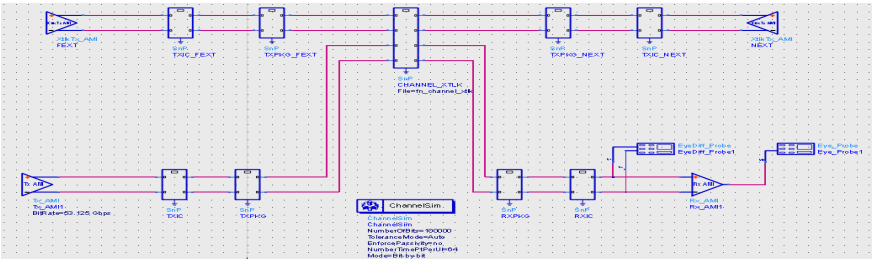
- The diagrams including 3 valleys and the depth is greater in turn
  - The impedance fluctuations of the signal channel affect the EyeHeight more than the EyeWidth
  - Common impedance tolerance +/-10% is not acceptable in the 56G PAM4 systems
  - The impedance tolerance is recommend to be less than or equal to +/-8%
  - Reduce the discontinuity points as possible as you can





@BER=1E-5

The Impact of Channel Crosstalk



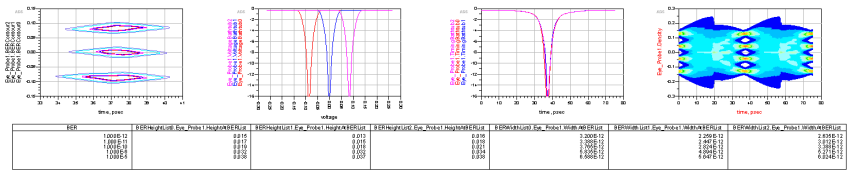
@IL=30dB	case1	case2	case3	case4
ICN/mV	1	2	3	4
XTK=NEXT				

@IL=30dB	case5	case6	case7	case8
ICN/mV	1	2	3	4
XTK=FEXT				

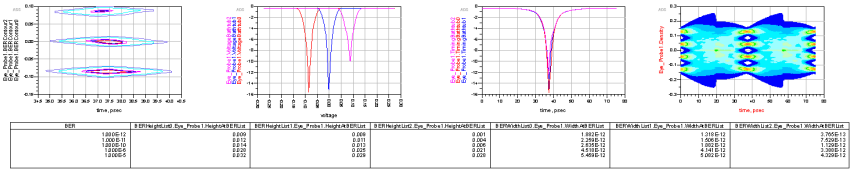
@IL=30dB	case9	case10	case11	case12
ICN/mV	1	2	3	4
XTK=FEXT 50%+NEXT 50%				

Case Simulations for Channel Crosstalk

- Case1



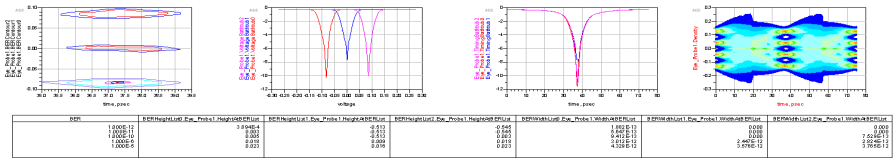
- Case2



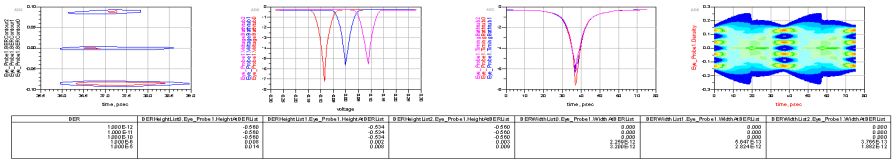
ZTE

Case Simulations for Channel Crosstalk

- Case3



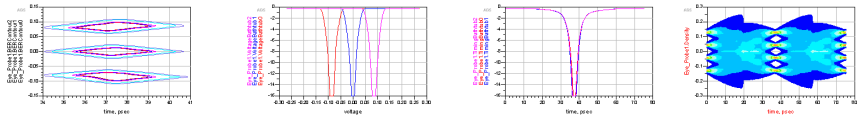
- Case4



ZTE

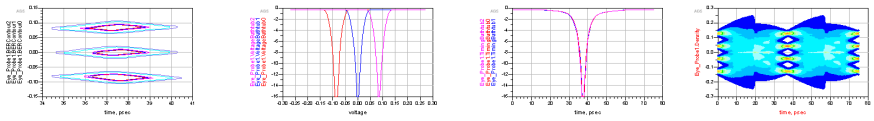
Case Simulations for Channel Crosstalk

- Case5



BER	BERHeightList0:Eye_Probe1.HeightABERList	BERHeightList1:Eye_Probe1.HeightABERList	BERHeightList2:Eye_Probe1.HeightABERList	BERWidthList0:Eye_Probe1.WidthABERList	BERWidthList1:Eye_Probe1.WidthABERList	BERWidthList1:Eye_Probe1.WidthABERList
1.000E-12	0.026	0.023	0.025	3.389E-12	3.389E-12	3.389E-12
1.000E-11	0.027	0.026	0.027	3.765E-12	3.765E-12	3.765E-12
1.000E-10	0.030	0.029	0.030	4.141E-12	4.141E-12	4.141E-12
1.000E-9	0.043	0.043	0.043	6.212E-12	6.024E-12	6.024E-12
1.000E-8	0.047	0.047	0.048	6.965E-12	6.777E-12	6.777E-12

- Case6

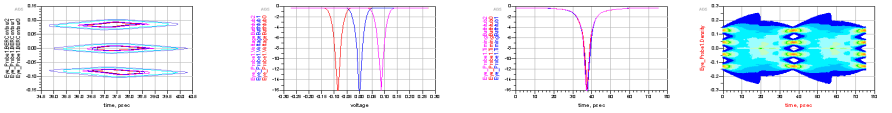


BER	BERHeightList0:Eye_Probe1.HeightABERList	BERHeightList1:Eye_Probe1.HeightABERList	BERHeightList2:Eye_Probe1.HeightABERList	BERWidthList0:Eye_Probe1.WidthABERList	BERWidthList2:Eye_Probe1.WidthABERList	BERWidthList1:Eye_Probe1.WidthABERList
1.000E-12	0.020	0.016	0.017	2.635E-12	2.635E-12	2.259E-12
1.000E-11	0.023	0.018	0.020	3.012E-12	3.012E-12	2.635E-12
1.000E-10	0.024	0.021	0.023	3.389E-12	3.389E-12	2.824E-12
1.000E-9	0.037	0.035	0.037	5.459E-12	5.271E-12	5.082E-12
1.000E-8	0.041	0.041	0.042	6.212E-12	6.024E-12	6.024E-12

ZTE

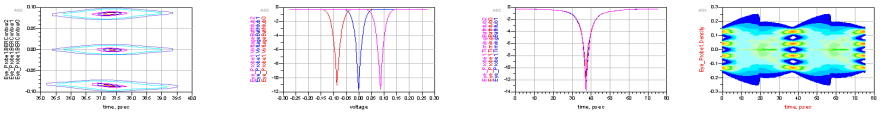
Case Simulations for Channel Crosstalk

- Case7



BER	BERHeightList0:Eye_Probe1.HeightABERList	BERHeightList1:Eye_Probe1.HeightABERList	BERHeightList2:Eye_Probe1.HeightABERList	BERWidthList0:Eye_Probe1.WidthABERList	BERWidthList2:Eye_Probe1.WidthABERList	BERWidthList1:Eye_Probe1.WidthABERList
1.000E-12	0.013	0.015	0.014	2.071E-12	2.259E-12	2.071E-12
1.000E-11	0.016	0.016	0.019	2.824E-12	3.012E-12	2.824E-12
1.000E-10	0.022	0.021	0.022	3.576E-12	3.576E-12	3.576E-12
1.000E-9	0.032	0.031	0.032	5.647E-12	5.271E-12	5.459E-12
1.000E-8	0.036	0.036	0.038			

- Case8

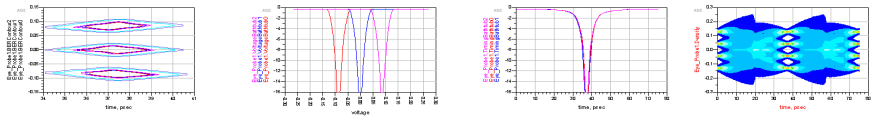


BER	BERHeightList0:Eye_Probe1.HeightABERList	BERHeightList1:Eye_Probe1.HeightABERList	BERHeightList2:Eye_Probe1.HeightABERList	BERWidthList0:Eye_Probe1.WidthABERList	BERWidthList2:Eye_Probe1.WidthABERList	BERWidthList1:Eye_Probe1.WidthABERList
1.000E-12	0.002	0.004	0.005	5.647E-13	5.647E-13	7.155E-13
1.000E-11	0.005	0.007	0.007	9.412E-13	9.412E-13	1.506E-12
1.000E-10	0.008	0.009	0.010	1.318E-12	1.318E-12	1.506E-12
1.000E-9	0.027	0.026	0.026	4.518E-12	4.141E-12	4.141E-12
1.000E-8						

ZTE

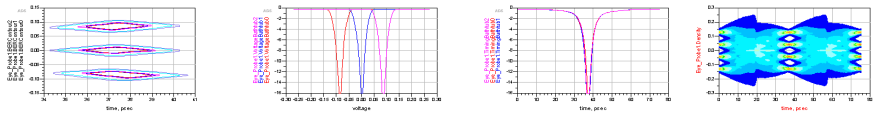
Case Simulations for Channel Crosstalk

- Case9



BER	BERHeightList0:Eye_Probe1.HeightAtBERList	BERHeightList1:Eye_Probe1.HeightAtBERList	BERHeightList2:Eye_Probe1.HeightAtBERList	BERWidthList0:Eye_Probe1.WidthAtBERList	BERWidthList2:Eye_Probe1.WidthAtBERList	BERWidthList1:Eye_Probe1.WidthAtBERList
1.0000E-12	0.023	0.026	0.023	3.0112E-12	1.8248E-12	3.2005E-12
1.0000E-11	0.028	0.029	0.028	1.3908E-12	1.3908E-12	3.0750E-12
1.0000E-10	0.032	0.031	0.032	1.7656E-12	1.7656E-12	3.0953E-12
1.0000E-9	0.042	0.043	0.042	6.0224E-13	8.8558E-13	2.8481E-12
1.0000E-8	0.047	0.048	0.047	6.7766E-13	6.5606E-13	6.5606E-13

- Case10

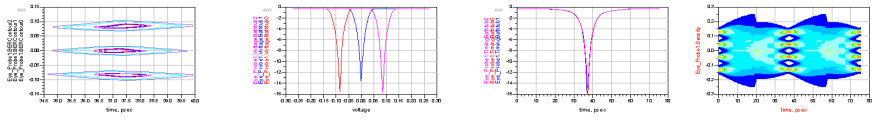


BER	BERHeightList0:Eye_Probe1.HeightAtBERList	BERHeightList1:Eye_Probe1.HeightAtBERList	BERHeightList2:Eye_Probe1.HeightAtBERList	BERWidthList0:Eye_Probe1.WidthAtBERList	BERWidthList2:Eye_Probe1.WidthAtBERList	BERWidthList1:Eye_Probe1.WidthAtBERList
1.0000E-12	0.017	0.019	0.021	3.0126E-12	2.6248E-12	3.0126E-12
1.0000E-11	0.020	0.021	0.024	1.3908E-12	1.3908E-12	2.9858E-12
1.0000E-10	0.026	0.024	0.027	1.8407E-12	2.4658E-12	2.9858E-12
1.0000E-9	0.041	0.042	0.042	6.1402E-13	8.2715E-13	6.2341E-13

ZTE

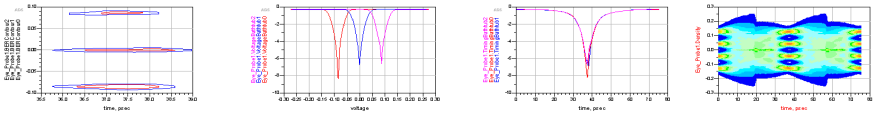
Case Simulations for Channel Crosstalk

- Case11



BER	BERHeightList0:Eye_Probe1.HeightAtBERList	BERHeightList1:Eye_Probe1.HeightAtBERList	BERHeightList2:Eye_Probe1.HeightAtBERList	BERWidthList0:Eye_Probe1.WidthAtBERList	BERWidthList2:Eye_Probe1.WidthAtBERList	BERWidthList1:Eye_Probe1.WidthAtBERList
1.0000E-12	0.009	0.010	0.011	1.9066E-12	1.9066E-12	1.2426E-12
1.0000E-11	0.013	0.014	0.013	1.3908E-12	1.3908E-12	1.0747E-12
1.0000E-10	0.025	0.023	0.030	4.5159E-13	4.5159E-13	4.1481E-12
1.0000E-9	0.032	0.032	0.039	6.4658E-13	8.2715E-13	6.0603E-13

- Case12

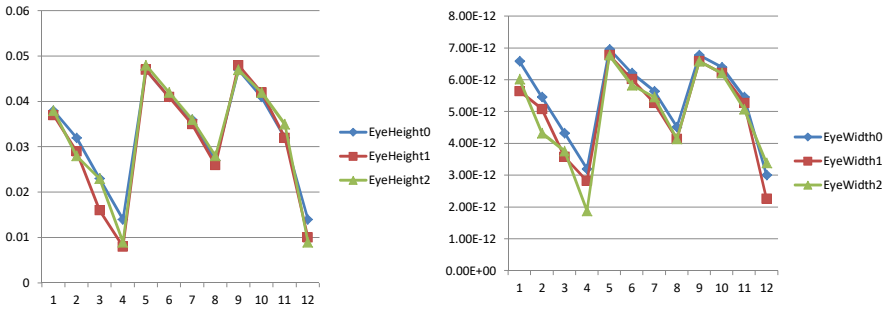


BER	BERHeightList0:Eye_Probe1.HeightAtBERList	BERHeightList1:Eye_Probe1.HeightAtBERList	BERHeightList2:Eye_Probe1.HeightAtBERList	BERWidthList0:Eye_Probe1.WidthAtBERList	BERWidthList2:Eye_Probe1.WidthAtBERList	BERWidthList1:Eye_Probe1.WidthAtBERList
1.0000E-12	-0.544	-0.529	-0.544	0.000	0.000	0.000
1.0000E-11	-0.544	-0.529	-0.544	0.000	0.000	0.000
1.0000E-10	0.000	0.000	0.000	3.0112E-12	1.3908E-12	2.2926E-12
1.0000E-9	0.016	0.016	0.000	3.0112E-12	1.3908E-12	3.3926E-12

ZTE

Factor Analysis for Channel Crosstalk

- NEXT is more influential to the 56G-PAM4 systems than FEXT
- ICN limited:
  - To be less than 4mV for all crosstalk is NEXT
  - To be 4mV is OK for all crosstalk is FEXT
  - To be less than 4mV for half of crosstalk is FEXT and the other half of crosstalk is NEXT



@BER=1E-5

ZTE

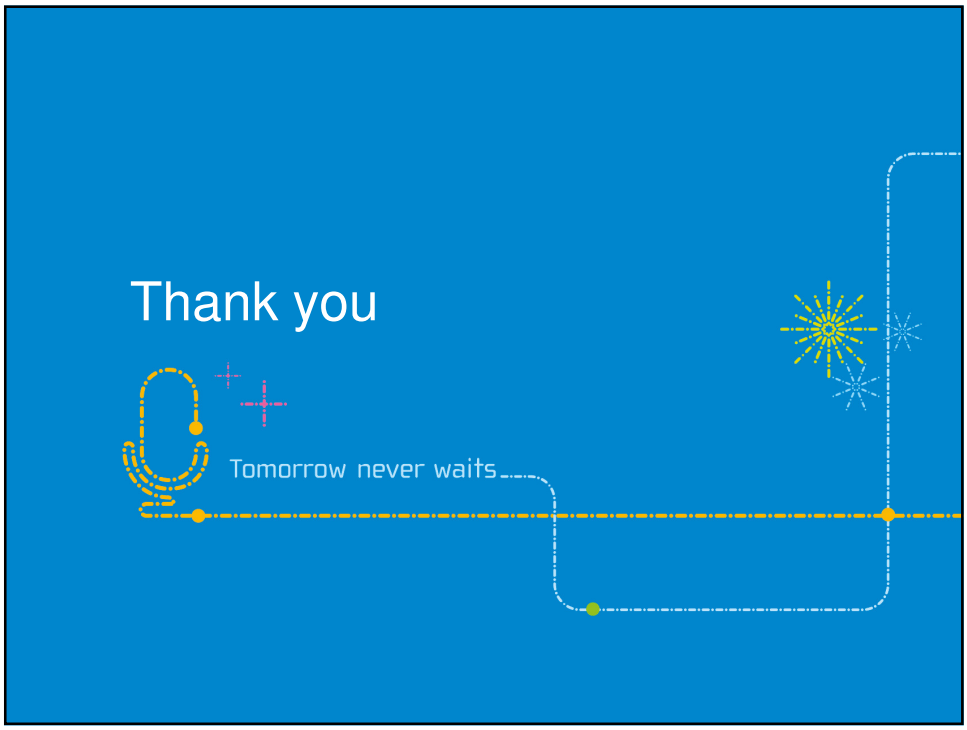
Agenda

- Introduction to PAM4 Modulation
- OIF CEI-56G-LR-PAM4 Specifics
- IBIS-AMI Model Simulation for 56G PAM4 Signals
- The Impact of Channel Characteristics to 56G PAM4 Systems
- Summary

Summary

- The 56G-PAM4 standard is still in continuous update
- IBIS-AMI model works well for 56G PAM4 systems simulation, although the PAM4 modeling is new until today
- After the analysis, we obtain some conclusions about the impact of channel characteristics to the 56G-LR PAM4 systems
  - —The IL resonance frequency should be more than 29GHz
  - —The IL resonance depth should be as smaller as possible
  - —The impedance tolerance is recommended to be less than or equal to +/-8%, and to reduce the discontinuity points as possible as you can
  - —NEXT is playing the leading role in the crosstalk and you might pay more attention to NEXT than FEXT
  - —ICN of crosstalk must be less than 4mV and is recommended to be less than 3mV

ZTE



Achieving Full System Signal Integrity for High Speed Backplane System

Dr. Wenliang Dai
Xpeedic Technology Co., Ltd.

Asian IBIS Summit
Shanghai China
November 11, 2016

XPEEDIC
ACCELERATE YOUR IC DESIGN

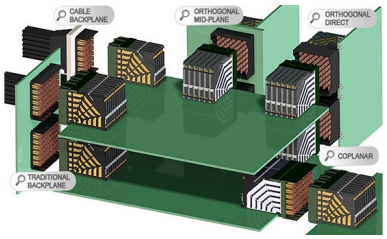
Page 1

Outline

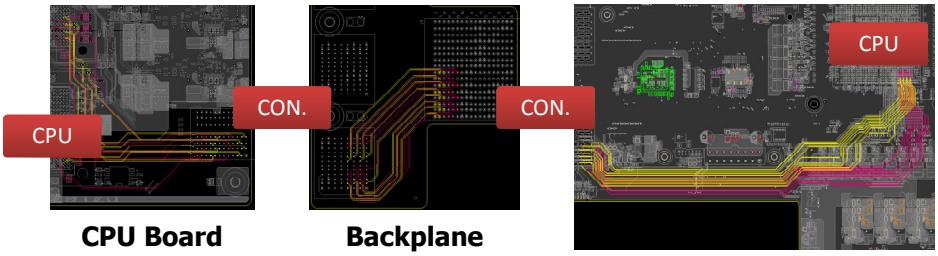
- Introduction of backplane system
- Challenge to backplane system simulation
- Components of EM simulation
- Analysis workflow
- Full backplane system SI simulation
- Summary

Backplane System

- Backplane system is used as a backbone to connect several printed circuit boards together to make up a complete system
- There are various configurations
  - Traditional backplane
  - Orthogonal direct
  - Orthogonal mid-plane
  - Coplanar
  - Cable backplane

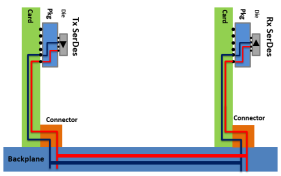


Backplane System Example -- Server Board

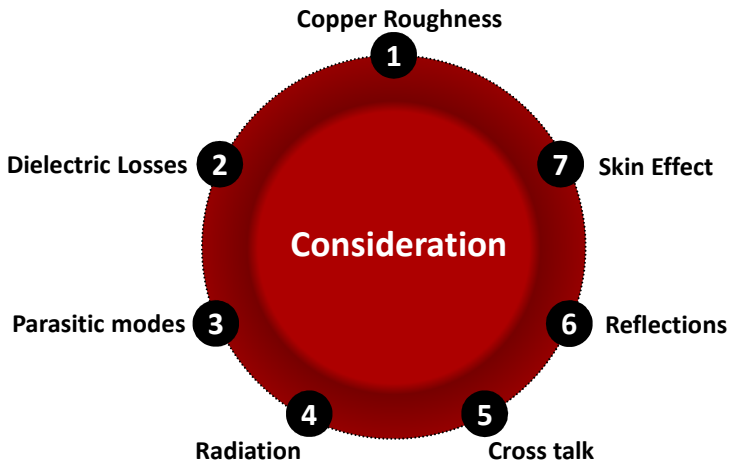


CPU Board **Backplane** **Switch Board**

- Complex PCB layout.
- Maybe system has capacitor or repeater, Engineer need to check repeater gain based on channel's loss.



Backplane Design Consideration



Challenges to Channel SI Simulation

- Reflection noise due to impedance mismatch, via, connector and other discontinuities.
- Need to capture all physical parasitic effects
  - Reflection, Coupling, Delay, Freq. dependent Losses,…
- Measurements become very difficult,
  - Parasitic values are small but important at high speed.
  - Large number of ports for interconnects.
- EM simulation of the discontinuities is a must. However, the current flow suffers the following problems:
  - Manual process to extract the via, trace, and other discontinuities
  - Manual process to build all the channels

Components of EM Simulation

✓ Transmitter

- Transistors
- Sources
- Algorithms
- Passives
- Memory

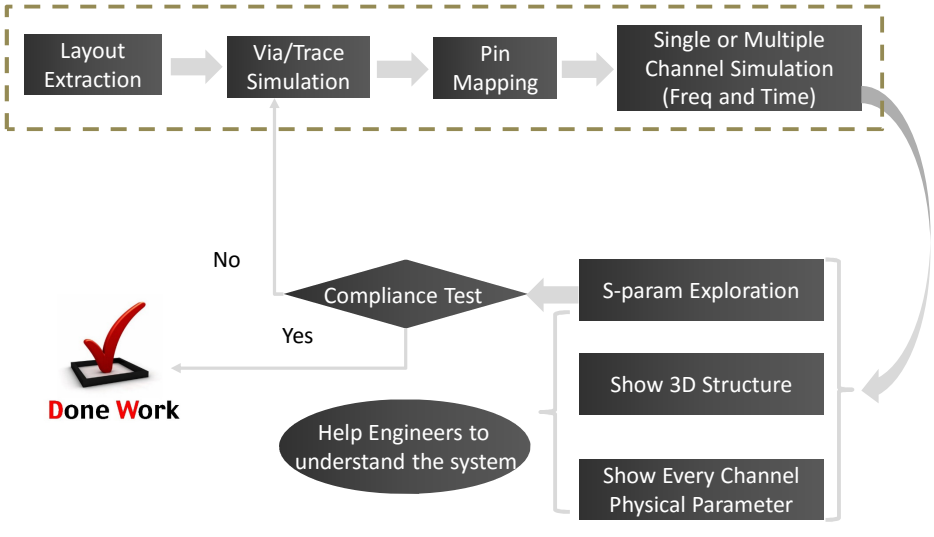
✓ Interconnect

- **Thru Via**
- **BB Via**
- **Microstrip**
- **Stripline**
- **Capacitor**
- **Repeater**
- **Connector**
- **Backdrill**

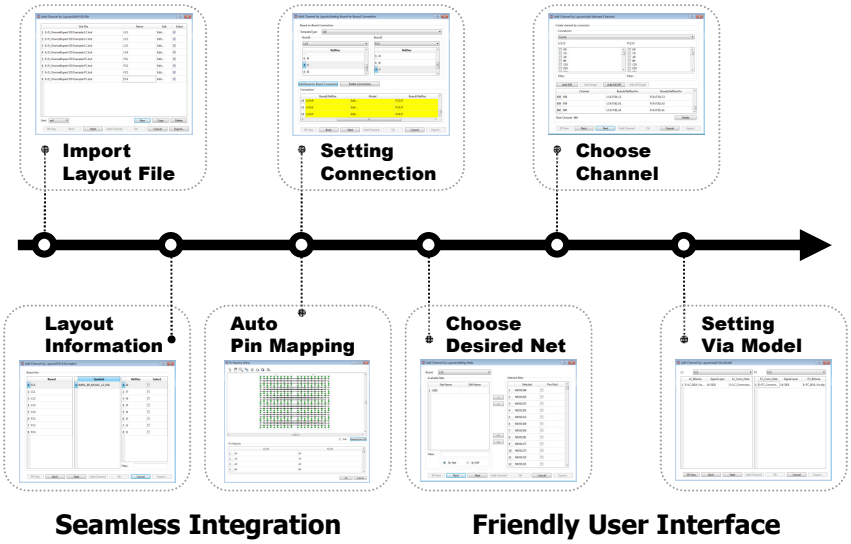
✓ Receiver

- Transistors
- Sources
- Passives
- Memory

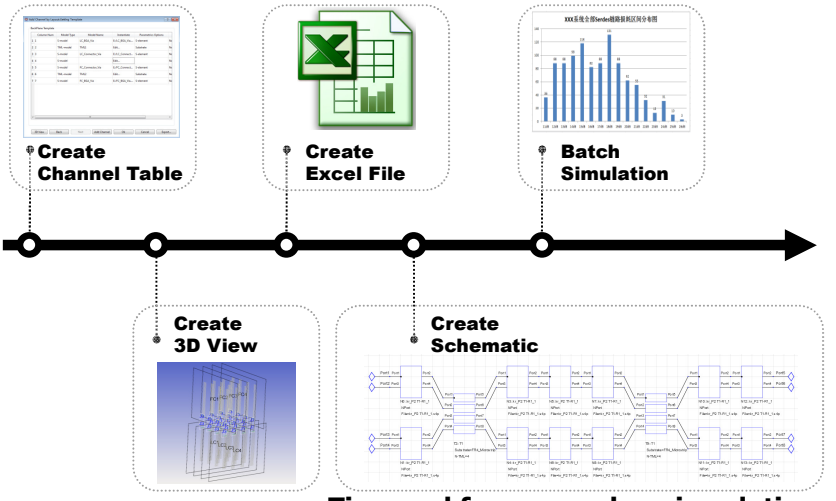
Analysis Workflow



Analysis Workflow

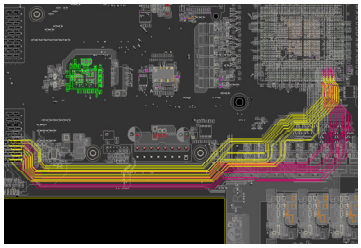


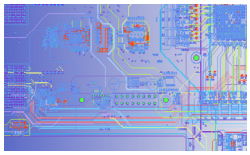
Analysis Workflow



Post-Layout Extraction

- Import all the boards for the backplane system
- Extract vias and traces from layout

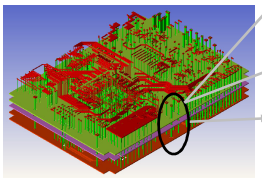


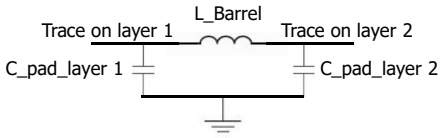


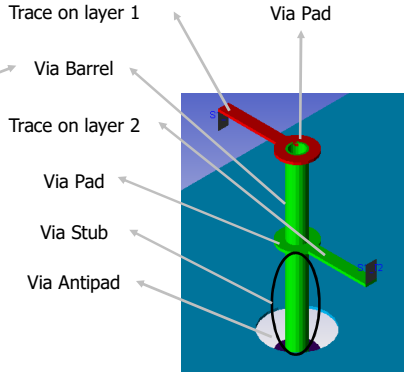
- Layout Files
- Model Template

- Self cleaning process
- Discrete components
- Area/Net selection
- Stackup definition
- Materials definition
- BB, Back drill definition
- Auto port definition
- Parameter/Optimization
- High flexibility

3D Via Modeling



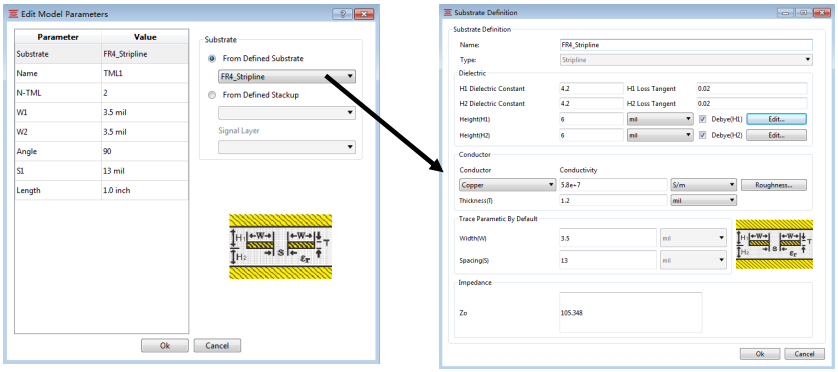




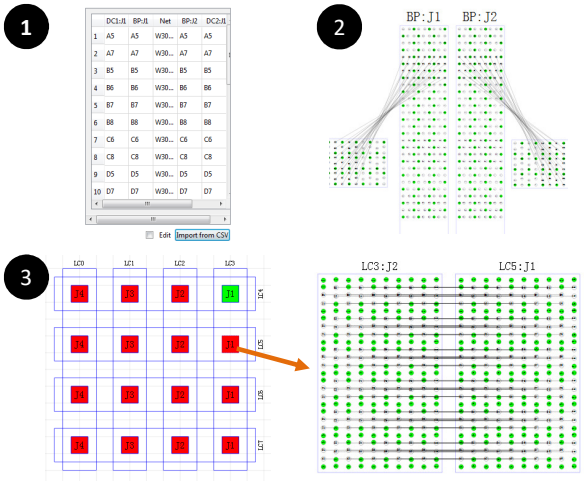
- Via and ground plane will lead to parasitic capacitance and parasitic inductance.
- ***How to deal with a lot of via models?***

Trace Modeling

- For trace, the common approach is to use 2D models for main high speed interconnect.

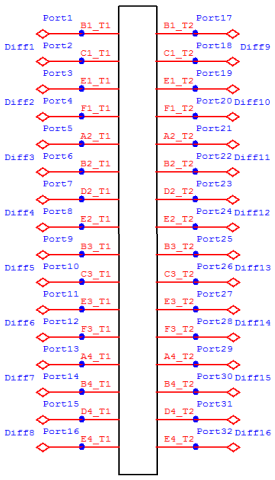


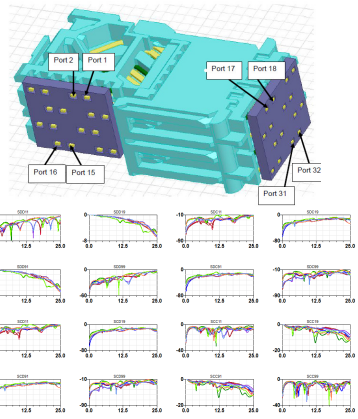
Connection between Boards through Pin Mapping



- Import .csv file.
- Create connection manually
- Create connection base on slot ID.

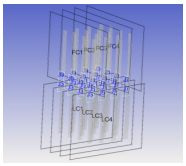
Connector S-parameter from Vendor



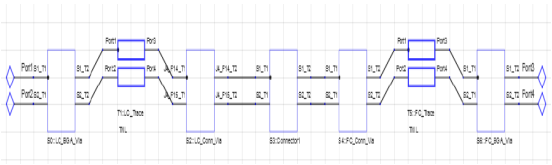


- Connector S-parameter file comes from vendor

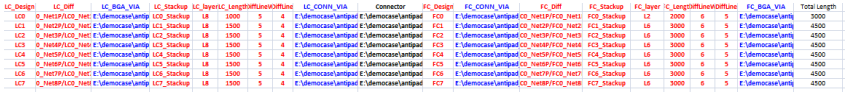
Auto Cascading to Create Channel



Channelview



Cascading

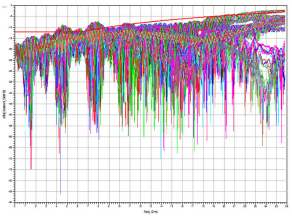


Excel File

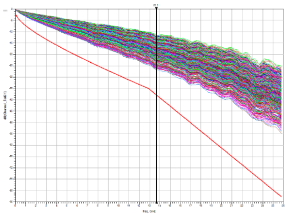
- 3D structure of BP system
- Hide/Show board or net in 3D
- Show entire channel path
- Single vs. multiple simulation and cascading
- Fast and memory efficient
- Show channel's structure size in Excel file
- Easily find worst channel
- Easily generate Excel report

Full Backplane SI Simulation - Frequency Domain

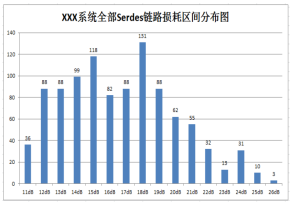
- Full backplane SI simulation is achieved by sweeping all the channels



Full Net Return Loss

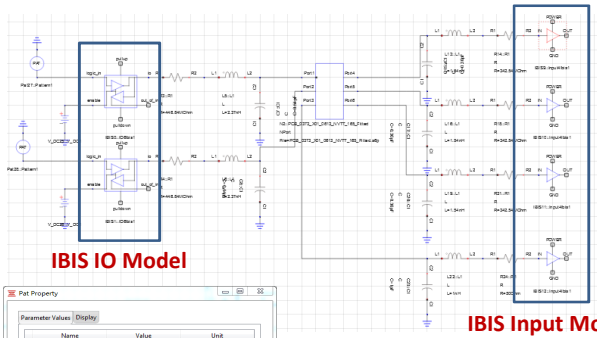


Full Net Insertion Loss

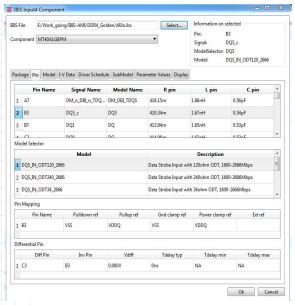


Net Distribution @ 13.67 GHz

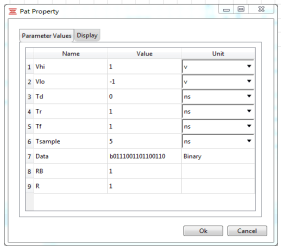
Full Backplane SI Simulation - Time Domain



IBIS IO Model

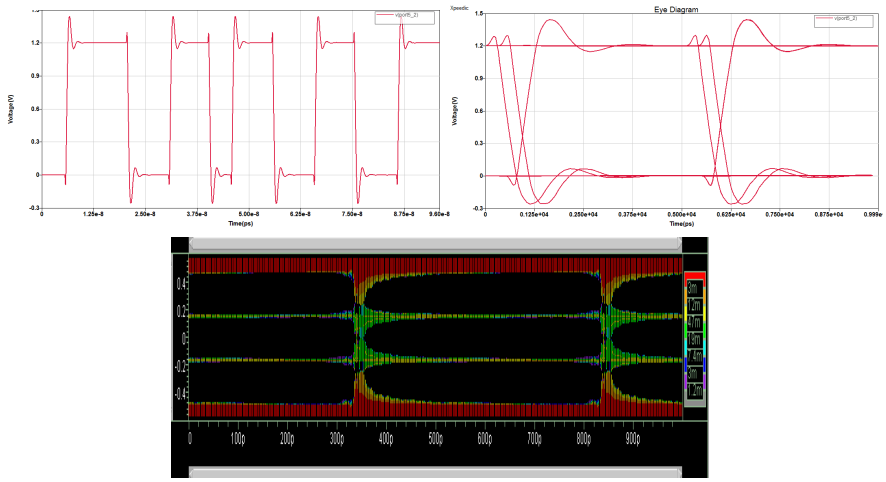


IBIS Input Model



- Support IBIS, IBIS-AMI, Spice model.
- Add proper pattern model.
- Fast modeling and high accuracy.

Full Backplane SI Simulation - Time Domain



Summary

- Passive channel modeling and simulation is essential to high speed channel design.
- Optimal channel design requires user friendly EDA tool to do layout extraction, via optimization, trace simulation, S-parameter cascading, S-parameter exploration, etc.
- Full backplane system SI simulation is achieved by sweeping all the channels with correct models.


XPEEDIC
ACCELERATE YOUR IC DESIGN

On-Die Decoupling Model Improvements for IBIS Power Aware Models

Randy Wolff and Aniello Viscardi
Micron Technology
Asian IBIS Summit
November 11, 2016, Shanghai, China
(Previously given at the European IBIS Summit
May 11, 2016 Turin, Italy)

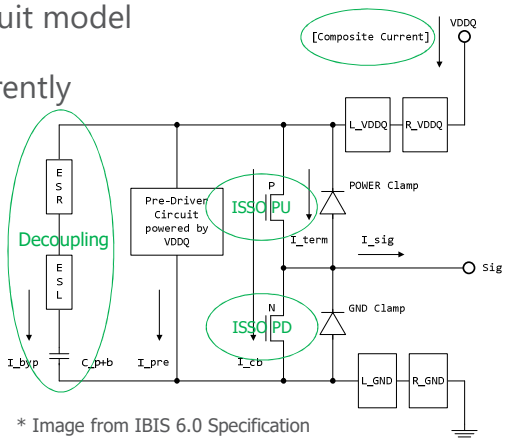
Outline

- IBIS Power-aware modeling overview
- On-die Decoupling models
- Multi-port Decoupling models
- Example Simulations
- Conclusions

IBIS Power-aware Modeling Overview

- Power Integrity modeling uses [Composite Current], [ISSO PU], [ISSO PD] and an IBIS-ISS on-die decoupling circuit model
- Decoupling model external to IBIS currently

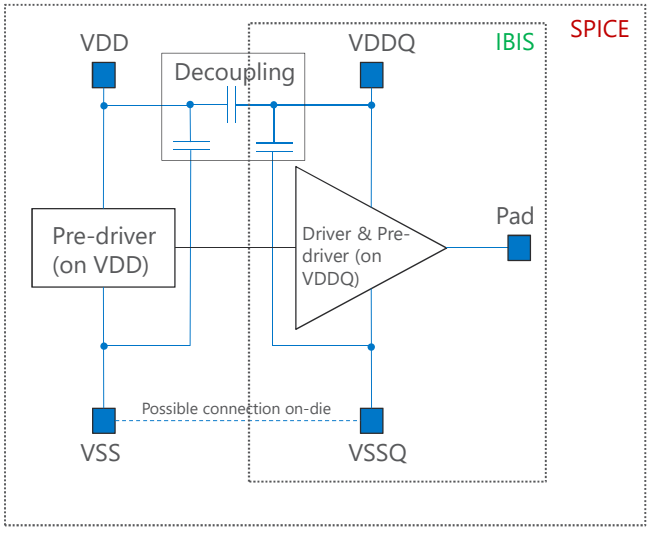
```
I_byp    - Bypass current
I_pre    - Pre-Driver current
I_cb     - Crow-bar current
I_term   - Termination current (optional)
L_VDDQ   - On-die inductance of I/O Power
R_VDDQ   - On-die resistance of I/O Power
L_GND    - On-die inductance of Ground
R_GND    - On-die resistance of Ground
C_p+b    - Bypass + Parasitic Capacitance
ESR      - Equivalent Series Resistance for on-die Decap
ESL      - Equivalent Series Inductance for on-die Decap
```



* Image from IBIS 6.0 Specification

On-die Decoupling Models

- SPICE model may have pre-driver circuits on separate power supplies
- May be one common ground on-die
- Decoupling model could include VDDQ, VSSQ, VDD, VSS
- What is needed for IBIS to correlate with SPICE?



Multi-port Decoupling Models

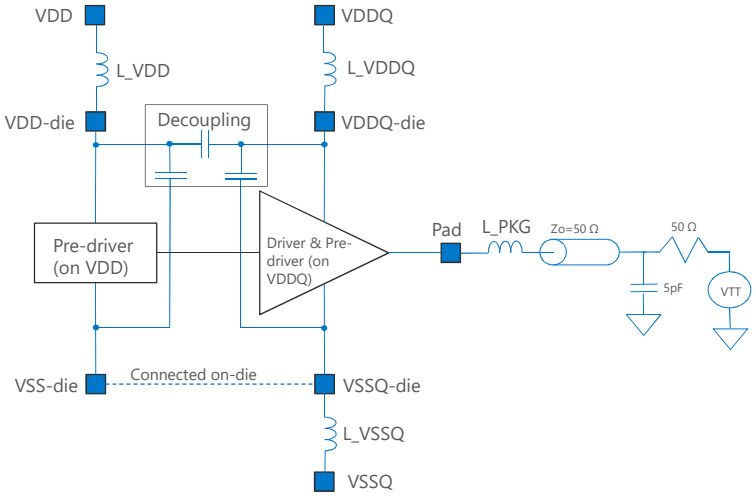
- Decoupling circuits may contain proprietary modeling equations or process data
- A non-proprietary model can be an S-parameter or a broadband SPICE macromodel (of the S-parameter characterization)
- S-parameter port options
  - 1-port: VDDQ with VSSQ reference
  - 2-port: VDDQ, VSSQ, with 0 reference
  - 3 or [4] port: VDDQ, VSSQ, VDD, [VSS], with 0 reference

SPICE Setup Examples for Decoupling Model Creation

- Buffer Instance in Hi-Z state:
  - Xbuff … VDDQ_die VSSQ_die … Buffer_name
- Port Definition:
  - Single Port
    - P1 VDDQ_die VSSQ_die port=1 Z0=50 DC VDDQ
  - Multi Port
    - P1 VDDQ_die 0 port=1 Z0=50 DC VDDQ
    - P2 VSSQ_die 0 port=2 Z0=50 DC 0
- AC Analysis
  - .lin sparcalc=1 filename='s_model.sNp' format=touchstone dataformat=ma freqdigit=10 spardigit=10
  - .ac dec 100 1 10e12

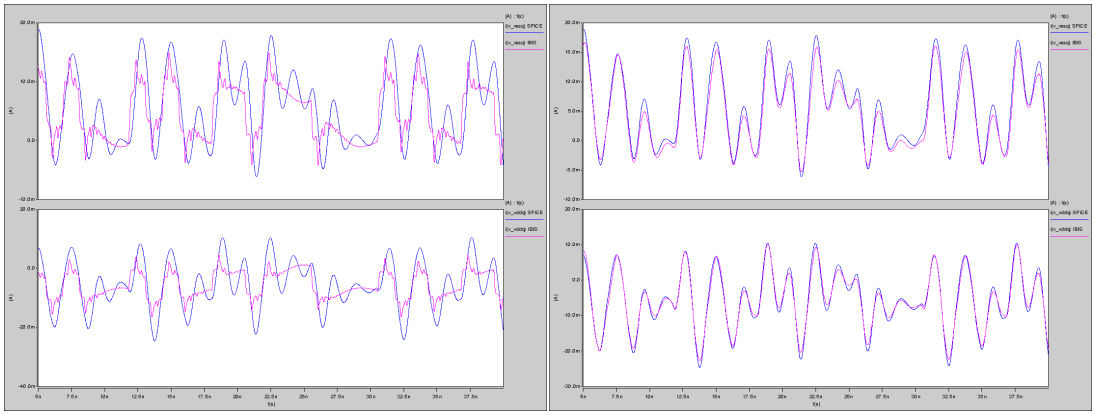
Example Simulation 1 – Ideal VDD
Comparing Transistor-level and IBIS Model in SPICE

- L_VDD=0 (short)
- L_VDDQ=1.25nH
- L_VSSQ=1.25nH
- L_PKG=1.25nH



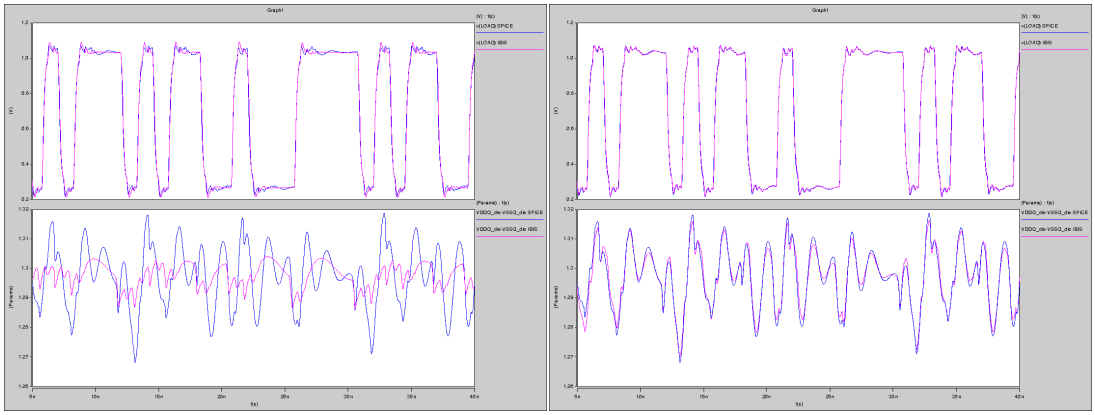
1-Port vs. 2-Port Models, I(VSSQ) and I(VDDQ)

1-Port | **2-Port**



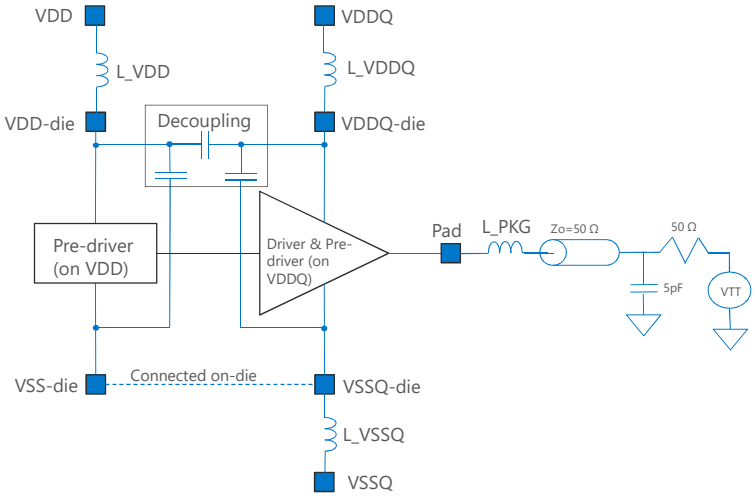
V(LOAD) and V(VDDQ_die)-V(VSSQ_die)

1-Port | **2-Port**



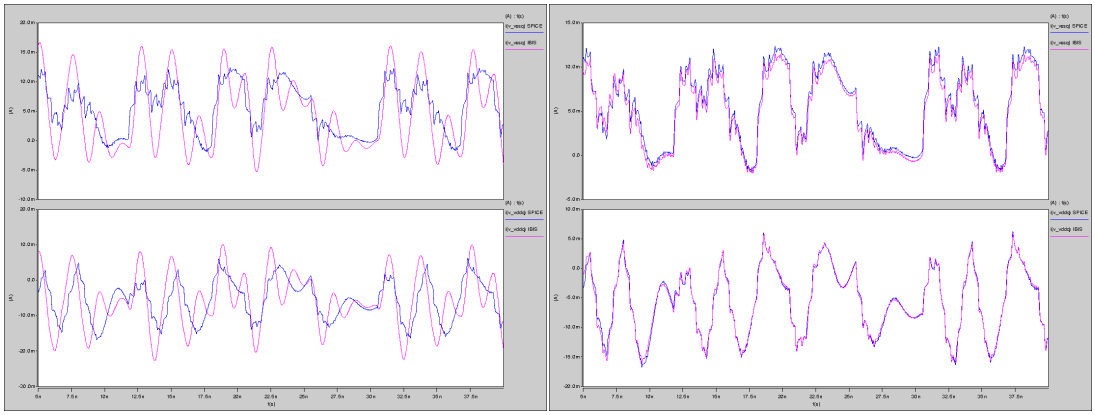
Example Simulation 2 – Non-ideal VDD
Comparing Transistor-level and IBIS Model in SPICE

- L_VDD=1.25nH
- L_VDDQ=1.25nH
- L_VSSQ=1.25nH
- L_PKG=1.25nH



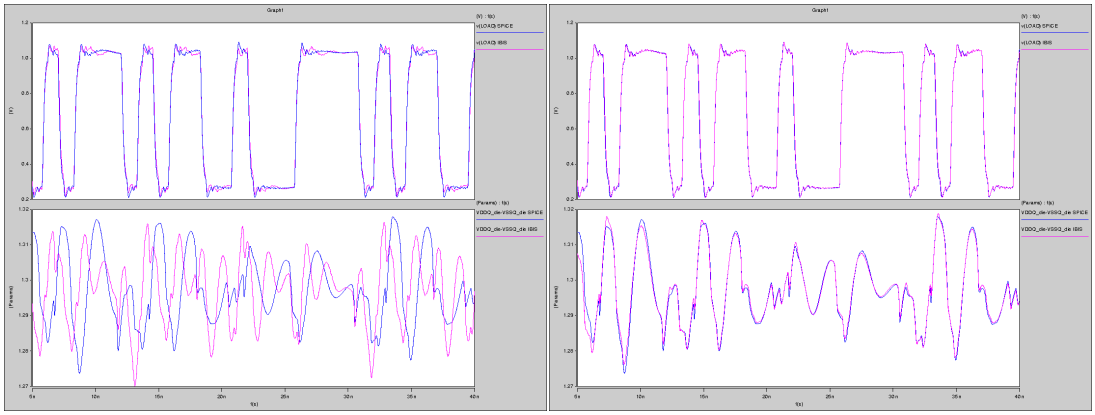
2-Port vs. 3-Port Models, I(VSSQ) and I(VDDQ)

2-Port | **3-Port**



V(LOAD) and V(VDDQ_die)-V(VSSQ_die)

2-Port | **3-Port**



Conclusions

- A 2-port S-parameter (3-terminal macro-model) for on-die decoupling is a better model than a 1-port model for power-aware simulations.
  - This solution requires use of node 0 in the decoupling model.
- Correlating to a SPICE simulation that includes non-ideal supply connections to pre-driver circuits requires extra ports for non-ideal supplies in the decoupling model.
- A multi-port decoupling model is most versatile. Unused ports not connected to a package model should be connected to 0.
- The new IBIS Interconnect BIRD will allow the IBIS-ISS decoupling model to be connected properly to the package model.

Micron®

IBISCHK6 V6.1.3 and Executable Model File Checking

Bob Ross, Teraspeed Labs
bob@teraspeedlabs.com

Asian IBIS Summit
Shanghai, China
November 11, 2016

Goals and Contents

- **New ibischk6 V6.1.3 executables available at the same location:**
  www.ibis.org/ibischk6/
- **Fixes 7 bugs**
- **Differences (new ibischk6 file names)**
- **New – executable model file checking per BUG179 enhancement for [Algorithmic Model] Executable lines**
- **Source code quality assurance tests**
- **Some limitations**

New BUGs 174-180 Fixed
www.ibis.com/bugs/ibischk/

180	Error with Legal List_Tip in Reserved_Parameters with Format List	Mike LaBonte, Signal Intergrity Software (SiSoft)
179	DLL SO Checking and Functional Existence and Platform Information	Mike LaBonte, SiSoft; Bob Ross, Teraspeed Labs; Lance Wang, IO Methodology
178	Error with Same Platform_Compiler_Bits for Rx and Tx of I/O* in IBIS-AMI	Michael Schaeder, Zuken; Bob Ross, Teraspeed Labs
177	Empty [Node Declarations] Stops Parser Completion	Arpad Muranyi, Mentor Graphics; and Bob Ross, Teraspeed Labs
176	[External Model] Error Not Issued for Ports List With Undeclared Port	Arpad Muranyi, Mentor Graphics; and Bob Ross, Teraspeed Labs
175	Incorrect Model References Through [Model Selector] Not Reported	Walter Katz, SiSoft
174	File Not Found Line Printed Under Some Operating Systems	Mike LaBonte, SiSoft and Bob Ross, Teraspeed Labs

New Names for ibischk6

- **Command line operation:**
- **Windows:**
  - **ibischk6_32.exe (versus ibischk6.exe)**
  - **ibischk6_64.exe (versus ibischk6.exe)**
- **Linux (Ubuntu):**
  - **ibischk6_32 (versus ibischk6)**
  - **ibischk6_64 (versus ibischk6)**
- **Used for source code quality assurance tests per BUG179**
- **Macintosh osx_32, osx_64 (also uploaded), but not part of source code release**

New Command Line Based on ibischk6 Name

Example: ibischk6_32.exe ➔"ibischk6_32" command

```
IBISCHK6 V6.1.3

IBISfile validation:
This program has been provided free to the electrical
engineering community by the IBIS Open Forum.  The
purpose of this program is to validate that the contents
of ASCII device data in a file specified conform to the
IBIS specification.
Usage: ibischk6_32       <IBS filename>
     : ibischk6_32  -ebd <EBD filename>
     : ibischk6_32  -pkg <PKG filename>
     : ibischk6_32  -ami <AMI filename>
Usage: ibischk6_32  -caution -numbered      <IBS filename>
     : ibischk6_32  -caution -numbered -ebd <EBD filename>
     : ibischk6_32  -caution -numbered -pkg <PKG filename>
     : ibischk6_32  -caution -numbered -ami <AMI filename>
The flags prior to the file name can be in any order, and the -caution and/or -
numbered flags are optional.
```

Can Rename ibischk6 File (Examples Below)

- **ibischk6.exe as in earlier versions for "ibischk6" command**
- **ibischk613_32.exe showing version and bits detail for "ibischk613_32" command**
- **Etc. - the new ibischk6 file name shows up in the Usage: lines, as shown on previous slide**

Syntax and Notation Related to BUG179

- **Under [Algorithmic Model] Executable, Executable_Rx and Executable_Tx lines have this information:**

  Platform_Compiler_Bits File_Name Parameter_File

- **Platform is operating system such as Linux, Windows**
- **Bits is 32 or 64 for common platforms**
- **File_Name is "executable model file" name such as abc.dll or abc.so**
- **Parameter_File is the .ami file**

Testing and Executable Combinations

- **32-bit and 64-bit operating system, ibischk6_* and executable model files are done consistent with the platform operating system**
  - **Ibischk6_32 will work on 64-bit platforms, but will load and test 32 bit executable model files**
- **Specification does not impose a requirement, but internal Windows requires executable names with at least a dot "."**
- **Message will give the recommended (but not required) extension**

bug179-1.ami
Full Function Existence Checking

```
(bug179
   (Reserved_Parameters
        (AMI_Version (Usage Info)(Type String)(Value "6.1"))
        (Init_Returns_Impulse (Usage Info)(Type Boolean)(Value True))
        (GetWave_Exists (Usage Info)(Type Boolean)(Value True))
        (Resolve_Exists (Usage Info)(Type Boolean)(Value True))
   )
)
```

Function Existence Testing

Each DLL/SO file must contain code symbols for exported functions in one of four possible combinations:

A. Case 1: Executable model file has AMI_Init, AMI_GetWave and AMI_Close. (IBIS 5.0 and above)
B. Case 2: Executable model file has AMI_Init and AMI_Close. (IBIS 5.0 and above)
C. Case 3: Executable model file has AMI_Resolve, AMI_Resolve_Close, AMI_Init, AMI_GetWave and AMI_Close. (IBIS 6.0 and above)
D. Case 4: Executable model file has AMI_Resolve, AMI_Resolve_Close, AMI_Init and AMI_Close. (IBIS 6.0 and above)

Test file names:
: noicgr No "C" combinations above and below
A: icg AMI_Init, AMI_Close, AMI_GetWave
B: ic AMI_Init, AMI_Close
C: icgr AMI_Init, AMI_Close, AMI_GetWave, AMI_Resolve, AMI_Resolve_Close
D: icr AMI_Init, AMI_Close, AMI_Resolve, AMI_Resolve_Close

Some Tests for ibischk6_32.exe when Checked with bug179-1.ami

```
| Normal case: GetWave and ResolveExists return true
|
Executable Windows_1_32 noicgr_32.dll   bug179-1.ami  ← 5 Errors
Executable Windows_2_32 ic_32.dll       bug179-1.ami  ← 3 Errors
Executable Windows_3_32 icg_32.dll      bug179-1.ami  ← 2 Errors
Executable Windows_4_32 icgr_32.dll     bug179-1.ami  ← Good
Executable Windows_5_32 icr_32.dll      bug179-1.ami  ← 1 Error
Executable Windows_6_64 noicgr_64.dll   bug179-1.ami  ← Executable
Executable Windows_7_64 ic_64.dll       bug179-1.ami    lines for 64-bit
Executable Windows_8_64 icg_64.dll      bug179-1.ami    Windows lines
Executable Windows_9_64 icgr_64.dll     bug179-1.ami    not checked
Executable Windows_10_64 icr_64.dll     bug179-1.ami
|
```

Lines 112 to 121

Partial Report for ibischk6_32.exe with New Error Codes

```
E4702 (line  112) - Code file noicgr_32.dll does not contain required AMI_Init() function
E4703 (line  112) - Code file noicgr_32.dll does not contain required AMI_Close() function
E4704 (line  112) - Code file noicgr_32.dll does not contain AMI_GetWave() function, required
because GetWave_Exists=True in AMI file bug179-1.ami
E4705 (line  112) - Code file noicgr_32.dll does not contain AMI_Resolve() function, required
because Resolve_Exists=True in AMI file bug179-1.ami
E4706 (line  112) - Code file noicgr_32.dll does not contain AMI_Resolve_Close() function,
required because Resolve_Exists=True in AMI file bug179-1.ami
E4704 (line  113) - Code file ic_32.dll does not contain AMI_GetWave() function, required because
GetWave_Exists=True in AMI file bug179-1.ami
E4705 (line  113) - Code file ic_32.dll does not contain AMI_Resolve() function, required because
Resolve_Exists=True in AMI file bug179-1.ami
E4706 (line  113) - Code file ic_32.dll does not contain AMI_Resolve_Close() function, required
because Resolve_Exists=True in AMI file bug179-1.ami
E4705 (line  114) - Code file icg_32.dll does not contain AMI_Resolve() function, required
because Resolve_Exists=True in AMI file bug179-1.ami
E4706 (line  114) - Code file icg_32.dll does not contain AMI_Resolve_Close() function, required
because Resolve_Exists=True in AMI file bug179-1.ami
E4704 (line  116) - Code file icr_32.dll does not contain AMI_GetWave() function, required
because GetWave_Exists=True in AMI file bug179-1.ami
```

Line 115 is Good (0 Errors):

```
Executable  Windows_4_32  icgr_32.dll  bug179-1.ami
```

Summary for Platforms/Bits Test for Full Test Case

```
... Status of [Algorithmic Model] Executables for Windows 32:
icr_64.dll:         Windows 64:         Not Checked
icgr_64.dll:        Windows 64:         Not Checked
icg_64.dll:         Windows 64:         Not Checked
ic_64.dll:          Windows 64:         Not Checked
icr_32.dll:         Windows 32:         Checked
icgr_32.dll:        Windows 32:         Checked
icg_32.dll:         Windows 32:         Checked
ic_32.dll:          Windows 32:         Checked
noicgr_64.dll:      Windows 64:         Not Checked
icr_32.dll:         Windows 64:         Not Checked
icgr_32.dll:        Windows 64:         Not Checked
icg_32.dll:         Windows 64:         Not Checked
ic_32.dll:          Windows 64:         Not Checked
noicgr_32.dll:      Windows 64:         Not Checked
icr_64.dll:         Windows 32:         Checked, has platform issue
icgr_64.dll:        Windows 32:         Checked, has platform issue
icg_64.dll:         Windows 32:         Checked, has platform issue
ic_64.dll:          Windows 32:         Checked, has platform issue
noicgr_64.dll:      Windows 32:         Checked, has platform issue
noicgr_32.dll:      Windows 32:         Checked
```

Summary for Platforms/Bits Test for Full Test Case (Continued)

```
icr_64.so:          Linux 64:           Not Checked
icgr_64.so:         Linux 64:           Not Checked
icg_64.so:          Linux 64:           Not Checked
ic_64.so:           Linux 64:           Not Checked
icr_32.so:          Linux 32:           Not Checked
icgr_32.so:         Linux 32:           Not Checked
icg_32.so:          Linux 32:           Not Checked
ic_32.so:           Linux 32:           Not Checked
noicgr_64.so:       Linux 64:           Not Checked
icr_32.so:          Linux 64:           Not Checked
icgr_32.so:         Linux 64:           Not Checked
icg_32.so:          Linux 64:           Not Checked
ic_32.so:           Linux 64:           Not Checked
noicgr_32.so:       Linux 64:           Not Checked
icr_64.so:          Linux 32:           Not Checked
icgr_64.so:         Linux 32:           Not Checked
icg_64.so:          Linux 32:           Not Checked
ic_64.so:           Linux 32:           Not Checked
noicgr_64.so:       Linux 32:           Not Checked
noicgr_32.so:       Linux 32:           Not Checked
... This IBISCHK6 executable supports Windows 32 bit only

Errors  : 28

File Failed
```

Status Report Lines

- Checked
- Not checked
- Checked, has platform issue
  - Platform bits different than operating system platform Bits
  - Executable model file does not have dll or so extension
  - Ibischk6_32 cannot load 64-bit executable model files and visa versa
- "… This IBISCHK6 executable supports Windows 32 bit only"
  - Refers to ibischk6_32.exe used in test

Recommended Extensions

- Windows: dll
- Linux: so
- No requirement but some Windows versions require executable names with at least a dot "."
- Other messages may suggest .dll for Windows or .so for Linux)

Limits and Issues

- ibischk6_32 works on 64-bit platforms if 32-bit executable model files load and work on the platform
- Platform name examples shown in the IBIS Specification – some may be specified in the future
  - Case insensitive Windows
  - Case insensitive Linux
- For unknown platform names, ibischk6 will try to load executable model file and run the functional existence test

Future and Conclusion

- No reference IBIS-AMI waveform checking
- Some commercial vendors offer reference IBIS-AMI waveform checking
- ibischk6 V6.1.3 valuable for function existence testing for Reserved_Parameters documented in the .ami file

TOUCHSTONE CONVERSION WRAPPER

ASIAN IBIS SUMMIT
SHANGHAI CHINA
NOVEMBER 11, 2016

Anders Ekholm

AGENDA

- Using TSCHK2 for touchstone format conversion
- Problem statement
- Fixing the problem using a Wrapper
- A Perl wrapper
- Solves the current issue of losing comments
- Wrapper avaliable on the IBIS webpage.

USING TSCHK2 FOR TOUCHSTONE FORMAT CONVERSION

The touchstone checker TSCHK2 from IBIS Open Forum can also be used for converting Touchstone models (TS) to Touchstone 2 model format.

To do so use the option –canonical e.g.:

Tschk2 –canonical ts1.s4p > ts2.s4p

This will fit the data into the TS2 model format, but will not add any extra data.

PROBLEM STATEMENT

However, doing so strips out any comments from the original touchstone file e.g.,

```
!Murata Part Number: GRM15XR11E222KA86
!These Parameters are Measured in Series Mode Connection
!      o--ll--o
!Port1          Port2
!      o------o
!Operation Temp=25[C], DC Bias Voltage=0[V]
!Freq. Start=300[kHz] Stop=6000000[kHz] 401[Steps]
# Hz S RI R 50
!Freq.(Hz)    S 11(Real)    S 11(Imag)    S 21(Real)    S 21(Imag)    S 12(Real)    S 12(Imag)    S 22(Real)    S 22(Imag)
300000        0.8473370     -0.3552390    0.1526630     0.3552390     0.1526630     0.3552390     0.8473370     -0.3552390
307520        0.8409069     -0.3612905    0.1590931     0.3612905     0.1590931     0.3612905     0.8409069     -0.3612905
```

PROBLEM STATEMENT

Becomes:

```
! Touchstone data file
[Version] 2.0
# Hz S RI R 50
[Number of Ports] 2
[Two-Port Data Order] 12_21
[Number of Frequencies] 401

[Network Data]
! freq          S11re          S11im          S12re          S12im          S21re          S21im          S22re
S22im
300000         0.847337       -0.355239      0.152663       0.355239       0.152663       0.355239
0.847337       -0.355239
307520         0.8409069      -0.3612905     0.1590931      0.3612905      0.1590931      0.3612905
0.8409069      -0.3612905
```


FIXING THE PROBLEM USING A WRAPPER

So to mitigate the problem without having to change TSCHK2, I wrote a small Perl wrapper.

Wrapper is a software code that sort of wraps around another code in this case the tschk2.

- The Perl wrapper will take the file to convert as input. It will read all the comments before the data and all the comments after the data and save those in memory.
- It will then run the tschk2 on the file to convert and save the result in temp.ts2
- Then it will read the temp.ts2 file and reinsert the comments into the output file xxxxx.snp

A PERL WRAPPER

```
#!/usr/bin/perl
#TS1toTS2 is a small wrapper to IBIS Open Forums tschk2, since using the IBIS Open Forums converting feature to convert models will not retain comments from the original file
#So this wrapper will read and save the comments run tschk2 and convert the model, after this it will read the converted model and add the comments
#and output that as the converted file. It will use the same file name for the output and the old touchstone file will be saved as .TS1
#It will only convert touchstone files into touchstone 2 files.
#It is a command line tool. It implemented as a quick & dirty solution so feel free to enhance it if you need to.

#This section will pick up the ts filename from the command line if missing give you an error
$options=join " ",@ARGV;
if ($ARGV=~/-h/)
…….
#read all the comments in the original file
open FIL,"<$file" or die "\n\nCan't open file: $file";
……
#Run tschk to convert file
……..  system "copy $file $newfile";
# add the comments in the final model.
open FIL,"<temp.ts2" or die "\n\nCan't open file: temp.ts2";
……
```


SOLVES THE CURRENT ISSUE OF LOSING COMMENTS

This solves our current problem of losing information from the original model when converting it into TS2.

We are trying to standardize on our S-parameter models in TS2 format.

WRAPPER AVAILABLE ON THE IBIS WEBPAGE

The wrapper has been made available on the IBIS Open Forum webpage.

Please feel free to use it.

It is distributed in source code format so you can adapt it to your specific needs.

http://www.ibis.org/tschk2/

ERICSSON