WELCOME FROM MIKE LABONTE, IBIS OPEN FORUM

Ladies and Gentlemen,

As chair of the IBIS Open Forum it is my pleasure to welcome you to the 2017 Asian IBIS Summit in Shanghai and to thank you for your presentations and participation. We are grateful to our sponsors Huawei Technologies, Cadence Design Systems, IO Methodology, Mentor, a Siemens Business, MostecEDA (SPISim), Synopsys, Teledyne LeCroy, and ZTE Corporation for making this event possible.

Since 1993 IBIS has provided the digital electronics industry with specifications to make signal, timing, and power integrity analyses much easier and faster. With the introduction of IBIS-AMI in 2008, the IBIS community generated new energy for high speed electronic design. IBIS is now known by engineers worldwide and is a required technology for many applications.

Support for IBIS in Asia has been strong, and the IBIS Open Forum looks forward to continued innovation and contributions from technology companies in Asia.

Thank you!

Mike LaBonte
SiSoft
Chair, IBIS Open Forum

WELCOME FROM MIKE LABONTE, IBIS OPEN FORUM

女士们先生们，

作为 IBIS 开放论坛的主席，我高兴地欢迎您参加 2017 年上海亚洲 IBIS 峰会，感谢您的介绍和参与。我们非常感谢我们的赞助商华为技术有限公司，Cadence Design Systems，IO Methodology Inc.，Mentor-a Siemens Business，MostecEDA（SPISim），Synopsys，Teledyne LeCroy 和中兴通讯，为此事件做出了可能。

自 1993 年以来，IBIS 为数字电子行业提供了使信号，时序和电源完整性分析更容易和更快速的规范。随着 IBIS-AMI 在 2008 年的推出，IBIS 社区为高速电子设计创造了新的能量。 IBIS 现在已被世界各地的工程师所了解，是许多应用所需的技术。

IBIS 在亚洲的支持一直很强，IBIS 开放论坛期待着亚洲技术公司的不断创新和贡献。

谢谢！

Mike LaBonte (**迈克 拉邦地**)
SiSoft 公司
主席，IBIS 开放论坛

WELCOME FROM HANG YAN, HUAWEI TECHNOLOGIES

Ladies and Gentlemen,

On behalf of Huawei Technologies, welcome to the 13th annual Asian IBIS Summit (China). I would like to express my appreciation to IBIS Open Forum and all the sponsors for co-organizing this event.

Since 2005, IBIS Asian Summit in China has been the top-level international conference in high speed digital design society in China. I am looking forward to work with IBIS members in China, and to expand our participations in the region. With the demand of high speed design, modeling and simulation technology will still be the key to find the solution. Accuracy, efficiency and complexity are the challenge we are facing now. Intelligence and digitization will be the trend.

Huawei has actively involved in all IBIS society's events. We hope to resolve high speed link issues with IBIS Open Forum, EDA vendors and IC vendors. Your comments and suggestions will be deeply appreciated! And any suggestion for China region technical discussion and activity are also welcome!

Welcome all of you to Shanghai! Hope you will enjoy all the technical discussions and sharing throughout the meeting, and have a nice journey!

Thank you!
Hang Yan
Huawei Technologies

WELCOME FROM HANG YAN, HUAWEI TECHNOLOGIES

各位专家，各位来宾：

我代表华为公司，欢迎大家来参加第 13 届亚洲 IBIS 技术研讨会，衷心地感谢 IBIS 协会组织本次会议。

自从 2005 年以来，IBIS 技术研讨会已经成为了中国高速设计领域的一次盛会。我很高兴有机会与 IBIS 协会一起促进和扩大在该领域的分享。在未来的高速设计中，模型和仿真技术仍将是解决问题的重要手段，准确度、速度和复杂度是我们面临的挑战，智能化和数字化是未来的方向。

华为积极参与各项 IBIS 活动，希望与 IBIS 协会、EDA 软件、芯片公司一道来共同解决许多高速链路设计上的挑战，欢迎大家会上讨论。同时也欢迎大家对我们中国区在 IBIS 技术讨论和组织上提出建议。

欢迎 IBIS 专家来到上海，希望你们能够喜欢所有的技术讨论和会议分享，度过美好一天。

谢谢大家
华为公司 严航

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 **SIGN IN**
- Vendor Tables Open at 8:30

8:45 **WELCOME**
- Yan, Hang (Paul)
  (Huawei Technologies, China)
- LaBonte, Mike (Chair, IBIS Open Forum)
  (SiSoft, USA)

9:00 **IBIS Update** **7**
LaBonte, Mike (SiSoft USA)

9:25 **IBIS Interconnect Modeling Using IBIS-ISS and Touchstone** **16**
Mirmak, Michael (Intel Corporation, USA)

10:00 **Signal Integrity Analysis for 56G-PAM4 Channel of 400G Switch** . . . **29**
Feng, Sophia; Wen, Vincent (Celestica, China)

10:30 **BREAK** (Refreshments and Vendor Tables)

10:50 **Think PAM4 SerDes** **40**
Zhou, Xiaojun (Huawei Technologies, China)

11:20 **Comparison of Time Domain and Statistical IBIS-AMI Analyses** **51**
LaBonte, Mike (SiSoft USA)

12:00 **FREE BUFFET LUNCH** (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

13:30 **A Way to Evaluate Post-FEC BER Based on IBIS-AMI Model 71**
Yu, Yanye; Guo, Tao; Zhu, Shunlin (ZTE Corporation, China)

14:00 **Characterizing and Modeling of a Linear CTE 84**
Liang, Skipper (Cadence Design Systems, China)

14:30 **Using DATA Files for IBIS-AMI Models 99**
Wang, Lance (IO Methodology, USA)

15:00 **BREAK** (Refreshments and Vendor Tables)

15:20 **IBIS-AMI Modeling Using Scripts and Spice Models 109**
Huang, Wei-hsing (SPISim, USA)

15:50 **Leveraging IBIS Capabilities for Multi-Gigabit Interfaces 118**
Willis, Ken (Cadence Design Systems, USA)

16:20 **DISCUSSION**

17:20 **CONCLUDING ITEMS**

17:30 **END OF IBIS SUMMIT MEETING**

IBIS Update

Mike LaBonte
SiSoft
Chair, IBIS Open Forum

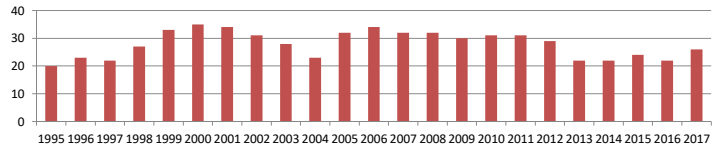
2017 Asian IBIS Summit
Shanghai, PRC
November 13, 2017

http://www.ibis.org/

Organization

26 IBIS Members

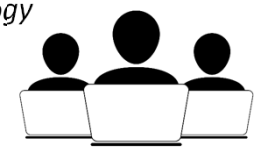
Number of Members by Year



Organization

IBIS Officers 2017-2018

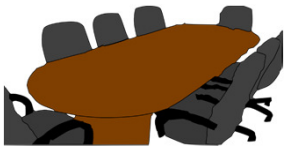
Chair:	*Mike LaBonte, SiSoft*
Vice-Chair:	*Lance Wang, IO Methodology Inc.*
Secretary:	*Randy Wolff, Micron Technology*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Anders Ekholm, Ericsson*
Postmaster:	*Curtis Clark, ANSYS*
Webmaster:	*Mike LaBonte, SiSoft*



2018 Officer Election nominations open May 17

Organization

IBIS Meetings



- Weekly teleconferences
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays)
- IBIS Open Forum teleconference every 3 weeks
  - 486 meetings so far
- IBIS Summit meetings: DesignCon, IEEE SPI, EDICON USA, EPEPS, Shanghai, Taipei, Tokyo

Organization

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees Thomas Munns, Phyllis Gross, Dorothy Lloyd
- SAE ITC provides financial, legal, and other services
- http://itc.sae.org/

Organization

Task Groups

- Interconnect Task Group
  - Chair: Michael Mirmak
  - http://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi
  - http://ibis.org/atm_wip/
  - Develop most other technical BIRDs
- Quality Task Group
  - Chair: Mike LaBonte
  - http://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development
- Editorial Task Group
  - Chair: Michael Mirmak
  - http://ibis.org/editorial_wip/
  - Produce IBIS Specification documents

Specification Development

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2018? IBIS 7.0

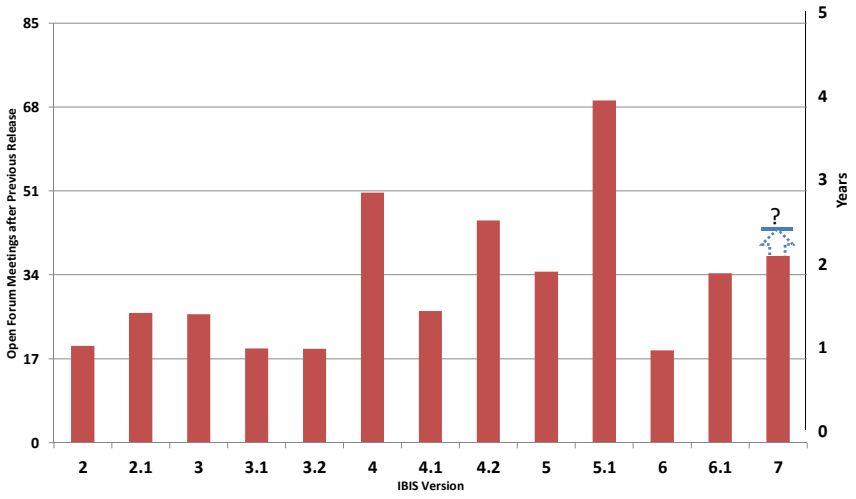
Current development

Other Work

- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone 2.0***
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

Specification Development

IBIS Version Development



As of 13-Nov-2017

Specification Development

Possible IBIS 7.0 Timeline

Meeting Date	Milestone
4/21/2017	Vote to establish 7.0 as the next IBIS version passes
5/12/2017	*BIRD review and acceptance (10 meetings)*
…	…
2/16/2018	Vote to approve 7.0 BIRD set is scheduled for next meeting
3/9/2018	7.0 BIRD set accepted. Editorial work begins
3/30/2018	
4/20/2018	
5/11/2018	Editorial announces 7.0 ready. Review period begins
6/1/2018	
6/22/2018	Vote to ratify 7.0 scheduled for next meeting
7/13/2018	7.0 ratified

BIRD = Buffer Issue Resolution Document

Specification Development

BIRDs Possibly Included in IBIS 7.0

BIRD	Title
147.6	Back-channel Support
158.7	AMI Ts4file Analog Buffer Models
179	New IBIS-AMI Reserved Parameter Special_Param_Names
180	Require Unique Pin Names in [Pin]
182	POWER and GND [Pin] signal_name as [Pin Mapping] bus_label
183	[Model Data] Matrix Subparameter Terminology Correction
184.2	Model_name and Signal_name Restriction for POWER and GND Pins
185.2	Section 3 Reserved Word Guideline Update
186.4	File Naming Rules
187.3	Format and Usage Out Clarifications
188.1	Expanded Rx Noise Support for AMI
189.4	Interconnect Modeling Using IBIS-ISS and Touchstone
191.2	Clarifying Locations for Si_location and Timing_location
192.1	Clarification of List Default Rules

Green = currently accepted BIRD

Specification Development

BIRDs Possibly Excluded from IBIS 7.0

BIRD	Title
125.1	Make IBIS-ISS Available for IBIS Package Modeling
145.3	Cascading IBIS I/O buffers with [External Circuit]s using the [Model Call] keyword
166.2	Resolving problems with Redriver Init Flow
163	Instantiating and Connecting [External Circuit] Package Models with [Circuit Call]
164	Allowing Package Models to be defined in [External Circuit]
165	Parameter Passing Improvements for [External Circuit]s
181.1	I-V Table Clarifications
190	Clarification for Redriver Flow

White = currently not an accepted BIRD

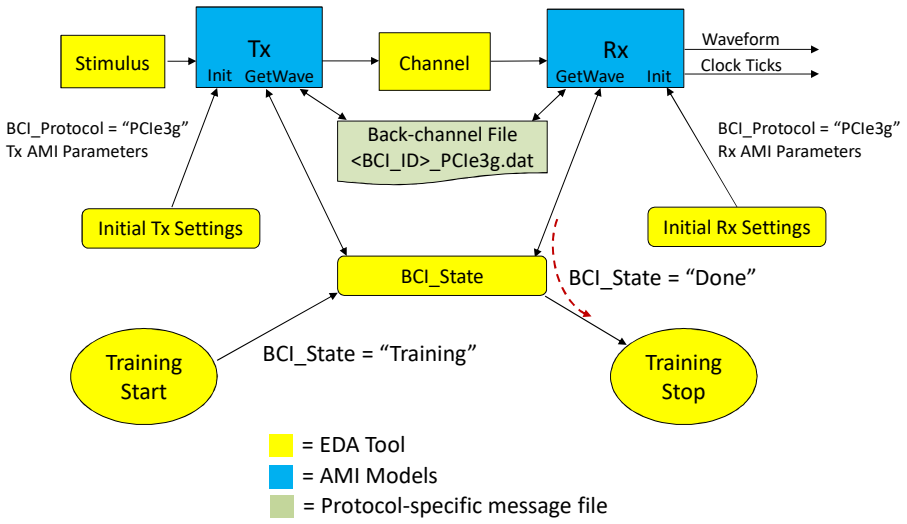
Specification Development

BIRD 147.6, Back-channel Support

- Enable back-channel link training messages between the Tx and Rx executable models to enable link training to optimize equalization settings during time domain (AMI_GetWave) simulations.
- New AMI Parameters:
  - BCI_Protocol, BCI_State, BCI_ID, BCI_Message_Interval_UI, BCI_Training_UI

Specification Development

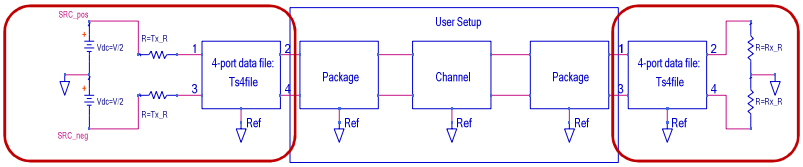
Link Training Back-channel



Specification Development

BIRD 158.7, AMI Ts4file Analog Buffer Models

- Touchstone on-die analog models for IBIS-AMI models directly included from the AMI file, bypassing the analog model in the IBIS file.
- Same as "TStoneFile" models, now "Ts4file".



Specification Development

BIRD 188.1, Expanded Rx Noise Support for AMI

- Bounded (uniform) Rx Noise must be supported by IBIS-AMI, separately from the existing Gaussian random Rx Noise parameter.

Parameter:	**Rx_Noise, Rx_GaussianNoise**
Required:	No, and Rx_Noise is illegal before AMI_Version 6.0; No, and Rx_GaussianNoise is illegal before AMI_Version 7.0

Parameter:	**Rx_UniformNoise**
Required:	No, and illegal before AMI_Version 7.0

Specification Development

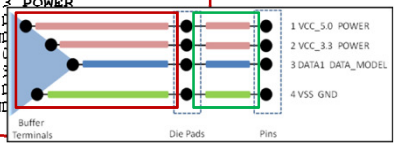
BIRD 189.4, Interconnect Modeling Using IBIS-ISS and Touchstone

```
[Interconnect Model Set]      Full_ISS_buf_pad_pin_PDN_4

[Interconnect Model]          Full_ISS_pad_pin_IO
File_IBIS-ISS   full_pad_pin_io.iss          full_pad_pin_IO_typ
Number_of_terminals = 8
1  Pin_Rail     pin_name       1     |  VCC_5.0 POWER
2  Pin_Rail     pin_name       2     |  VCC_3.3 POWER
3  Pin_I/O      pin_name       3     |  DATA1 DATA_MODEL
4  Pin_Rail     pin_name       4     |  VSS GND
5  Pad_Rail     pad_name     VCC1    |  VCC_5.0 POWER
6  Pad_Rail     pad_name     VCC2    |  VCC_3.3 POWER
7  Pad_I/O      pin_name       3     |  DATA1 DATA_MODEL
8  Pad_Rail     pad_name     VSS1    |  VSS GND
[End Interconnect Model]

[Interconnect Model]          Full_ISS_buf_pad_IO
File_TS         full_buf_pad_io.s8p |        full_buf_pad_IO_typ
Number_of_terminals = 8
1  Pad_Rail     pad_name     VCC1    |  VCC_5.0 POWER
2  Pad_Rail     pad_name     VCC2    |  VCC_3.3 POWER
3  Pad_I/O      pin_name       3     |  DATA1 D
4  Pad_Rail     pad_name     VSS1    |  VSS GND
5  Buffer_Rail  pin_name       1     |  VCC_5.0
6  Buffer_Rail  pin_name       2     |  VCC_3.3
7  Buffer_I/O   pin_name       3     |  DATA1 D
8  Buffer_Rail  pin_name       4     |  VSS GND
[End Interconnect Model]

[End Interconnect Model Set]
```



[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.

Interconnect Modeling Update Using IBIS-ISS and Touchstone

Michael Mirmak
Intel Corporation
michael.mirmak@intel.com

Asian IBIS Summit
Shanghai, PRC
November 13, 2017

Agenda

- History
- The need for improved interconnect support
- Principles of the Interconnect Proposal
  - Structure
  - Terminals, Models and Sets, and Groups (new)
  - New Keywords
- An example explained
- New or changed features
- Summary

History

- Interconnect Task Group resumed meeting in early 2014
  - Received draft BIRD from Walter Katz (SiSoft) to support IBIS-ISS packages within IBIS
- BIRD189.x uploaded (awaiting approval)
  - http://www.ibis.org/birds/
  - 41 pages with examples
  - Still resolving some issues
  - Comments welcome
- Intended for IBIS Version 7.0
- Brief overview with some key points is given here

Why Update Interconnect Modeling?

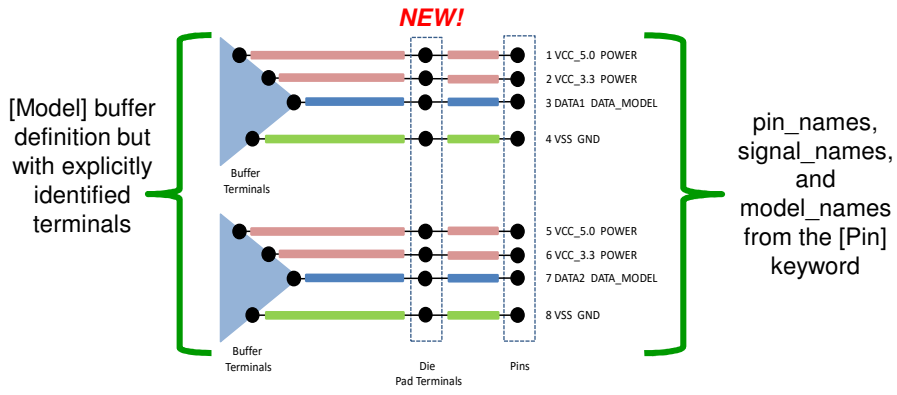
- Improve package models with IBIS-ISS (an HSPICE subset) and Touchstone support
- Package modeling in IBIS stable since 2000
  - [Pin], [Package], [Package Model]
  - [Alternate Package Models] selector added
  - Limited support of loss, crosstalk and/or partitioning
- EBD (Electrical Board Description) for boards; No coupling and limited package model application
- IBIS, IBIS-ISS, Touchstone 2.0 and ICM are separate specifications
  - Limited interaction between them for package modeling
  - ICM (Interconnect Model) never adopted by industry

Features of the Interconnect Proposal

- Supports…
  - IBIS-ISS and Touchstone models (common in industry)
  - Both I/O and supply (POWER and GND) connections
  - (New) optional Die pad interface between Pins and Buffers
  - I/O pin_names as terminal qualifiers
    - *May have optional Aggressor_Only designation*
  - POWER and GND terminal qualifiers by pin_name, pad_name, signal_name or [Pin Mapping] bus_label for rail connections with direct or combined terminals
  - Many other features not covered here

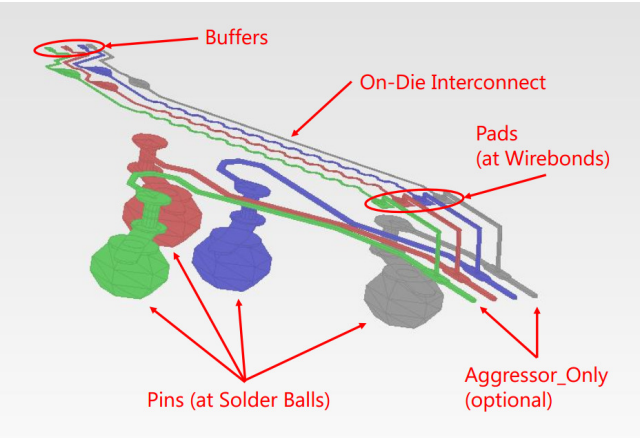
A few objectives for the Interconnect Modeling proposal

Structure of the Interconnect Proposal



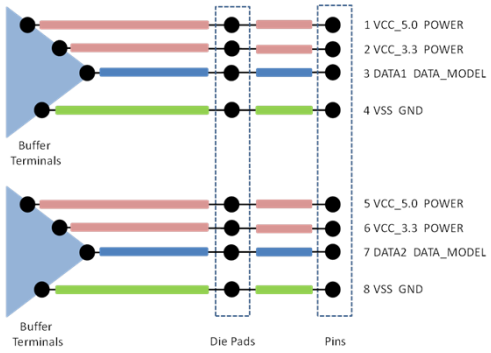
Introduces optional Die pad interface for terminals separate from Buffer and Pin interface terminals

Relates to Physical Structures



One-to-one path connection; Die pad interface optional; Aggressor_Only designation optional

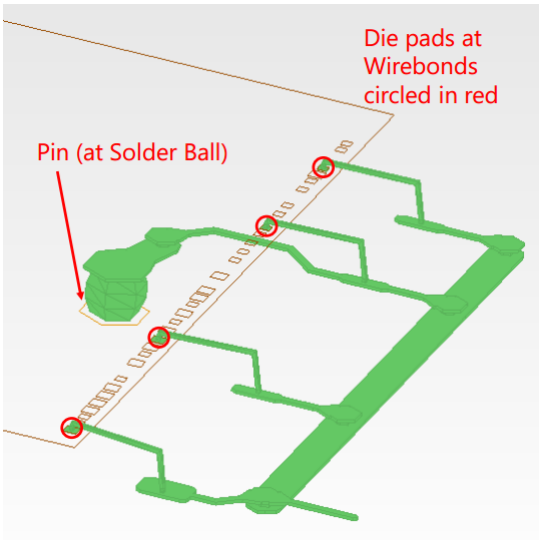
Terminals at Buffer, Die Pad and Pin Interfaces



Original IBIS (4.0 and earlier)
- Pins are explicit
- Buffer terminals implicit in [Model]
- Die pad terminals same as buffer terminals
- Packages defined connections between pins and buffers

Current Proposal
- Die pad terminals are now explicit
- Buffer terminals are now explicit
- [Pin]s are…. still pins
- Separate interconnect definitions can be created between …
  - Pin-to-Die pad terminals,
  - Die pad-to-Buffer terminals,
  - Pin-to-Buffer terminals (still) supported

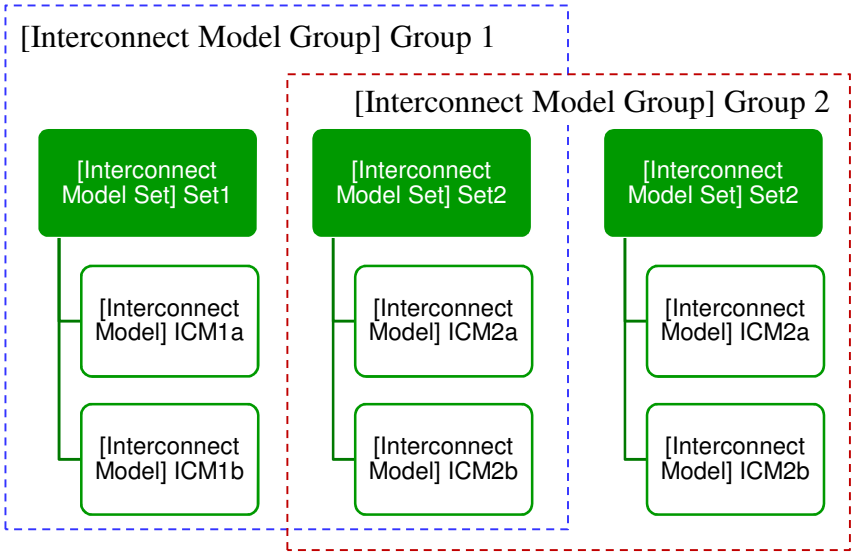
Physical Rails (Can be Merged)



New Keywords and Subparameters (Limited Discussion Here)

- [Bus Labels] | bus_label
- [Die Supply Pads] | pad_name, optional bus_label
- [Interconnect Model]/[End Interconnect Model]
  - Unused_port_termination <Open | Ref.> | Unused port ref. Z
  - Param | parameter passing
  - File_IBIS-ISS | names IBIS-ISS file
  - File_TS, File_TS0 | names Tstone file
  - Number_of_terminals=<value> | number of terminals
  - <terminal lines> | described later
- [Interconnect Model Set]/[End Interconnect Model Set]
- [Interconnect Model Set Group]/[End Interconnect Model Set Group] (New and changed from “Selector”)

Interconnect Hierarchy



[Interconnect Model Set]s [Interconnect Model Set Group]s (New)

- [Interconnect Model Set] <set_name>
  - Encapsulates one or more Interconnect Models
- [Interconnect Model Set Group] <group_name>
  - References one or more Interconnect Model Sets to be used together
  - Should be used to establish a complete path for selected buffers
  - <group_name> helps in identify the buffers that are selected for simulation
- Some Example Groupings and Applications
  - Separate groups: one per interface (e.g., memory, network)
  - Separate groups for coupled vs. single-line simulations
  - Different sets for different power delivery network complexities
    - *POWER connected at single pin, single buffer terminal*
    - *POWER connected through multiple pins, rails to individual buffer terminals*

[Interconnect Model]

- [Interconnect Model] <interconnect_model_name>
  - Connections between terminals with IBIS-ISS or Touchstone files
  - Terminal connection points at Buffer, Die pad, or Pin interfaces
  - Identifies rail or I/O terminals
  - Allows pin_name, signal_name, pad_name, or bus_label terminal qualifiers for rails (and pin_name for I/O terminals)
  - Identifies whether a coupled signal is only an aggressor or also "experiences" coupling from other sources

How package and on-die electrical information is generated and delivered today

<Terminal lines> Syntax

- All column entries on one line:

  <Terminal_number> <Terminal_type>
  <Terminal_type_qualifier> <Qualifier_entry>
  [Aggressor_Only]

- <Terminal_number> is IBIS-ISS node position or Touchstone port number

- Allowable <Terminal_type> names and associations next

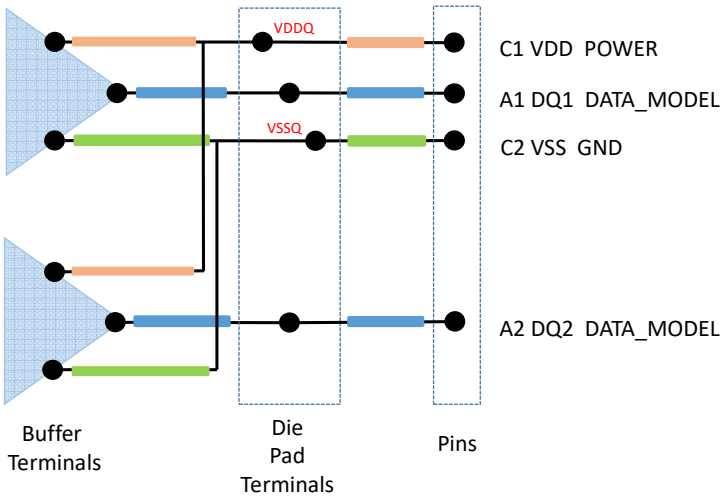
Allowable <Terminal_type> Associations

<Terminal_number> <Terminal_type> <Terminal_type_qualifier> <Qualifier_entry> [Aggressor_Only]

Terminal_type	Terminal_type_qualifier				Aggressor_Only
	pin_name	signal_name	bus_label	pad_name	
Pin_I/O	X				A
Pad_I/O	X				A
Buffer_I/O	X				A
Pin_Rail	Y	Y	Y		
Pad_Rail		Y	Y	Z	
Buffer_Rail		Y	Y		
Pullup_ref	X				
Pulldown_ref	X				
Power_clamp_ref	X				
Gnd_clamp_ref	X				
Ext_ref	X				

<Qualifier_entry>: "X" I/O pin_name; "Y," or "Z": POWER or GND name. Optional "A": "Aggressor_Only"

Example Showing Connections



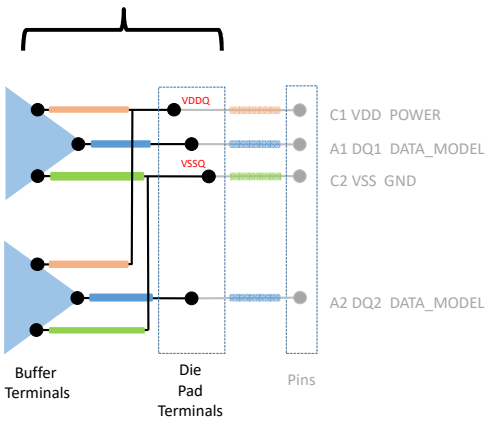
[Die Supply Pads] for pad_names Shown in Example

The [Die Supply Pads] keyword establishes pad_name <Qualifier_entries> for rails, and associates them with signal_name (and optionally with bus_label entries)

```
[Die Supply Pads] signal_name bus_label
| pad_name
VDDQ                VDD
VSSQ                VSS
```


[Interconnect Model] for Buffer-to-Die Pad Side

```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS        buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O        pin_name     A1 |  DQ1 (DQ signal)
2  Pad_I/O        pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref     pin_name     A1 |  VDD (POWER connection)
4  Pulldown_ref   pin_name     A1 |  VSS (GND connection)
5  Buffer_I/O     pin_name     A1 |  DQ1 (DQ signal)
6  Pullup_ref     pin_name     A2 |  VDD (POWER connection)
7  Pulldown_ref   pin_name     A2 |  VSS (GND connection)
8  Buffer_I/O     pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail       pad_name   VDDQ |  VDD  POWER
10 Pad_Rail       pad_name   VSSQ |  VSS  GND
|
[End Interconnect Model]
```



[Interconnect Model] for Buffer-to-Die Pad Side (Expanded)

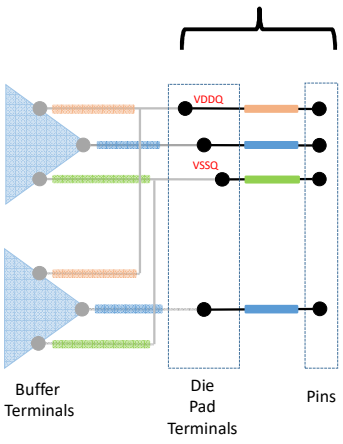
```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS        buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O        pin_name     A1 |  DQ1 (DQ signal)
2  Pad_I/O        pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref     pin_name     A1 |  VDD (POWER connection)
4  Pulldown_ref   pin_name     A1 |  VSS (GND connection)
5  Buffer_I/O     pin_name     A1 |  DQ1 (DQ signal)
6  Pullup_ref     pin_name     A2 |  VDD (POWER connection)
7  Pulldown_ref   pin_name     A2 |  VSS (GND connection)
8  Buffer_I/O     pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail       pad_name    VDDQ |  VDD  POWER
10 Pad_Rail       pad_name    VSSQ |  VSS  GND
|
[End Interconnect Model]
```

[Interconnect Model]

File and subcircuit

<Terminal lines> for connecting the subcircuit nodes (by position) to the interconnect structure

[Interconnect Model] for Die Pad-to-Pin Side




```
[Interconnect Model] Partial_ISS_pad_pin_2
|
File_IBIS-ISS        pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O    pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O    pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail   signal_name  VDD | VDD (POWER connection)
4  Pin_Rail   signal_name  VSS | VSS (GND connection)
5  Pad_I/O    pin_name      A1 | DQ1  (DQ signal)
6  Pad_I/O    pin_name      A2 | DQ2  (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail   pad_name    VDDQ | pad_name with VDD
8  Pad_Rail   pad_name    VSSQ | pad_name with VSS
|
[End Interconnect Model]
|
[End Interconnect Model Set]
```

[Interconnect Model] for Die Pad-to-Pin Side (Expanded)

[Interconnect Model]

File and subcircuit

<Terminal lines> for connecting the subcircuit nodes (by position) to the interconnect structure

```
[Interconnect Model] Partial_ISS_pad_pin_2
|
File_IBIS-ISS        pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O    pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O    pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail   signal_name  VDD | VDD (POWER connection)
4  Pin_Rail   signal_name  VSS | VSS (GND connection)
5  Pad_I/O    pin_name      A1 | DQ1  (DQ signal)
6  Pad_I/O    pin_name      A2 | DQ2  (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail   pad_name    VDDQ | pad_name with VDD
8  Pad_Rail   pad_name    VSSQ | pad_name with VSS
|
[End Interconnect Model]
|
[End Interconnect Model Set]
```


Complete [Interconnect Model Set] With Both [Interconnect Model]s

[Interconnect Model Set]

[Interconnect Model]s

```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS        buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O        pin_name     A1 |  DQ1 (DQ signal)
2  Pad_I/O        pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref     pin_name     A1 |  VDD (POWER connection)
4  Pulldown_ref   pin_name     A1 |  VSS (GND connection)
5  Buffer_I/O     pin_name     A1 |  DQ1 (DQ signal)
6  Pullup_ref     pin_name     A2 |  VDD (POWER connection)
7  Pulldown_ref   pin_name     A2 |  VSS (GND connection)
8  Buffer_I/O     pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail       pad_name   VDDQ |  VDD  POWER
10 Pad_Rail       pad_name   VSSQ |  VSS  GND
|
[End Interconnect Model]
```

```
[Interconnect Model] Partial_ISS_pad_pin_2
|
File_IBIS-ISS        pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O    pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O    pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail   signal_name  VDD | VDD (POWER connection)
4  Pin_Rail   signal_name  VSS | VSS (GND connection)
5  Pad_I/O    pin_name      A1 | DQ1  (DQ signal)
6  Pad_I/O    pin_name      A2 | DQ2  (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail   pad_name    VDDQ | VDD is signal name
8  Pad_Rail   pad_name    VSSQ | VSS is signal name
|
[End Interconnect Model]
|
[End Interconnect Model Set]
```

[End Interconnect Model Set]

[Interconnect Model Set Group] (New) for a Selected Group

```
[Interconnect Model Set Group]    A1_A2_PDN
|
| Interconnect Model Set Name     File_reference
Full_ISS_PDN                      NA
|
[End Interconnect Model Set Group]
```

[Interconnect Model Set Group] is at same level as [Package Model] for selected group of Buffer_IO pin(s)

Name should be descriptive for easy selection (e.g., A1-A2_PDN)

Can contain several references to [Interconnect Model Set]s

Sets can be in the .ibs file (NA) or in a separate directories

[Interconnect Model]s within a Group must be connected

File_TS, File_TS0 (New) Issue

- Touchstone files can now be documented with a single reference (File_TS) or ground “Node 0” reference (File_TS0)
  - Offering both choices eliminates issue about which is better
  - File_TS0 would not be used for power-aware simulations
- File_IBIS-ISS with S model can be used for more references, if needed

Touchstone Unused Port Termination

- Not an issue with IBIS-ISS – all terminal connections are required
- For Touchstone files
  - Unused_port_termination <Open | Reference>
  - Reference: reference impedance reduces the number of Touchstone ports through matrix reduction
  - Open: represents the physically disconnected port
  - EDA tools might still provide an interface to override the choices
- Other options still being discussed

Summary

- BIRD189.x improves IBIS package modeling
- Links IBIS, IBIS-ISS and Touchstone for package models
  - Adds flexible support for package loss, crosstalk and partitioning
- Formalizes and separates Die pads and Buffers
- Other extensions (not covered here) included

New advanced Interconnect format for IBIS Version 7.0!

Signal Integrity Analysis for 56G-PAM4 Channel of 400G Switch

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Asian IBIS Summit
Shanghai, PRC
November 13, 2017

Celestica™

Agenda

Think Bigger. Reach Further.

- Background
- 200GBASE-KR4
- 400GAUI-8 C2M/200GBASE-CR4
- CEI-56G-VSR-PAM4
- Conclusion

Background

Think Bigger. Reach Further.

- Celestica focuses on advanced switches, storage and server.
- The switch bandwidth is moving from 100G to 400G.
- Data rate is moving from 25 Gbps to 56 Gbps.

- 56G PAM4 SERDES
- 25G NRZ SERDES

Agenda

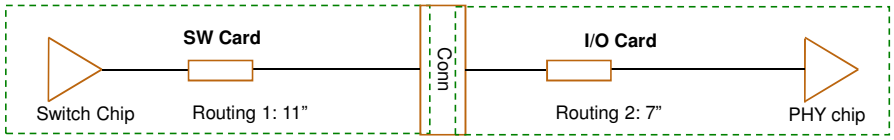
Think Bigger. Reach Further.

- Background
- 200GBASE-KR4
- 400GAUI-8 C2M/200GBASE-CR4
- CEI-56G-VSR-PAM4
- Conclusion

200GBASE-KR4- Channel Topology

Think Bigger. Reach Further.

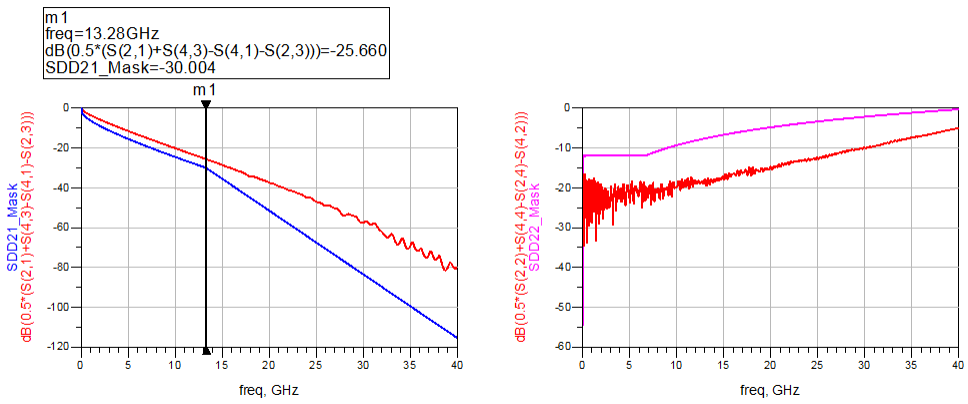
- This channel is between switch chip and PHY chip.



- Megtron 4 level material is used for the analysis.

200GBASE-KR4- Frequency Domain Simulation Results

Think Bigger. Reach Further.

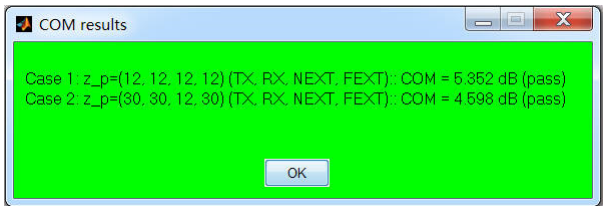


- The simulation results are shown above. The channel includes an 11 inch trace on the Switch Card, a 7 inch trace on the I/O Card and one connector. The channel can meet the 200GBASE-KR4 specifications of the passive channel requirements.

200GBASE-KR4- COM Simulation

Think Bigger. Reach Further.

- Consideration of the 9 FEXT and 8 NEXT crosstalk models to run the COM.
- The crosstalk considers the crosstalk in BGA area and the crosstalk in connector area.



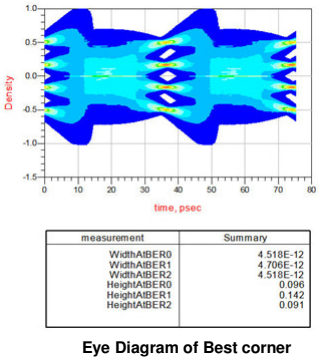
- Simulation results show that the 11 inch trace in Switch Card and 7 inch trace in I/O Card can pass the COM specification with default package model.

200GBASE-KR4- Time Domain Simulation Results(1)

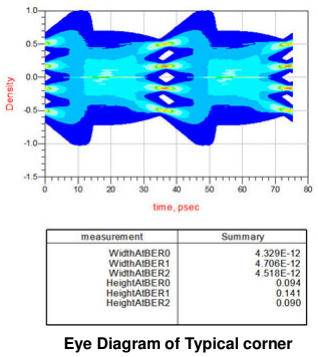
Think Bigger. Reach Further.

- The simulation settings and results are shown in the Table and Figure below. The channel is from switch chip to PHY chip.

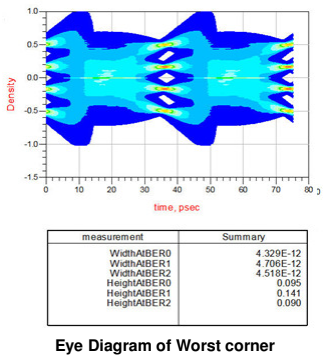
Trace Length	PVT Corner: Best Eye Width/Eye Height @BER=1e-6 in Sim	PVT Corner: Typical Eye Width/Eye Height @BER=1e-6 in Sim	PVT Corner: Worst Eye Width/Eye Height @BER=1e-6 in Sim
11inches in Switch Card and 7inches in I/O Card	4.52ps/96mV	4.33ps/95mV	4.33ps/141mV
	4.71ps/142mV	4.71ps/141mV	4.71ps/141mV
	4.52ps/91mV	4.52ps/90mV	4.52ps/90mV



Eye Diagram of Best corner



Eye Diagram of Typical corner



Eye Diagram of Worst corner

Simulation results show that the channel including total 18 inches of trace can support 53.125 Gbps data rate.

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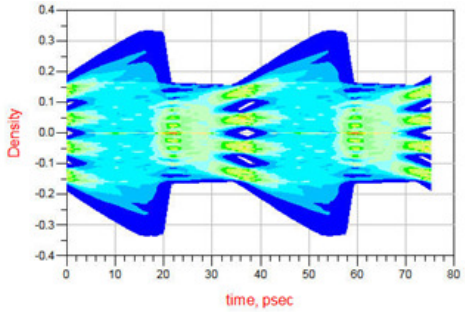
200GBASE-KR4- Time Domain Simulation Results(2)

Think Bigger. Reach Further.

- The simulation settings and results are shown in the Table and Figure below. The channel is from the PHY chip to switch chip.

Trace Length	PVT Corner: Worst Eye Width/Eye Height @BER=1e-4 in Sim
11inches in Switch Card and 7inches in I/O Card	2.64ps/5mV
	2.64ps/14mV
	2.45ps/5mV



measurement	Summary
WidthAtBER0	2.635E-12
WidthAtBER1	2.635E-12
WidthAtBER2	2.447E-12
HeightAtBER0	0.005
HeightAtBER1	0.014
HeightAtBER2	0.005

Eye Diagram of Worst corner

There is some issues with the time domain simulation of PHY TX and switch chip RX. Celestica is working with the chip vendor.

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Agenda

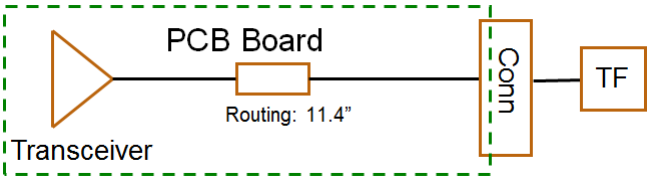
Think Bigger. Reach Further.

- Background
- 200GBASE-KR4
- 400GAUI-8 C2M/200GBASE-CR4
- CEI-56G-VSR-PAM4
- Conclusion

400GAUI-8 C2M/200GBASE-CR4- Interconnect Modeling

Think Bigger. Reach Further.

- The 400GAUI-8 C2M specification has defined the requirement from the host transmit to the test fixture. The topology is shown in the Figure below. Megtron 7 PCB material has been used in this channel.



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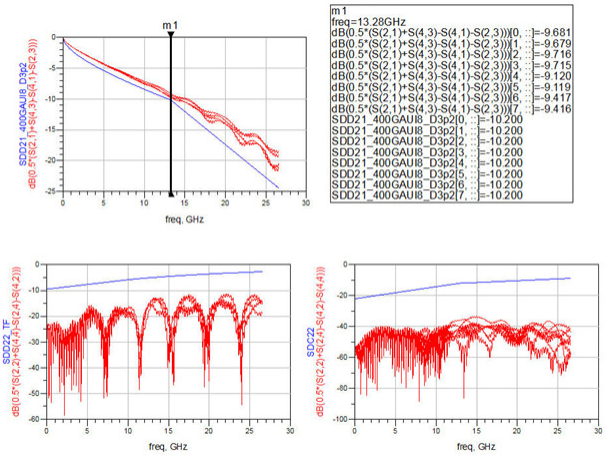
400GAUI-8 C2M/200GBASE-CR4- Host Channel Analysis in Frequency Domain

Think Bigger. Reach Further.



- Simulation results show that the channel, including 11.4 inches of trace, can meet the 400GAUI-8 C2M specification passive requirements.

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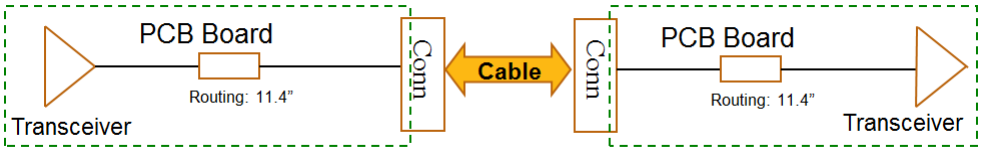
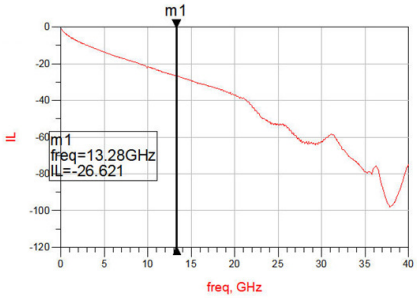
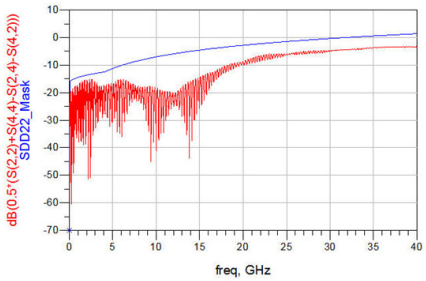
400GAUI-8 C2M/200GBASE-CR4
- Loopback Channel Analysis, Topology and 2.5m Cable)

Think Bigger. Reach Further.

- The copper cable loopback channel topology with 200GBASE-CR4 is shown below.







- Simulation results show the IL/RL of two 11.4 inch channels with a 2.5m 28AWG cable loop back can meet the 200GBASE-CR4 specification passive requirements.

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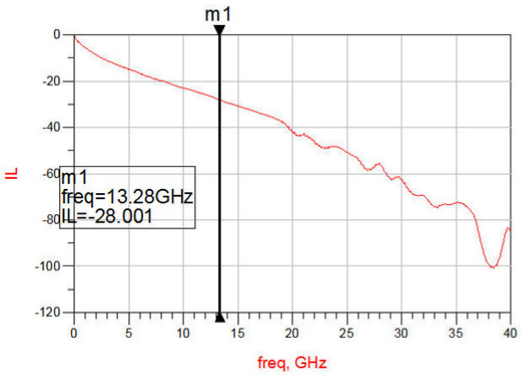
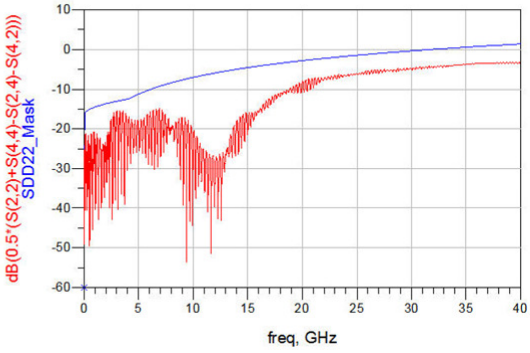
400GAUI-8 C2M/200GBASE-CR4
- Loopback Channel Analysis, 3m Cable

Think Bigger. Reach Further.





- Simulation results show the IL/RL of two 11.4 inch channels with **3m 28AWG** cable loop back can meet the 200GBASE-CR4 specification passive requirements.

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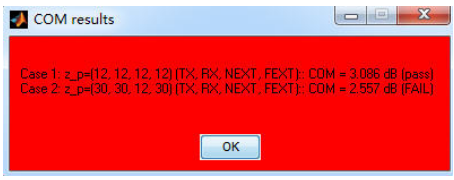
400GAUI-8 C2M/200GBASE-CR4
- Loopback Channel Analysis, COM, 3m

Think Bigger. Reach Further.

- The channel margin shall be greater than or equal to 3dB after COM calculation for 200GBASE-CR4 Channel.
- 9 aggressor FEXT channels and 8 aggressor NEXT channels on both side of the victim channel are considered for the COM crosstalk analysis. The major contributors to crosstalk such as traces, vias, cable paddle card are considered for the crosstalk modeling. The detailed trace modeling with crosstalk is shown below.



- Simulation results show that the channel including two 11.4 inch traces with **3m 28AWG** QSFP-DD cable assembly, Case1 can pass and Case2 cannot meet the IEEE802.3cd Specification COM requirement for 200GBASE-CR4 based on the default package S parameters.

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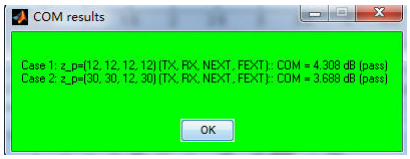
400GAUI-8 C2M/200GBASE-CR4- Loopback Channel Analysis (COM, 2.5m)

Think Bigger. Reach Further.



- Simulation results show that the channel including two 11.4 inch traces with the **2.5m 28AWG** QSFP-DD cable assembly, can meet the IEEE802.3cd/D2.2 Specification COM requirement for 200GBASE-CR4 based on the default package S parameters for both cases.

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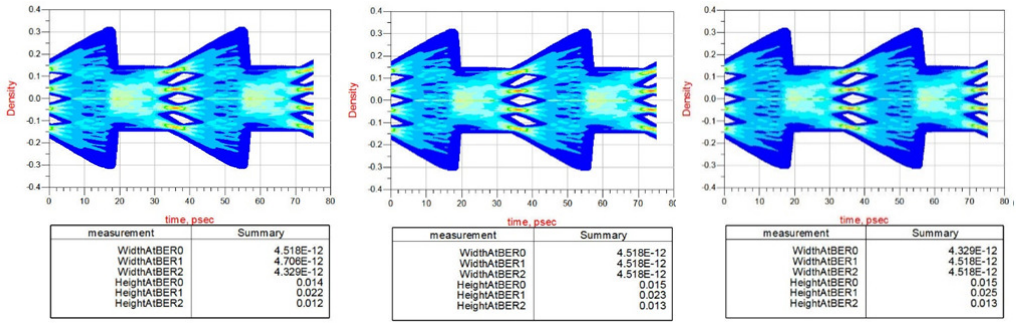
400GAUI-8 C2M/200GBASE-CR4
- Loopback Channel Time Domain Analysis

Think Bigger. Reach Further.

- The simulation settings and results are shown in the Table and Figure below.

Trace Length	Cable	PVT Corner: Best Eye Width/Eye Height @BER=1e-6 in Sim	PVT Corner: Typical Eye Width/Eye Height @BER=1e-6 in Sim	PVT Corner: Worst Eye Width/Eye Height @BER=1e-6 in Sim
11.4inch	3m 28AWG	4.52ps/14mV	4.52ps/14mV	4.52ps/14mV
		4.71ps/22mV	4.71ps/22mV	4.71ps/22mV
		4.33ps/12mV	4.33ps/12mV	4.33ps/12mV



Eye Diagram of Best corner | **Eye Diagram of Typical corner** | **Eye Diagram of Worst corner**

Simulation results show that the channel including two 11.4 inch traces can support the 3m 28AWG QSFP-DD cable for 53.125G rate.

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Agenda

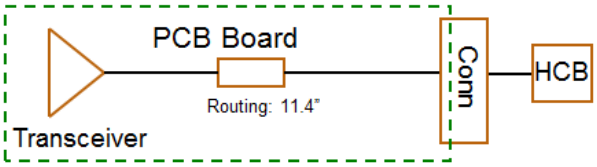
Think Bigger. Reach Further.

- Background
- 200GBASE-KR4
- 400GAUI-8 C2M/200GBASE-CR4
- CEI-56G-VSR-PAM4
- Conclusion

CEI-56G-VSR-PAM4
- Interconnect Modeling

Think Bigger. Reach Further.

- The CEI-56G-PAM4-VSR specification defines the requirement from the host transmit to the external IO connector. The topology is shown in the Figure below. Megtron 7 PCB material has been used in this channel. Note that from Host PCB to Connector insertion loss is up to 8.5 dB.



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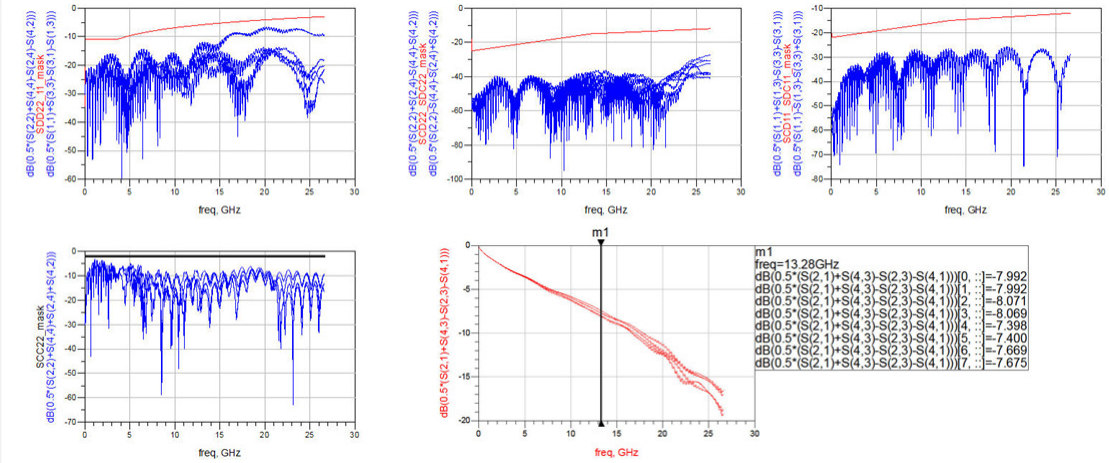
CEI-56G-VSR-PAM4 S
- Host Channel Analysis in Frequency Domain

Think Bigger. Reach Further.



- Simulation results show that the channel including an 11.4 inch trace with one connector can meet the passive requirement of the CEI-56G-VSR-PAM4 specifications.

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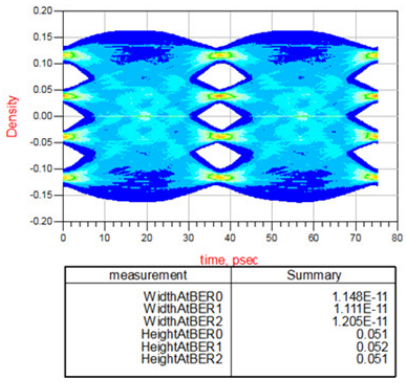
CEI-56G-VSR-PAM4
- Host Channel Analysis in Time Domain

Think Bigger. Reach Further.

- The simulation results are shown in the table below.

Trace Length	Eye Width/Eye Height (@BER=1e-6 in Sim)	Eye Width/ Eye Height (@BER=1e-6 in spec)
11.4 inches	11.48ps/51mV	>=8.28ps/35 mV
	11.11ps/52mV	
	12.05ps/51mV	



measurement	Summary
WidthAtBER0	1.148E-11
WidthAtBER1	1.111E-11
WidthAtBER2	1.205E-11
HeightAtBER0	0.051
HeightAtBER1	0.052
HeightAtBER2	0.051

- Simulation results show that the channel including a 11.4 inch trace with one connector can meet the eye height requirement of the CEI-56G-VSR-PAM4 specification at TP1a.

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Think PAM4 Serdes

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Asian IBIS Summit
Shanghai, PRC
November 13, 2017

HUAWEI TECHNOLOGIES CO., LTD.

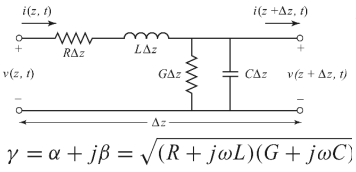
HUAWEI

Outline

- **Introduction of loss TL**
- **PAM4 Serdes Architecture**
- **CTLE characteristics and response**
- **FFE characteristics and response**
- **FFE parameter optimization and taps selection**
- **FFE defects and the advantages of DFE**
- **PAM4 Serdes Simulation with IBIS-AMI**
- **Summary**

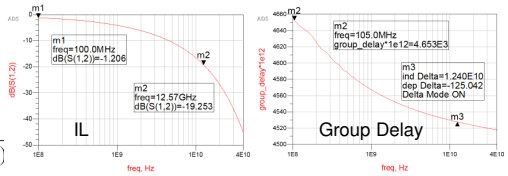
Lossy TL and ISI

- **Characteristics of Lossy Transmission Line**



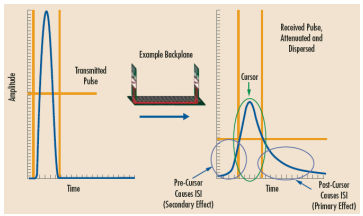
$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

RLGC are frequency dependent

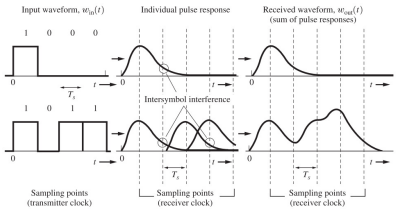


IL and Group Delay are frequency dependent

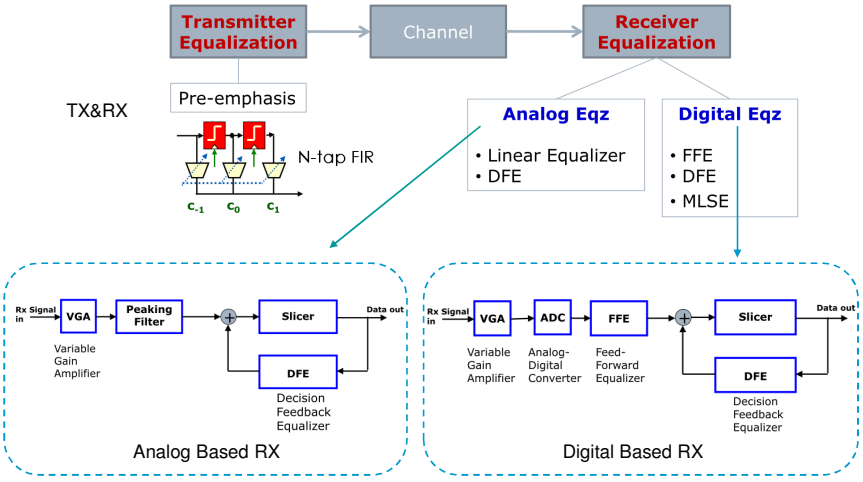
- **ISI: Channel is band limited, pulse width expands**



ISI



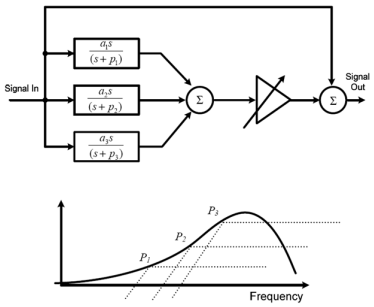
PAM4 Serdes Architecture*



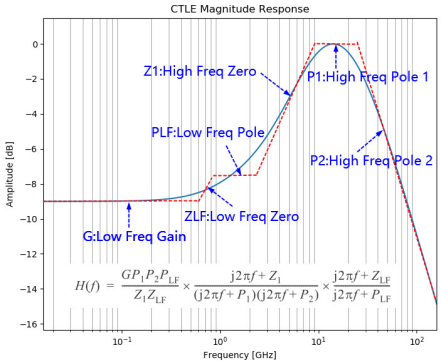
[*: Vivek Telang, Equalization for High-Speed Serdes Systems – A System-level Comparison of Analog and Digital Techniques, IEEE SSCS Technical Seminar, Friday, August 10, 2012]

CTLE Frequency Response

- **CTLE：High-Pass Filter**
  - The locations of Zeros and Poles determine frequency response
  - Zero: Rise at 20dB/decade
  - Pole: Drop at 20dB/decade



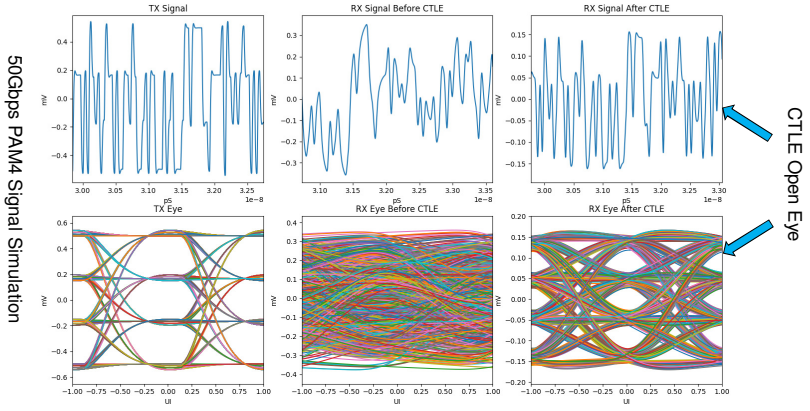
Typical CTLE



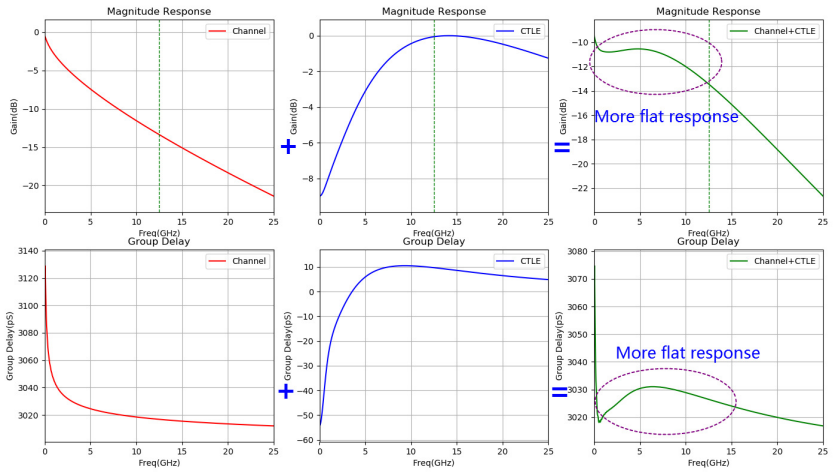
Reference CTLE in 802.3bs

Lossy Channel with CTLE-Time Domain

TX(NO EQ) → Channel(Loss=13dB) → RX(CTLE Gain=9dB)



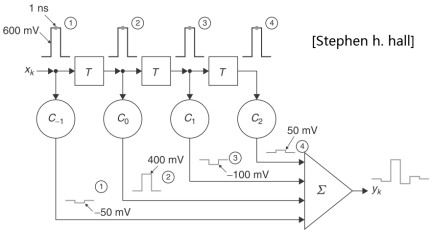
Lossy Channel with CTLE-Frequency Domain

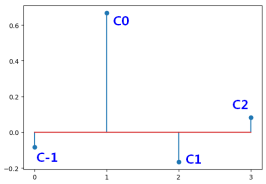


CTLE makes in-band response more flat

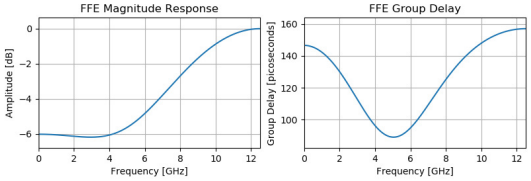
FFE and Its Response

Typical 4-Tap FFE
C-1=-1/12
C0=2/3
C1=-1/6
C2=1/12





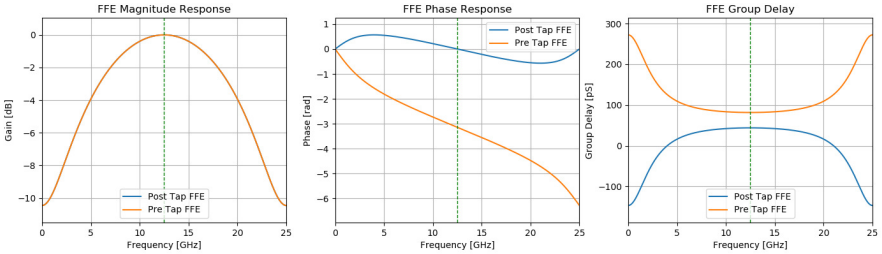
Impulse Response



Frequency Domain Response

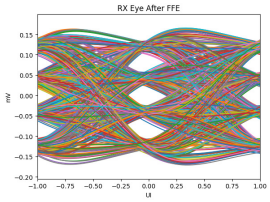
Post Tap versus Pre Tap

- **Post Tap FFE: [0.65, -0.35], Pre Tap FFE: [-0.35, 0.65]**
- **Gain= 20*log(1/0.3)=10.4dB to reach peak gain at Nyquist frequency**
- **Different phase response and group delay**

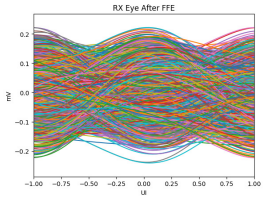


Tap coefficients of FFE

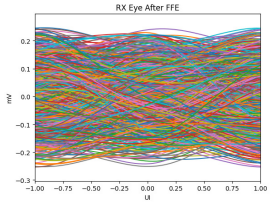
- **Same TX and Channel but different RX FFE**



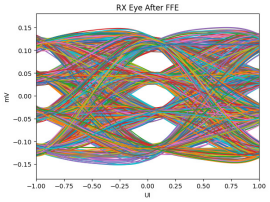
FFE=[0.65, -0.35]



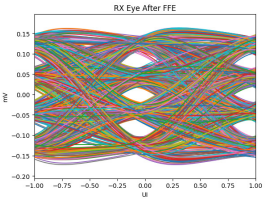
FFE=[-0.35, 0.65]



FFE=[0.65, 0, -0.35]



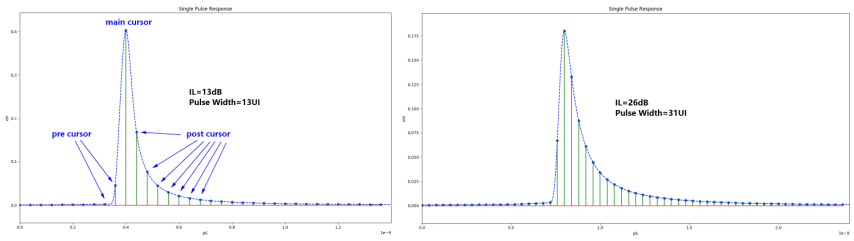
FFE=[-0.1, 0.65, -0.25]



FFE=[0.65, -0.3, -0.05]

How many taps are enough?
How to choose tap values?

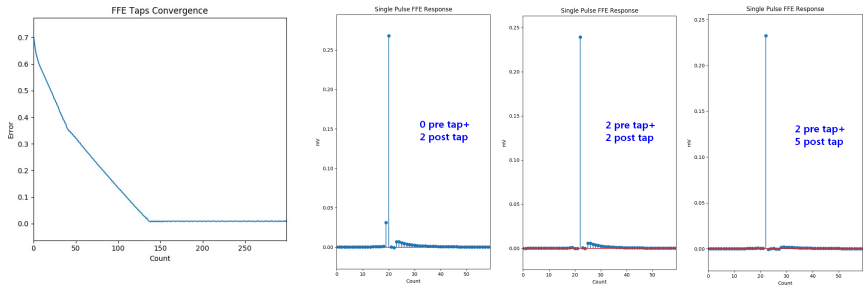
Single Pulse Response of Channel



- **The greater loss of the channel produces a lower pulse response amplitude and a greater pulse width**
- **When Σ(|pre cursor|+|post cursor|)>main cursor, eye closed**

How to choose FFE tap values?

- **Adaptive FFE**
  - ZF: Zero-Forcing
  - LMS: Least Mean Square

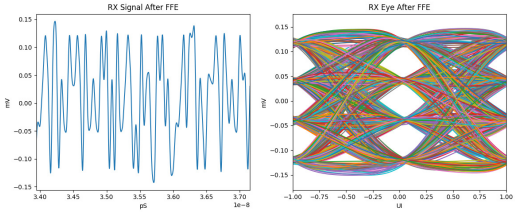


FFE coefficient convergence

Different number of taps

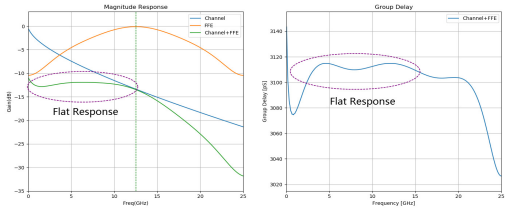
Time-frequency Response of Optimized FFE

TX(NO EQ) → Channel(LOSS=13dB) → RX(FFE,1 pre+3 post)



Time Domain Simulation

The optimal taps coefficient produce the best received eye

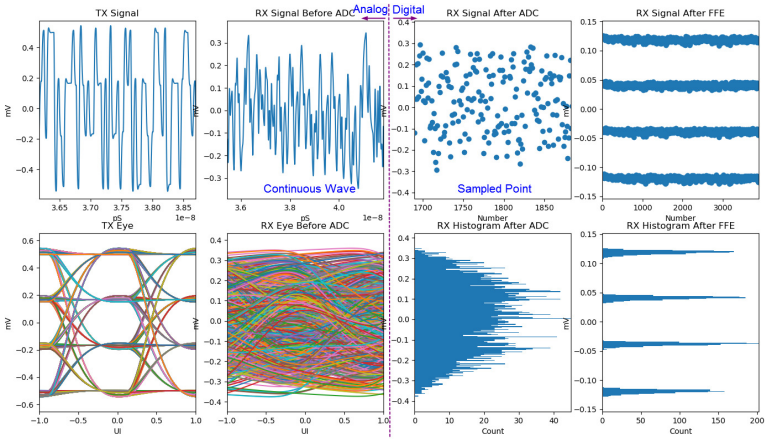


Frequency Domain Simulation

Multi-Taps FFE can do fine tuning of gain and phase

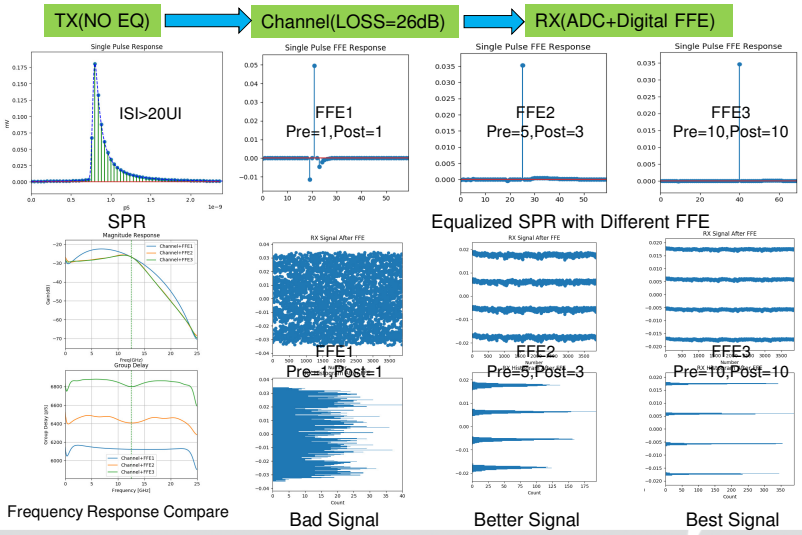
Digital Based FFE

TX(NO EQ) → Channel(LOSS=13dB) → RX(ADC+FFE,1 pre+3 post)

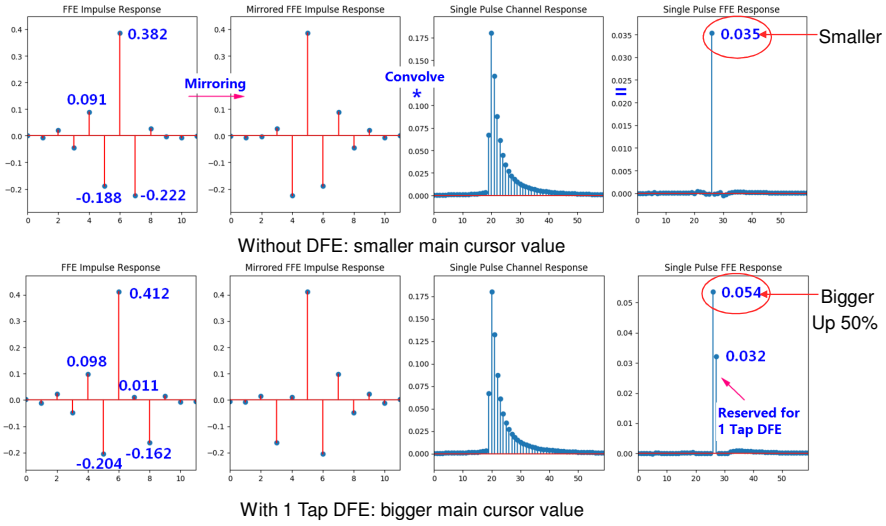


TX Signal | RX Input Signal | ADC Sampled Signal | Equalized Signal

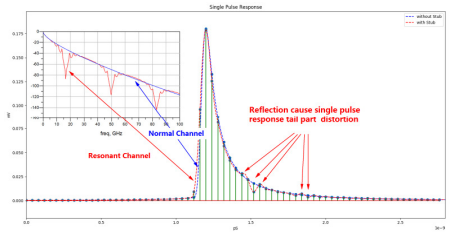
How many FFE taps are enough?

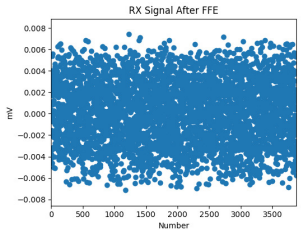


The Unique Value of DFE

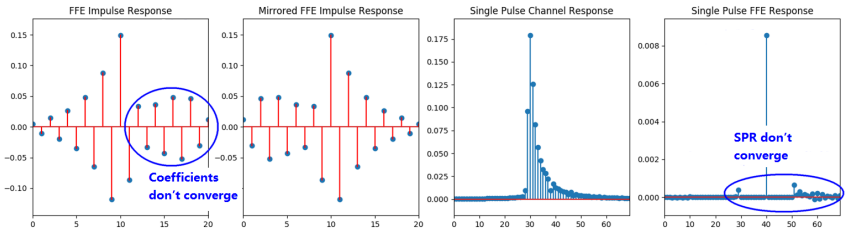


The Dead Zone of FFE



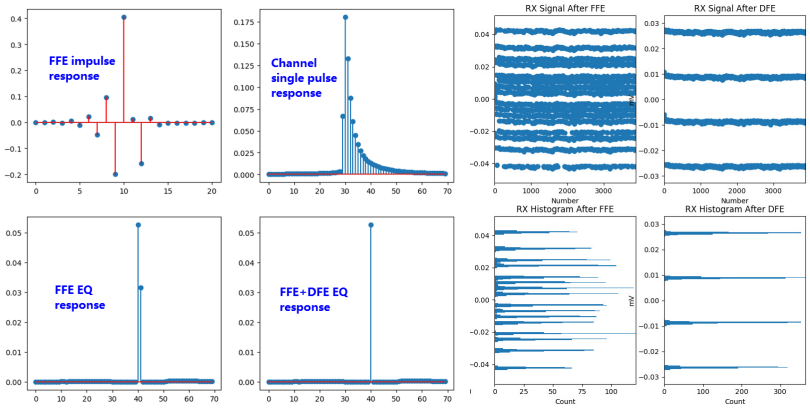


SPR Compare



FFE Can 't Recover Signal from Resonant Channel

Multi-Tap FFE + 1 Tap DFE Simulation



Single Pulse Response Full Channel Simulation

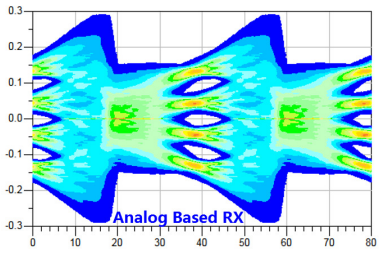
By adding1-tap DFE, the amplitude of equalized signal increases by 50%. For high-loss long-distance channel, RX with DFE is very important.

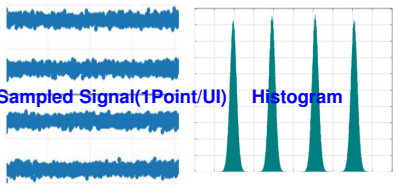
PAM4 Serdes Simulation with IBIS-AMI

```
AMI_GetWave (double *wave,
 long wave_size,
 double *clock_times,
 char **AMI_parameters_out,
 void *AMI_memory)
```

Time Domain Waveform

IBIS-AMI API





Digital Based RX

Summary

- **With the arrival of the PAM4 Serdes, more receivers change from analog architecture to digital architecture**
- **Digital based RX can leverage DSP technology, but RX becomes more complicated**
- **The current IBIS-AMI specification is suited for analog based RX, but lacks support for the digital architectures**
- **IBIS-AMI is a type of “black box” model that hides the signal of the internal nodes**
- **Need a more general PAM4 simulator to support digital RX (adc, adaptive dsp, cdr, snr, ser, ber, fec, etc.)**
- **This presentation illustrates the need**

Thank you

www.huawei.com

Comparison of Time Domain and Statistical IBIS-AMI Analyses

Mike LaBonte
SiSoft

Asian IBIS Summit 2017
Shanghai, PRC
November 13, 2017

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9 Combinations of TX and RX Model Types

- AMI file has:
  - GetWave_Exists = True — Best for bit-by-bit simulation
  - Init_Returns_Impulse = True — Best for statistical analysis
  - 3 types: “Init-only”, “GetWave-only”, “Dual”
  - 3 TX * 3 RX = 9 combinations

Case #	TX			RX			Convolution Input	Statistical	Time Domain
	Getwave Exists	**Init_Returns_Impulse**	**Meaning**	**Getwave Exists**	**Init_Returns_Impulse**	**Meaning**			
1	FALSE	TRUE	Init-Only	FALSE	TRUE	Init-Only	3	OK	Static TX EQ, Static RX Eq
2	FALSE	TRUE	Init-Only	TRUE	FALSE	Getwave-Only	1 or 2	No RX EQ	Static TX EQ, Dynamic RX Eq
3	FALSE	TRUE	Init-Only	TRUE	TRUE	Dual	2	OK	Static TX EQ, Dynamic RX Eq
4	TRUE	FALSE	Getwave-Only	FALSE	TRUE	Init-Only	3	No TX EQ	Dynamic TX EQ, Static RX EQ
5	TRUE	FALSE	Getwave-Only	TRUE	FALSE	Getwave-Only	1,2,or 3	No TX or RX EQ	Dynamic TX EQ, Dynamic RX EQ
6	TRUE	FALSE	Getwave-Only	TRUE	TRUE	Dual	1	No TX EQ	Dynamic TX EQ, Dynamic RX EQ
7	TRUE	TRUE	Dual	FALSE	TRUE	Init-Only	iFFT(FFT(3)/FFT(2))	OK	Dynamic TX EQ, Static RX EQ
8	TRUE	TRUE	Dual	TRUE	FALSE	Getwave-Only	1	No RX EQ	Dynamic TX EQ, Dynamic RX EQ
9	TRUE	TRUE	Dual	TRUE	TRUE	Dual	1	OK	Dynamic TX EQ, Dynamic RX EQ

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Simulation limitations

	Correct equalization of TX and RX modeled
	Correct equalization of TX and RX modeled: Assumes no adaptation in TX
	Assumes Static RX Equalization is a good representation of the RX: No adaptation
	Assumes Static RX EQ is a good representation of the RX: No Adaptation, Requires advanced math capabilities in Simulator
	Equalization data is missing

Case #	TX	RX	Statistical	Time Domain
1	Init Model Only	Init Model Only	OK	Static TX EQ, Static RX EQ
2	Init Model Only	Getwave Model Only	No RX EQ	Static TX EQ, Dynamic RX EQ
3	Init Model Only	Dual Model	OK	Static TX EQ, Dynamic RX EQ
4	Getwave Model Only	Init Model Only	No TX EQ	Dynamic TX EQ, Static RX EQ
5	Getwave Model Only	Getwave Model Only	No TX or RX EQ	Dynamic TX EQ, Dynamic RX EQ
6	Getwave Model Only	Dual Model	No TX EQ	Dynamic TX EQ, Dynamic RX EQ
7	Dual Model	Init Model Only	OK	Dynamic TX EQ, Static RX EQ
8	Dual Model	Getwave Model Only	No RX EQ	Dynamic TX EQ, Dynamic RX EQ
9	Dual Model	Dual Model	OK	Dynamic TX EQ, Dynamic RX EQ

Best Option

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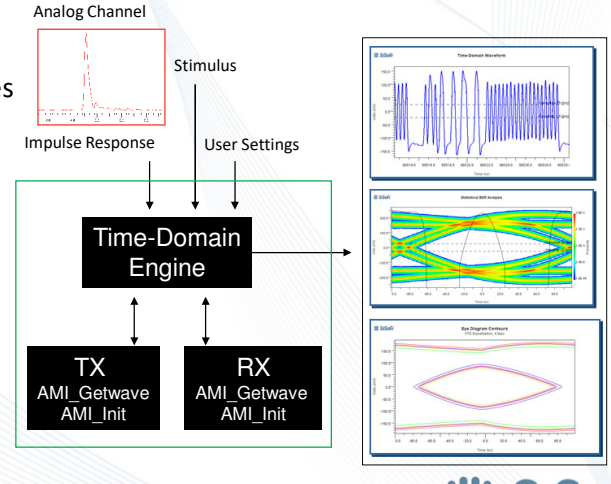
Time-Domain Simulation

- **Inputs:**
  - Channel and buffer Impulse responses
  - User-defined input stimulus
  - Algorithmic models (AMI_GetWave)
- **Analysis Method:**
  - Waveform processing & convolution
- **Outputs:**
  - Bit pattern waveforms
  - Persistent eye diagrams
  - Eye height / width measurements
  - Eye contours @ probabilities
  - Equalized / unequalized responses



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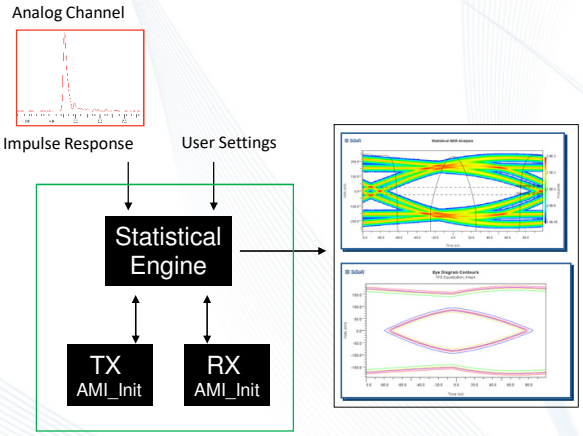
Statistical Simulation

- **Inputs:**
  - Analog channel impulse response
  - User selections for model parameters
  - Algorithmic models (AMI_Init / impulse response processing)
- **Analysis Method:**
  - Convolution engine (pulse response)
- **Outputs:**
  - Statistical eye diagrams
  - Eye height / width measurements
  - Eye contours @ probabilities
  - Equalized / unequalized responses



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Which IBIS-AMI Model Type is Best?

- Need to evaluate suitability for modeling:
  - Impairments: The factors that harm the signal
    - Mostly in the channel
    - Statistical analysis has advantages
  - Corrective measures: Signal improvements
    - Mostly inside the SerDes
    - Time domain has advantages

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Impairments To Be Modeled

Amplitude Impairment	Physical Cause
Inter-symbol interference (ISI)	Signal distortion (linear and nonlinear)
Crosstalk	Electromagnetic coupling in passive interconnect
Receiver sensitivity	Low signal amplitude causes decision latch to fail clock-data timing
Additive White Gaussian Noise (AWGN)	Shot noise in receiver amplifiers

Clock Impairment	Physical Cause
Random Jitter (RJ)	a. Shot noise in oscillator gain element b. Power supply noise modulating gate delays
Duty Cycle Distortion (clock) (DCD)	For half rate clock, duration difference between positive and negative half cycles
Duty Cycle Distortion (data)	Difference between data rise and fall times
Sinusoidal Jitter (SJ)	Clock noise on power supply modulating gate delays

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Corrective Measures To Be Modeled

Corrective Measure	Time Domain Behavior
TX FFE	May adapt in time domain, but this is rare
RX CTLE	Linear, time-invariant (LTI)
RX AGC	Adapts in time domain
RX Saturation	Not adaptive, but not time-invariant either
RX DFE	Adapts in time domain
Others…	

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Inter-Symbol Interference (ISI) Impairments

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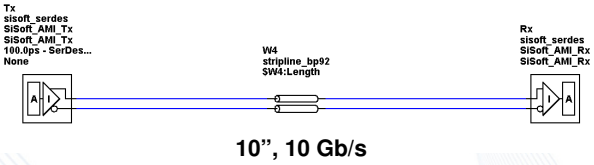
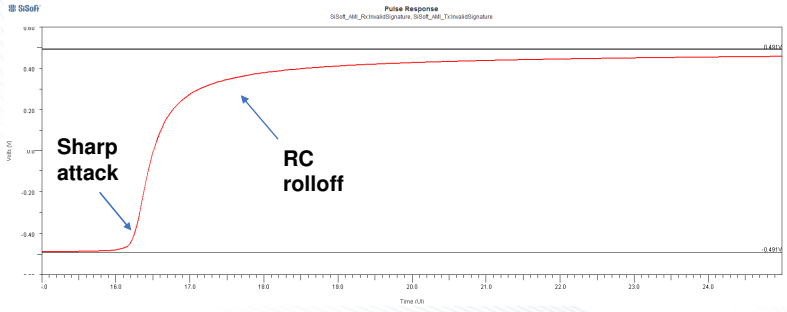
Step Response Analysis



10", 10 Gb/s



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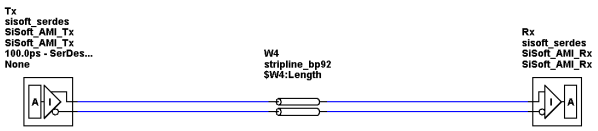
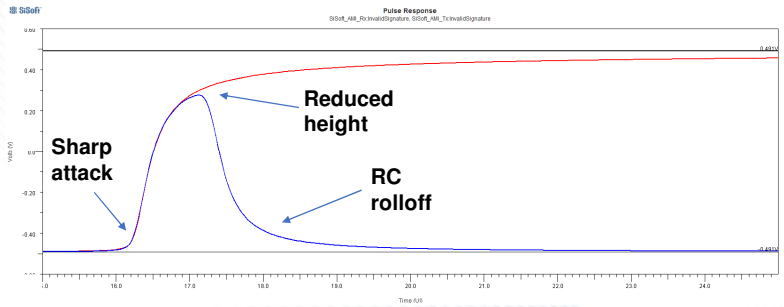
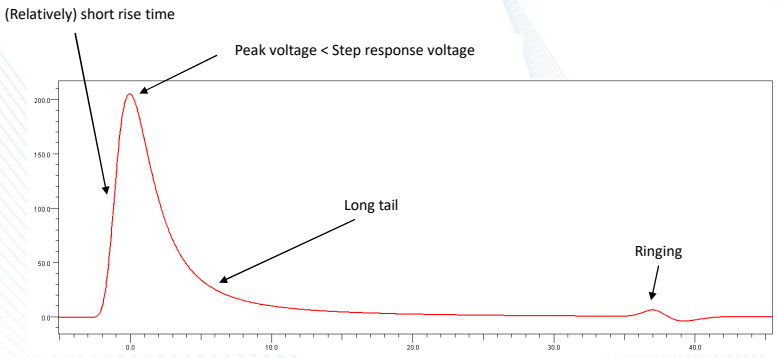
Pulse vs. Step Responses



10", 10 Gb/s



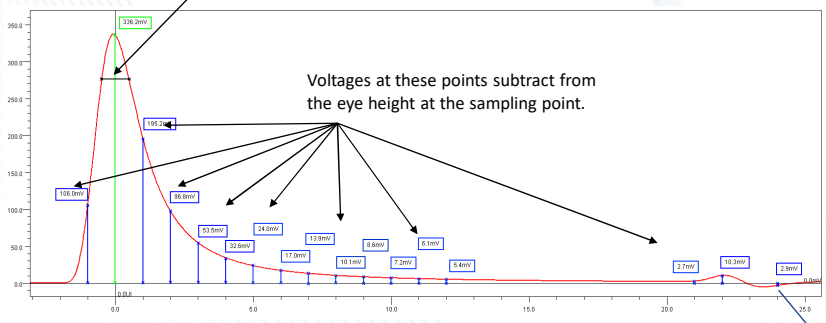
Channel Pulse Response



- Requires accurate Tx/Rx analog models to correctly predict ringing impairment due to reflections

Aligned Pulse Response and ISI

Hula hoop algorithm determines clock sampling time and main cursor height.
This is the maximum possible inner eye height.



$$Inner\ Eye\ Height = \text{main\_cursor} - \Sigma\,|\text{ISI\_voltages}|$$

- Voltage and time scales show ISI contributions
- Useful in evaluating EQ & predicting eye opening

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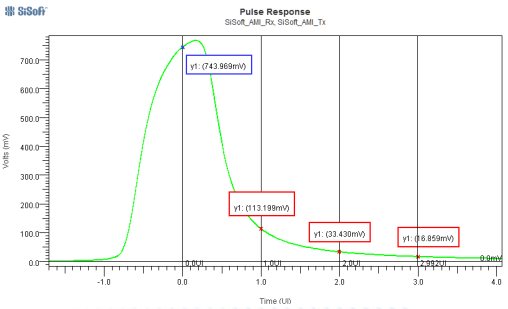
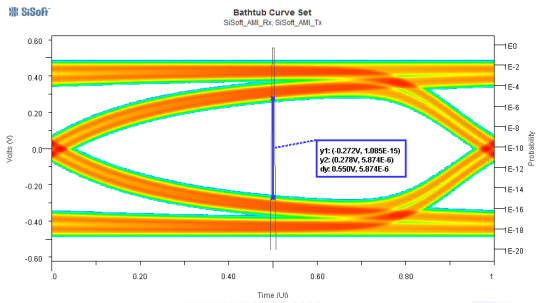
Statistical ISI Inner Eye Quick Calculation



Prediction: 580mV



Simulated Actual: 550mV

$$Inner\ Eye\ Height = \text{main\_cursor} - \Sigma\,|\text{ISI\_voltages}|$$

A quick calculation gets us close, but small amounts of energy in the tail add up

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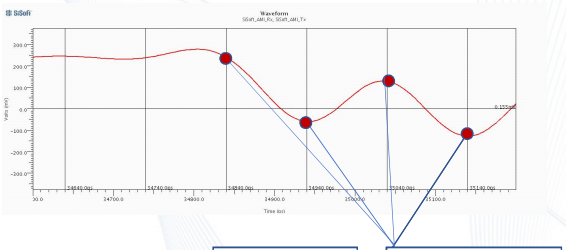
Time Domain ISI

- Time domain waveform from impulse response
- Bit pattern modulated
- Linear superposition
- LTI assumed

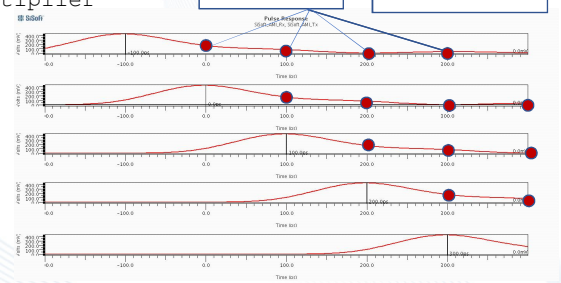
Example bit pattern: 11010



ISI here

Shows up here

Data		Multiplier
1	x	0.5
1	x	0.5
0	x	-0.5
1	x	0.5
0	x	-0.5



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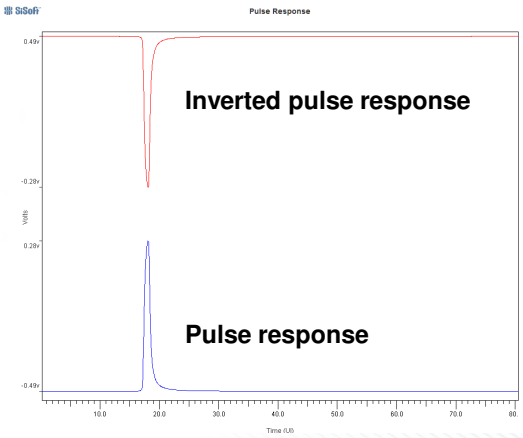
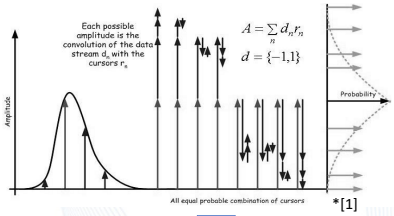
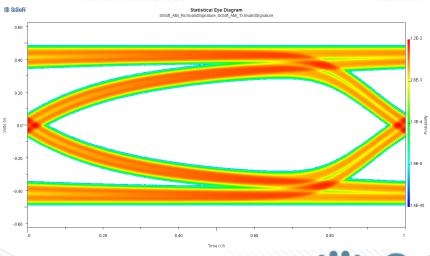
Statistical ISI





*[1]



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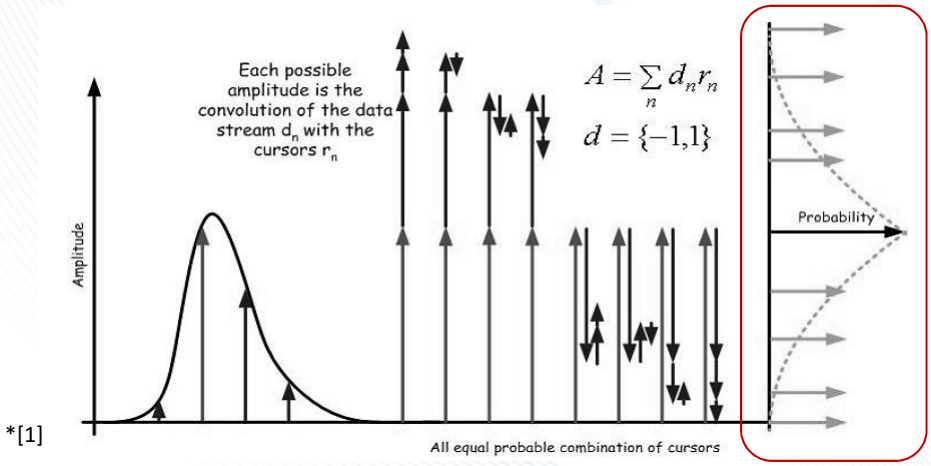
All Possible LTI Combinations Evaluated



*[1]

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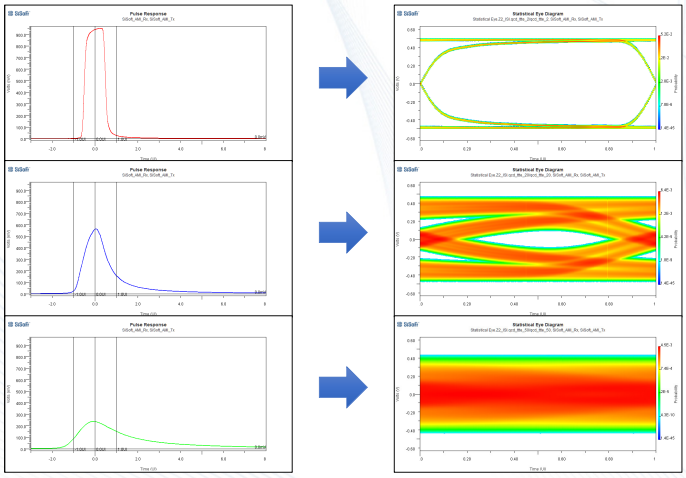
Channels, Pulses and Statistical Eyes

Short channel, Minimal ISI

Medium channel, Moderate ISI

Long channel, Extreme ISI



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Accounting for All ISI Scenarios

- A 28Gbps link may have a bit every 0.2 inches
- Many bits can be on the channel at once
- With reflections that number is multiplied
- Required impulse response may be many UI in length
- The bit pattern affects how these interact

To completely model all possible ISI scenarios we must try every possible bit pattern for the number of UI needed to capture all significant ISI

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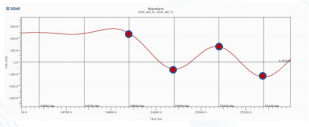
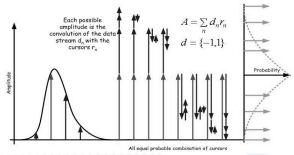
Can We Account for All ISI Scenarios?

- Theoretically need to try 2^N patterns, where N is the number of UI before ISI becomes insignificant
  - Example: 24 UI NRZ impulse response must simulate 2^{24} = 16,777,216 patterns, each 24 UI in length, total of 402,653,184 bit computations
- Time domain simulation
  - N-length patterns tested sequentially
  - PRBS helps reduce redundancies
  - Often able to simulate only a fraction of cursor combinations
- Statistical analysis
  - Able to directly calculate all 2^N cursor combinations
  - Efficient computation of channel response, not a circuit
  - May still have a practical upper limit for N





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Jitter and Noise Impairments

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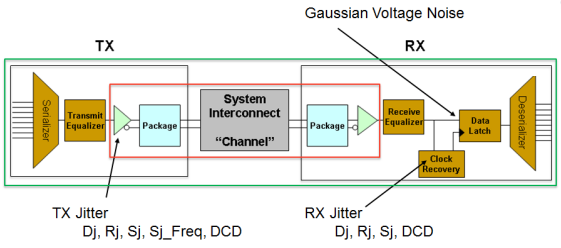
Jitter and Noise in IBIS-AMI

- IBIS 6.1 provides multiple TX & RX impairments
- TX jitter directly modulates the TX output
  - Simulators jitter the stimulus pattern sent to the TX in time domain simulations
  - Statistical analysis convolves jitter with eye diagram
- RX jitter affects recovered clock behavior
  - Simulators combine jitter data with clock information returned by the RX
  - Statistical analysis convolves jitter with eye diagram
- RX noise affects sampling latch data input
- **Jitter and noise are handled by the simulator, not by the models**



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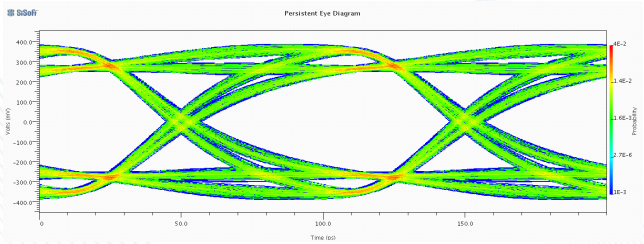
Time Domain Eyes With and Without Tx Jitter

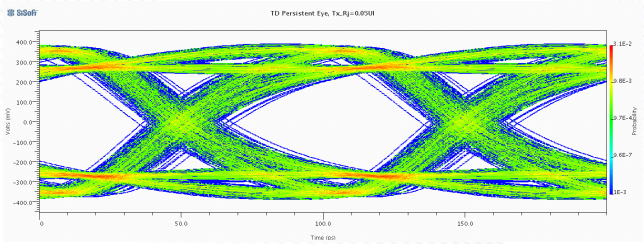
Random Jitter
(Tx_Rj) = 0



Only Impairment is Inter-Symbol Interference (ISI)

1e-3

Tx_Rj = 0.05UI



ISI + Jitter

1e-3

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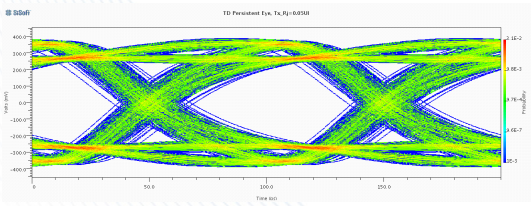
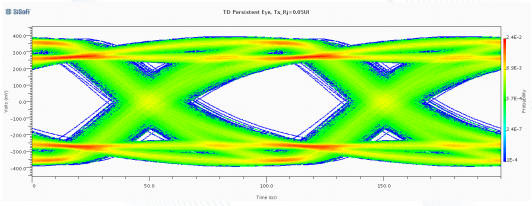
Time Domain: How Many Bits to Simulate?

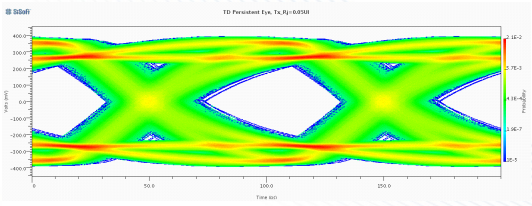
1,000 UI



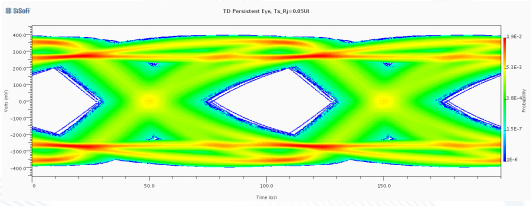
10,000 UI



100,000 UI



1,000,000 UI



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What Maximum BER Can We Tolerate?

• IEEE-802.3bj-KR4 FEC on	1e-5	
• IEEE-802.3bj-KR4 FEC off	**1e-12**	if low latency required
• OIF-CEI-56G FEC on	1e-4	
• OIF-CEI-56G FEC off	**1e-20**	
• PCIe-G3	**1e-12**	
• PCIe-G4	**1e-12**	
• DDR4	**1e-12**	eye mask rules
• DDR5	TBD	

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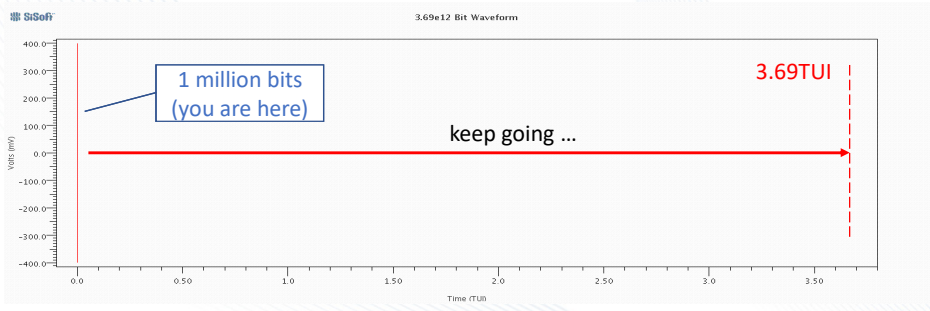
How Many Error-Free Bits for 1e-12 BER?

It's Not 1e12

Confidence Level	90%	95%	99%
Maximum BER	1e-12	1e-12	1e-12
Error-free Bits Simulated *[2]	3.00e12	3.69e12	5.30e12



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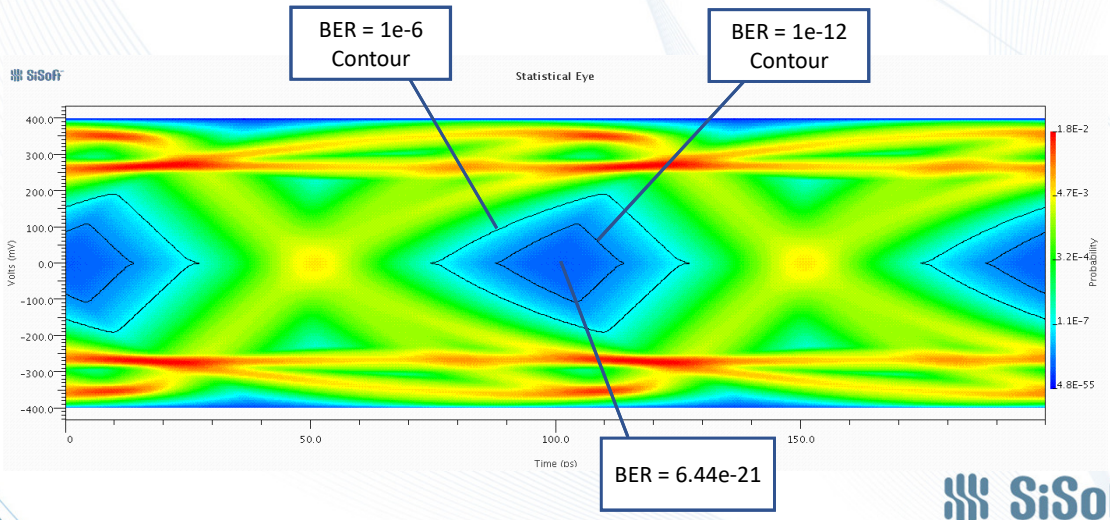
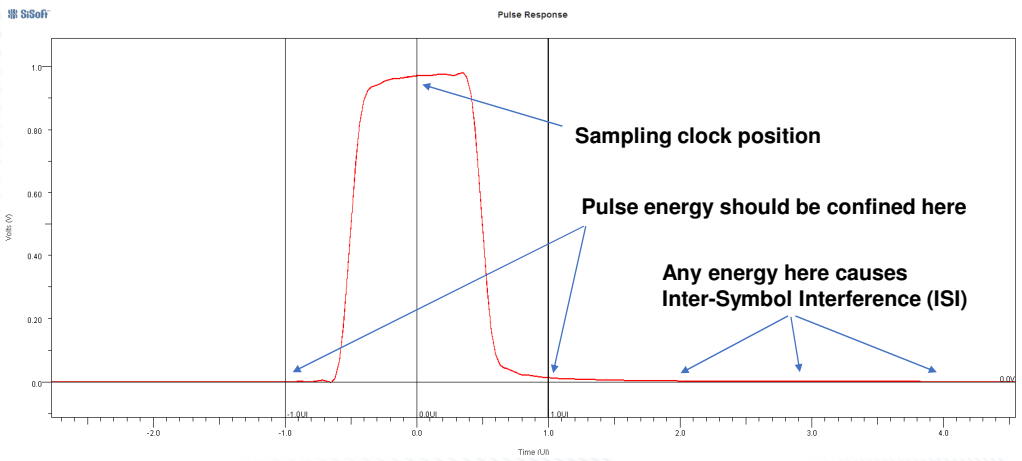
Statistical Eye With ISI and Jitter

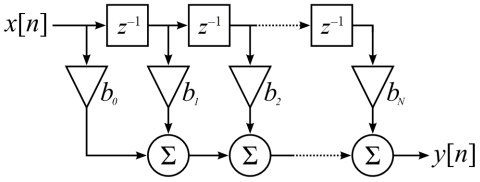


Tx Corrective Measures

Desired Pulse Response for Low ISI



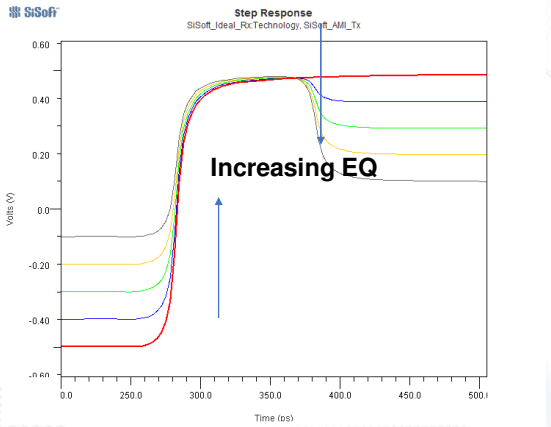
Tx Feed-Forward Equalization (FFE)



- Usually implemented as taps spaced at the signal data rate
- Can precede the signal (pre-cursor), follow the signal (post-cursor), or both
- Typical configuration is 1 pre-cursor, 2 post-cursor taps

TX FFE Equalization (1st post-cursor)

- Goal: boost high frequency content
- Transition occurs at full strength, then driver "pulls back" for subsequent bits
- TX EQ is often referred to as de-emphasis
- TX EQ always reduces the energy sent into the channel



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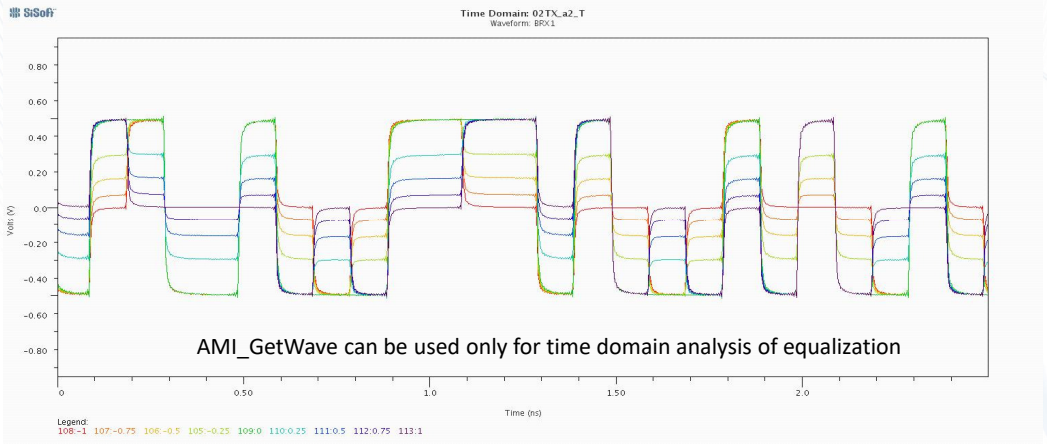
AMI_GetWave Models Can Process Equalization Directly in Time Domain



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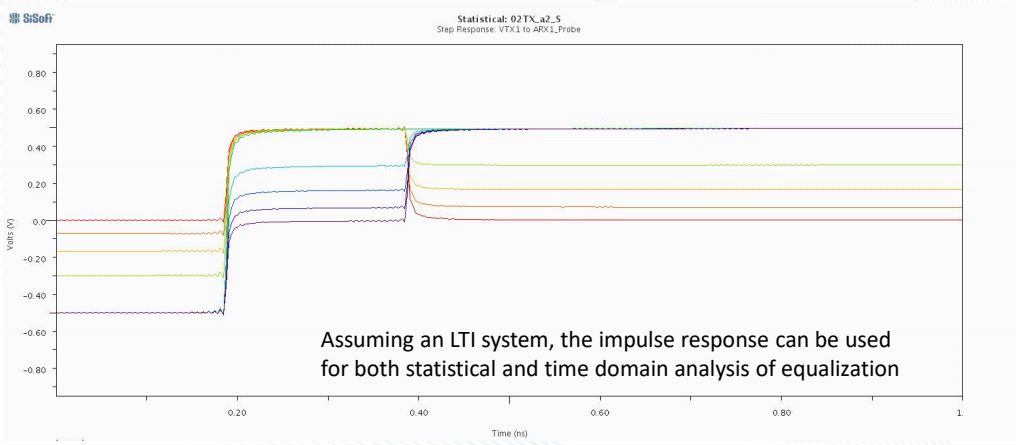
AMI_Init Can Return Impulse Response for Equalization



Assuming an LTI system, the impulse response can be used for both statistical and time domain analysis of equalization

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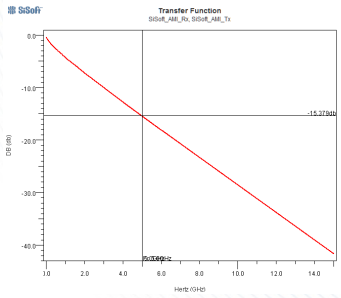
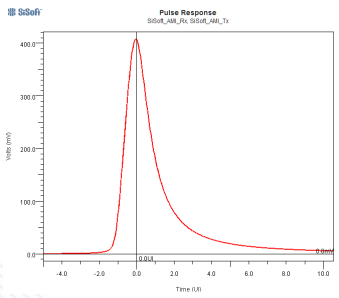
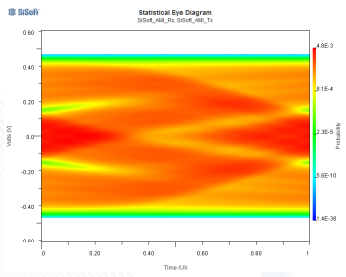
EQ Example: 20 inch channel, 10 Gb/s



15.3 dB loss



12+ bits of ISI



No EQ = No eye

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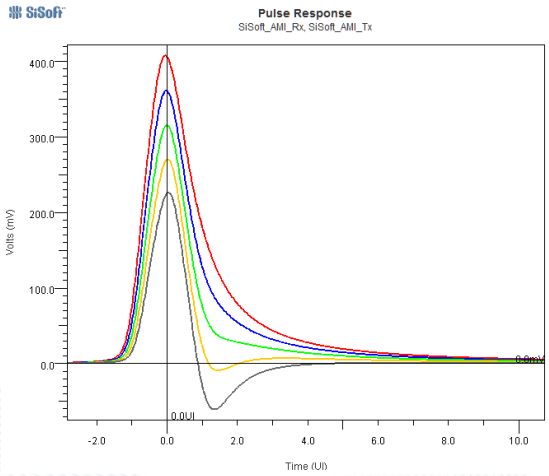
Sweeping the 1st Post-cursor Pulse Response

Case	Cursor	1st Post
1	1.0	0.0
2	0.9	-0.1
3	0.8	-0.2
4	0.7	-0.3
5	0.6	-0.4

- Which case will give us the best eye?



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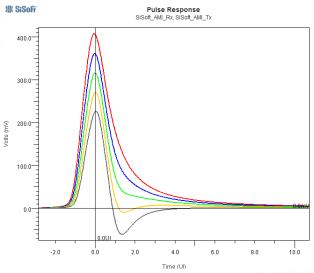
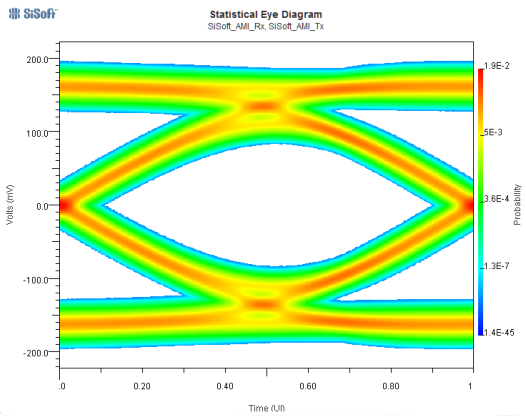
Using Pulse Responses to Find TX Equalization

Row	Tx:tap_filter.0	Tx:tap_filter.1	Stat Eye Height (V)
1	1	0	0
2	.9	-.1	0
3	.8	-.2	0.0706985
4	.7	-.3	0.166147
5	.6	-.4	0.126204





Full Time Domain analysis not required

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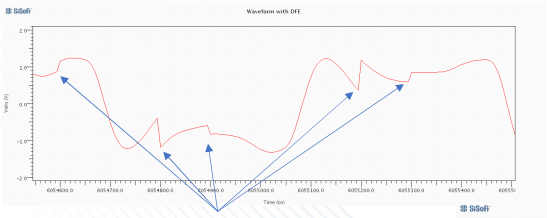
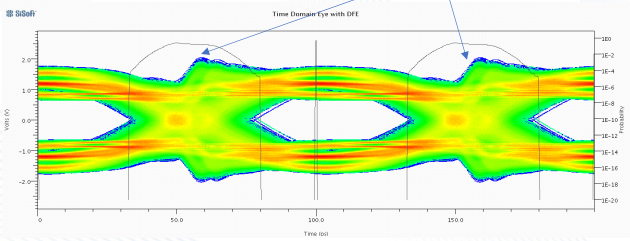
AMI_GetWave Can Also Model Time-Variant Effects



RX Decision Feedback Equalizer (DFE) taps

- Adaptive corrections
  - DFE
  - CTLE
  - AGC
- Non-Linear Impairments
  - Saturation

RX DFE action visible in eye diagram



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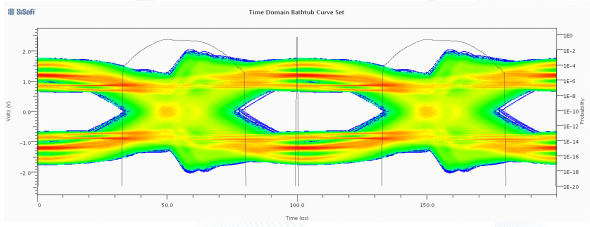
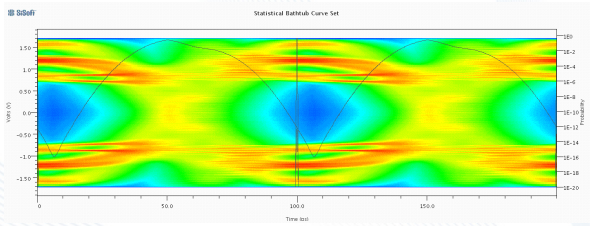
Using Both Time Domain and Statistical Analysis

- No single analysis method models all impairments and all corrective measures well enough
- Many helpful techniques, eg.:
  - Statistical extrapolation of time domain
  - Get adapted settings from time domain and apply to statistical (can reduce Ignore_Bits)
  - Approximate adapted DFE in RX AMI_Init





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Conclusions

- IBIS-AMI time domain simulation with AMI_GetWave can precisely model non-linear effects such as DFE and saturation.
  - But it can be impossible to simulate enough bits in time domain to prove the low BER requirements of some technologies.
- IBIS-AMI statistical analysis can quickly evaluate very low BER.
  - But it can not precisely model time-variant effects such as DFE and saturation.
- It is good practice to use both analysis methods.

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Thank You

- Much content copied from:
  - *Pragmatic Signal Integrity Boot Camp*
    - Donald Telian, SiGuys
    - Michael Steinberger, SiSoft
    - Tripp Worrell, SiSoft
    - Todd Westerhoff, SiSoft
    - Graham Kus, SiSoft
    - Eric Brock, SiSoft
  - DesignCon 2017, Santa Clara, CA
- References

[1] Anthony Sanders, Mike Resso, John D'Ambrosia, *Channel Compliance Testing Utilizing Novel Statistical Eye Methodology*, DesignCon 2004
[2] Jeruchim, Michel C., Philip Balaban, and K. Sam Shanmugan, *Simulation of Communication Systems*, Second Edition, New York, Kluwer Academic/Plenum, 2000

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ZTE

A Way to Evaluate post-FEC BER based on IBIS-AMI Model

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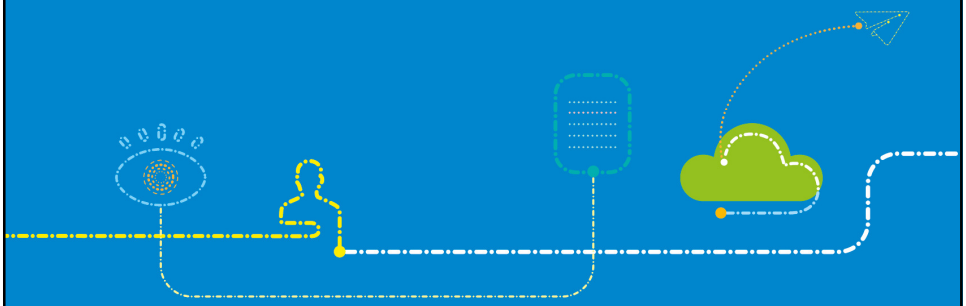
Asian IBIS Summit, Shanghai, China, November 13, 2017



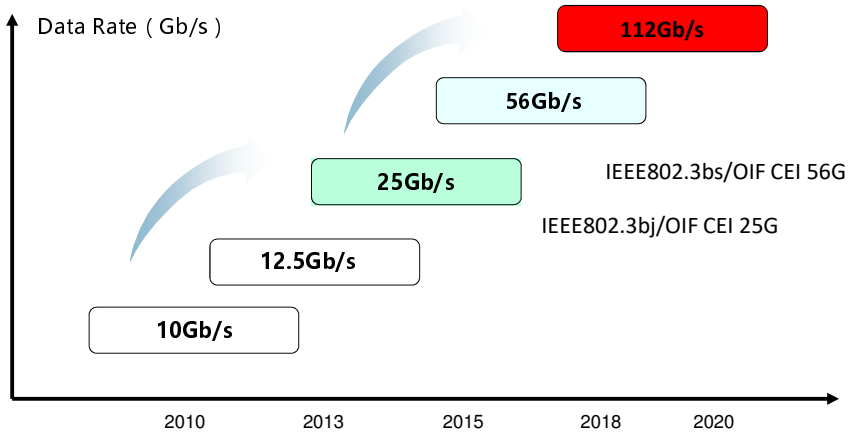
Agenda

- Introduction
- Error Propagation Theory
- A Simulation Case
- Summary

Introduction

200/400&800 Gigabit Ethernet is urgently needed in carrier network

Higher data rate requirements for 56Gb/s,even 112Gb/s



3

ZTE

Introduction

Besides equalization techniques, some new techniques have been used for SerDes systems in order to meet 100GE- 400GE-800GE specs

Higher Data Rate：25Gb/s to 56 Gb/s to 112 Gb/s

Equalization：
De-emphasis+CTLE+DFE

IC Architecture：
Analog based architecture
DSP based architecture

Fanny Modulation：NRZ or PAM4
Forward Error Correction：**FEC**
(optional vs. forced)

How to use it in simulation?

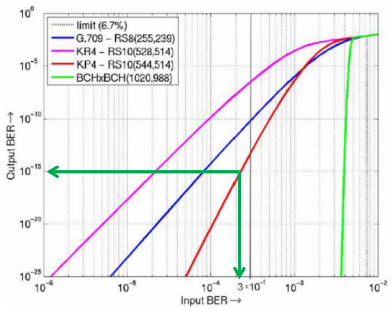
4

ZTE

Introduction

The Forward Error Correction（FEC）has been used to Increase serial link system budgets and relaxing BER requirements

- Code Gain
  - Gain vs Higher Frequency
- Time
  - Serial Link Latency
- Complexity
  - Area and Power



Target (OIF-56G-LR)
2.2e-4 without FEC
1e-15 with FEC

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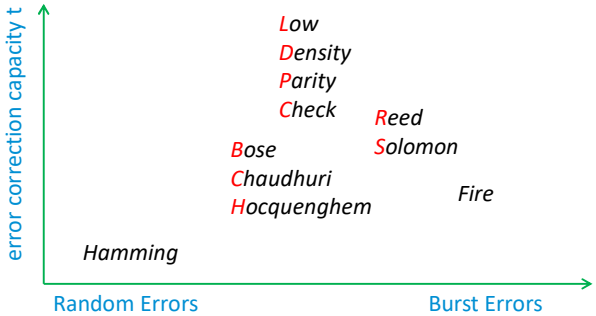
Introduction

- Important FEC codes



Recently adopted FEC

- Fire Code （1604, 1584） – OIF CEI-P
- QC Code （2112, 2080） – 10GBASE-KR
- RS（528, 514, 7） over GF(2^{10}) – 100GBASE-KR4
- RS（544, 514, 15） over GF(2^{10}) – 100GBASE-KP4

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Introduction

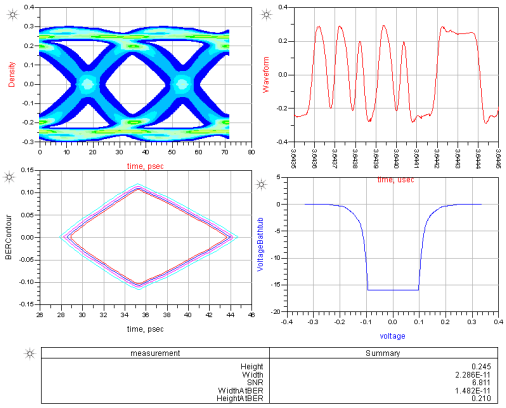
- *What can we get from simulaiton based on IBIS-AMI model?*

Available

- Eye Diagram
- Waveform
- Contour
- Bathtub

Absent

- postFEC BER



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Introduction

- Current Problems
  - ➢ FEC is a forced function in 400GE and 800GE system
  - ➢ There is no FEC function model in the IBIS-AMI yet
- System Vendor Requirements
  - ➢ IBIS-AMI models can be used for FEC simulations
  - ➢ postFEC BER

We proposed a new solution evaluated the postFEC BER using FEC model

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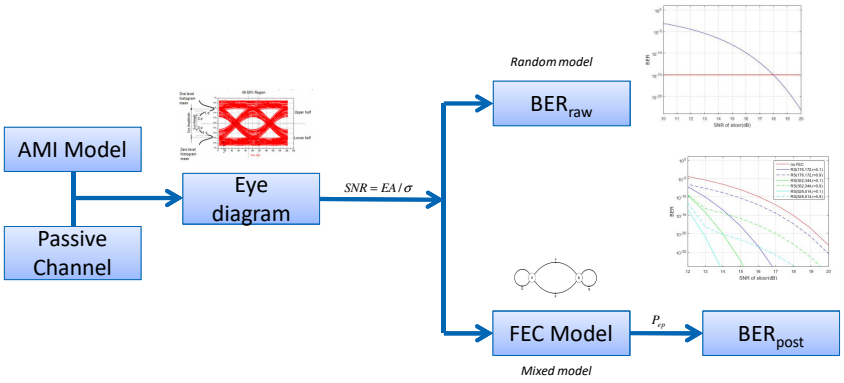
Introduction

- Suggested Solution Process



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Agenda

- Introduction
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Error Propagation Theory

Random Error

- The presence and the location of the error satisfy the random distribution
- The errors are independent of each other
- Usually caused by the random noise of the channel, AWGC channel
- Random errors are generally single bit.

Burst Error

- The error contains a series of bits, the first and last bit in an error are always wrong
- There is a certain relationship between the error bits
- Caused by some structures, such as DFE, Scrambler
- The length of the error is called the burst error length

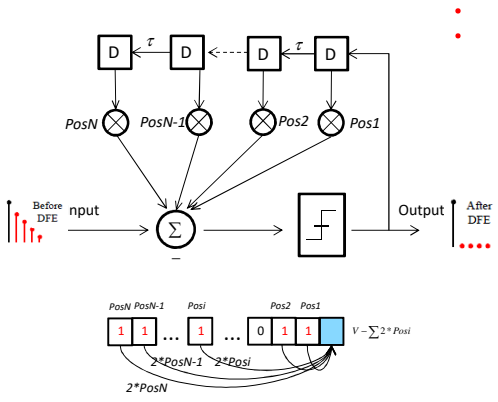
Mixed Error

- Channel contains random error and burst error
- We consider the channel as random error channel without DFE, otherwise the channel is a mixed error channel

ZTE

Error Propagation Theory

DFE diagram



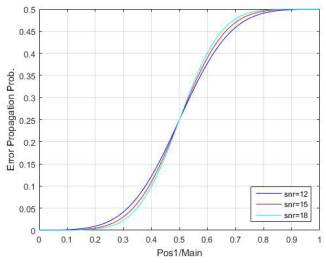
- If all DFE state registers were right, error probability is decided by slicer SNR
- If *ith*-cursor were wrong, generate a (2**Posi*) voltage deviation
- The output of DFE is associated with the previous N-bits information, where N is the number of DFE taps

ZTE

Error Propagation Theory

- Many methods are used to analyse the error propagation such as
  - Monte-Carlo simulation
  - Markov chain model
  - Error Propagation theory

...



- Decision feedback equalizer (DFE) is widely used to reduce ISI
- However, this structure induces burst errors in channel
- The increased input BER performs a penalty on FEC coding gain
- Trade off between n-Tap DFE and high coding gain FEC

ZTE

Error Propagation Theory

- FEC analysis for random error channel
  - Raw BER is decided by the channel SNR

$$BER_{pre} = Q(\sqrt{SNR}) = \frac{1}{2} erfc(\frac{\sqrt{SNR}}{\sqrt{2}})$$

  - Every RS-FEC symbol has *m*-bits, thus the error symbol rate is

$$SER_{FEC,pre} = 1-(1-BER_{pre})^{m}$$

  - RS-FEC can correct *t*-symbol, the Probability of un-correction in FEC symbol is

$$P_{UE} = \sum_{i=t+1}^{n} \frac{i}{n} \binom{n}{i} SER_{pre}{}^{i} \left(1-SER_{pre}\right)^{n-i}$$

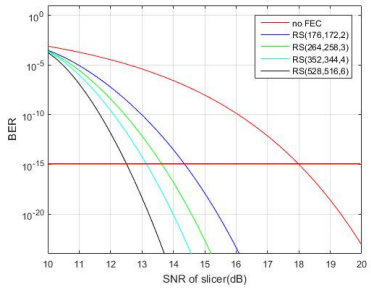
  - The output BER is

$$BER_{post} = 1-(1-P_{UE})^{1/m} \approx P_{UE}/m$$

ZTE

Error Propagation Theory

- FEC Gain for Several RS Codes



- Without FEC, ~18dB SNR is needed to get 1e-15 BER
- Code with larger *t* can get higher net coding gain (NCG)
- At BER 1e-15, *t=2, 3, 4, 6* RS codes can get 3.6dB, 4.4dB, 4.8dB, and 5.5dB NCG, respectively
- The result is too idealistic because the model just considers the random error

ZTE

Error Propagation Theory

- FEC analysis for 1-tap DFE channel
  - Raw BER is decided by the channel SNR

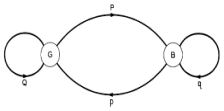
$$BER_{pre} = \frac{1}{2} erfc(\frac{\sqrt{SNR}}{\sqrt{2}})$$

  - The error propagation probability (Pep) is

$$P_{ep} = \frac{1}{4}\left[erfc\left(\frac{(1+2b_1/b_0)\sqrt{SNR}}{\sqrt{2}}\right) + erfc\left(\frac{(1-2b_1/b_0)\sqrt{SNR}}{\sqrt{2}}\right)\right]$$

b1/b0 is the ratio of Pos1 to main

  - Error propagation follows the Markov chain probability of (*k+1)* consecutive errors and is



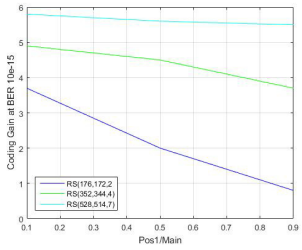
$$p(bl = k+1) = p_{ep}^{\ k}(1 - p_{ep})$$

  - Calculate the postFEC BER

ZTE

Error Propagation Theory

- Coding Gain Vs. Tap coefficient



- When Pos1/Main increase, FEC coding gain decreases
- RS codes with larger *t* can get higher gain
- Gain drops more rapidly for RS codes with small *t* because they cannot correct the long errors effectively
- RS(528, 514, 7) can get about 5.8dB gain for random error channel, consistent with 802.3bj ad OIF-25G standard

ZTE

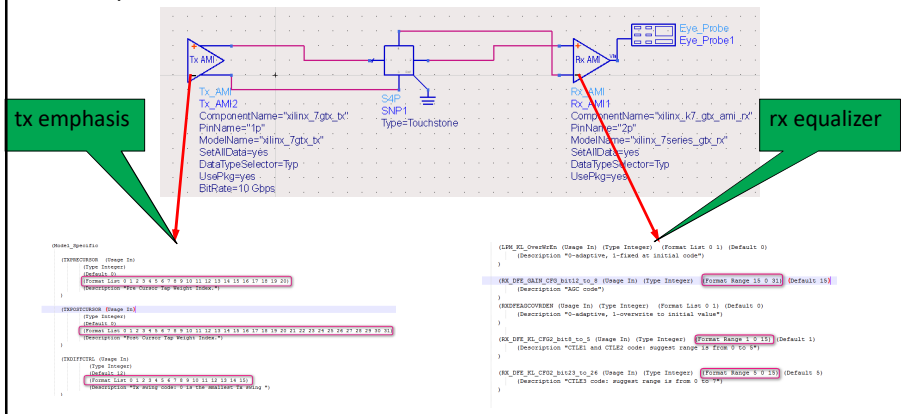
Agenda

- Introduction
- Error Propagation Theory
- A Simulation Case
- Summary

ZTE

A Simulation Case

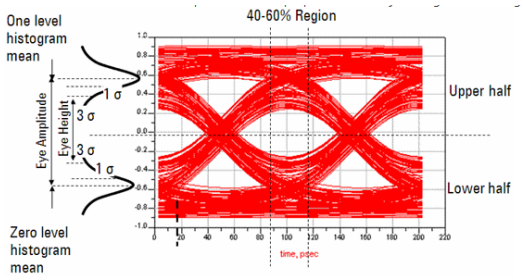
- Acquisition of SNR



- Simulation with IBIS-AMI model
- Using the optimal tx emphasis parameters
- Using the optimal rx equalizer parameters
- Getting the best eye diagram

ZTE

A Simulation Case



- SNR=S/N=S_amp/(N_sigma1+N_Sigma0), where S_amp=signal amplitude
- S_amp: 1 level histogram mean - 0 level histogram mean
- N_sigma: 1 sigma value

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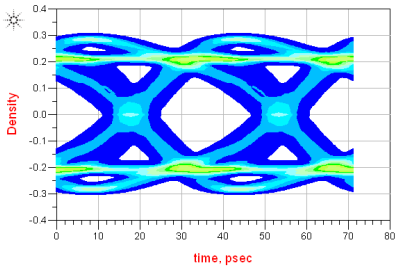
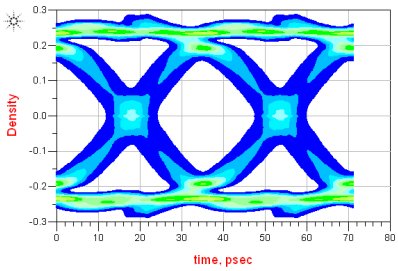
A Simulation Case

- Comparison

DFE OFF



DFE ON



- DFE impacts are obvious on eye diagram quality

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A Simulation Case

- Results for RS(528, 514, 7)

	SNR=12dB	SNR=13dB	SNR=14dB	SNR=15dB
	BER_{post}			
BER_{pre}	3.43e-5	3.97e-6	2.70e-07	9.36e-9
Random (Pos1/main=0)	3.53e-14	1.30e-21	5.98e-31	1.27e-42
Pos1/main=0.5	3.82e-14	1.41e-21	6.48e-31	1.70e-42
Pos1/main=1	5.29e-14	2.06e-21	7.13e-24	2.48e-25

- The error propagation probability increases while the DFE tap coefficient becoming larger
- The BER increases with the tap coefficient
- Larger SNR shows more obvious change as shown by the relatively low BER and the effect of error floor

ZTE

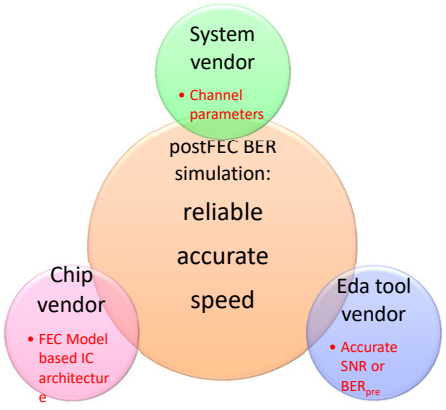
Agenda

- Introduction
- Error Propagation Theory
- A Simulation Case
- Summary

ZTE

Summary

- We proposed a method to evaluate the postFEC BER for a system
- To achieve the simulation in the common **EDA Tool** based on **IBIS-AMI** model, we appeal to all the members to solve the problem together.

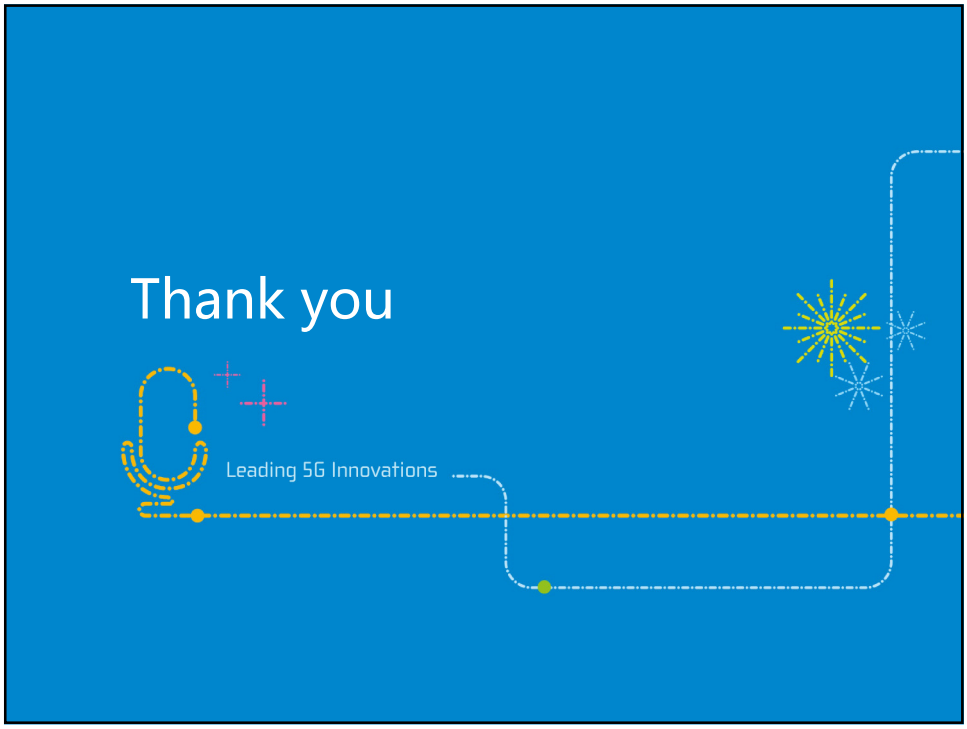


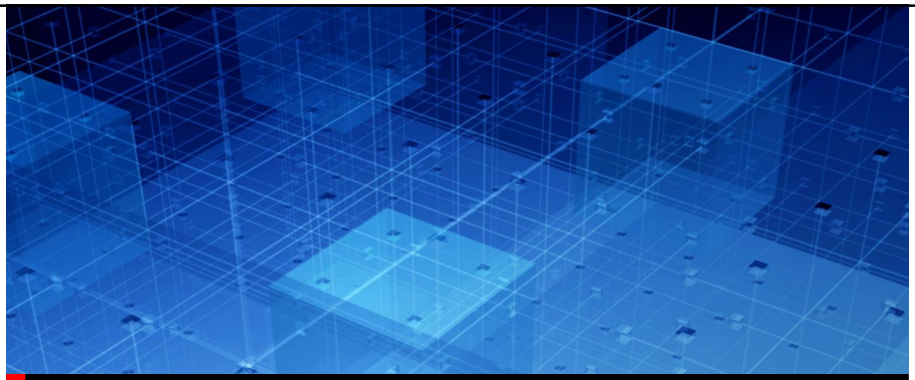
ZTE

Summary

- An analysis method is performed combining AMI model and FEC function
- FEC function modeled based on error propagation theory
- SNR calculated through EDA tool with IBIS-AMI model
- Calculate the postFEC BER
- Advantages: SNR contains multiple effects of chip and channel; each part can be optimized separately
- We appeal to all the members to solve the problem together

ZTE





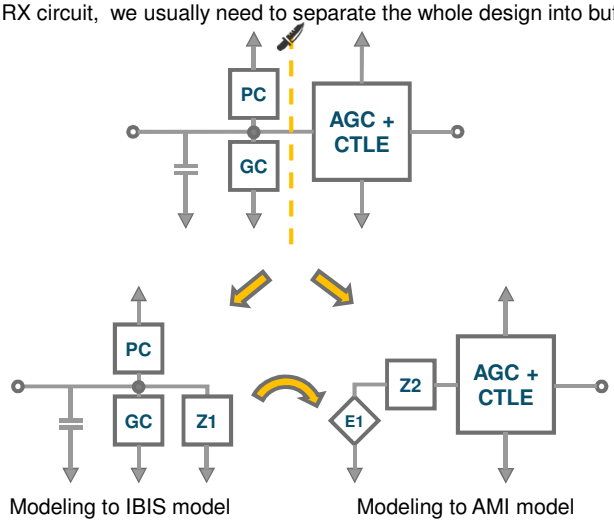
Characterizing and Modeling of a Linear CTE

Skipper Liang
Asian IBIS Summit
Shanghai, PRC
November 13, 2017

cadence

To Divide a RX Circuit:

For modeling a RX circuit, we usually need to separate the whole design into buffer part and algorithm part:



1. Question 1: What's the value of **Z1** and **Z2**?
2. Question 2: What if the whole design is described in **an encrypted netlist**?

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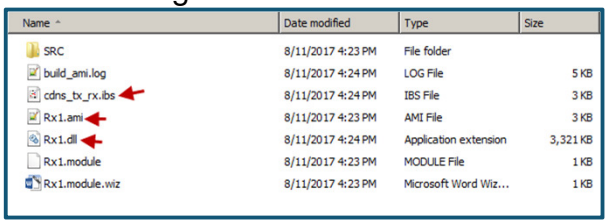
IBIS model

- generated from AMI generation tools



Name	Date modified	Type	Size
SRC	8/11/2017 4:23 PM	File folder	
build_ami.log	8/11/2017 4:24 PM	LOG File	5 KB
cdns_tx_rx.ibs	8/11/2017 4:24 PM	IBS File	3 KB
Rx1.ami	8/11/2017 4:23 PM	AMI File	3 KB
Rx1.dll	8/11/2017 4:24 PM	Application extension	3,321 KB
Rx1.module	8/11/2017 4:23 PM	MODULE File	1 KB
Rx1.module.wiz	8/11/2017 4:23 PM	Microsoft Word Wiz...	1 KB

Many AMI generation tools will generate an IBIS model along with the AMI models generation:

1. Question 1: Can we use this IBIS model? **YES**
2. Question 2: If yes, is there any requirement of the circuit while modeling this circuit in this way?

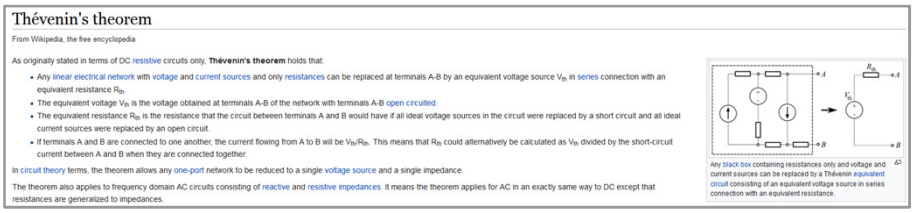
   The circuit should be a RX one composed of linear components.

3. Question 3: If my circuit could meet the requirement list above, how to do the modeling?

   Detailed in the following pages

cadence

Thevenin's Theorem



Thévenin's theorem

From Wikipedia, the free encyclopedia

As originally stated in terms of DC resistive circuits only, **Thévenin's theorem** holds that:

- Any linear electrical network with voltage and current sources and only resistances can be replaced at terminals A-B by an equivalent voltage source V_{Th} in series connection with an equivalent resistance R_{Th}.
- The equivalent voltage V_{Th} is the voltage obtained at terminals A-B of the network with terminals A-B open circuited.
- The equivalent resistance R_{Th} is the resistance that the circuit between terminals A and B would have if all ideal voltage sources in the circuit were replaced by a short circuit and all ideal current sources were replaced by an open circuit.
- If terminals A and B are connected to one another, the current flowing from A to B will be V_{Th}/R_{Th}. This means that R_{Th} could alternatively be calculated as V_{Th} divided by the short-circuit current between A and B when they are connected together.

In circuit theory terms, the theorem allows any one-port network to be reduced to a single voltage source and a single impedance.

The theorem also applies to frequency domain AC circuits consisting of reactive and resistive impedances. It means the theorem applies for AC in an exactly same way to DC except that resistances are generalized to impedances.

Any black box containing resistances only and voltage and current sources can be replaced by a Thévenin equivalent circuit consisting of an equivalent voltage source in series connection with an equivalent resistance.

In short:

V_{TH} = The voltage across the Port – "node A and B" while treating the Port – "node A and B" as **OPEN**

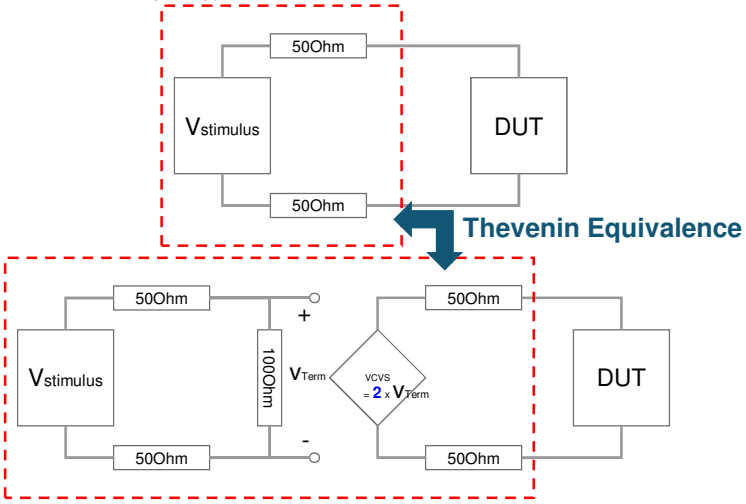
I_{SC} = The current goes into node A and leaves node B while treating the Port – "node A and B" as **SHORT**

$R_{TH} = V_{TH}/I_{SC}$

cadence

Thevenin Equivalence

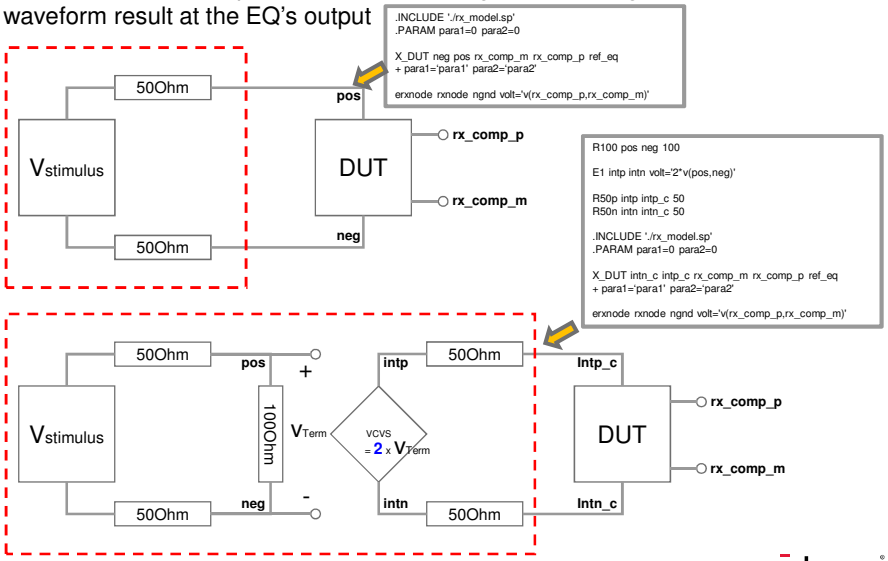
Typically, an RX test topology



cadence

Thevenin Equivalence(Cont'd)

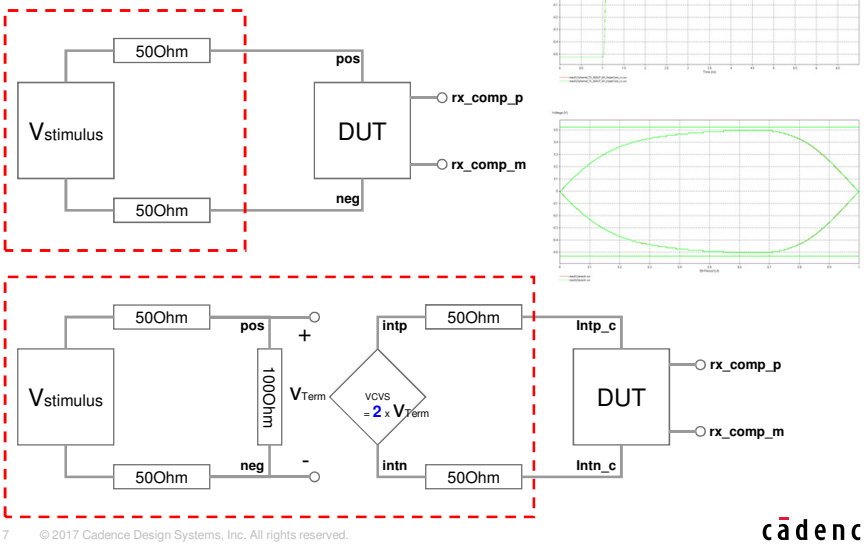
You can do a small experiment – the following 2 netlist will give the same waveform result at the EQ's output



cadence

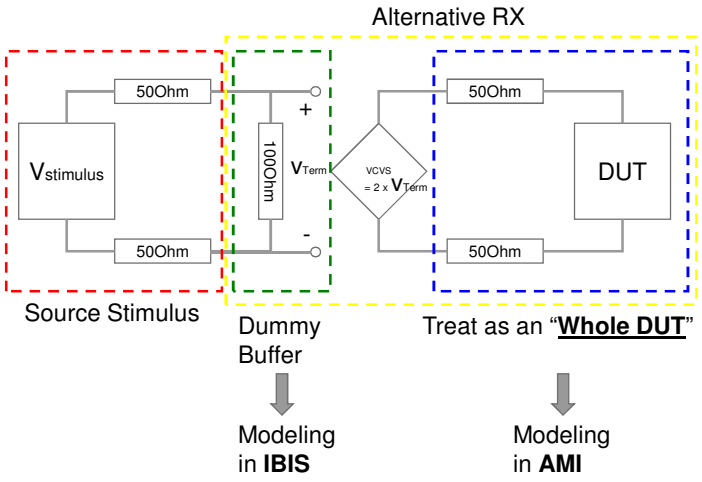
Thevenin Equivalence(Cont'd)

Hard to tell the difference



cadence

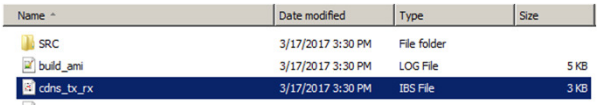
Alternative RX



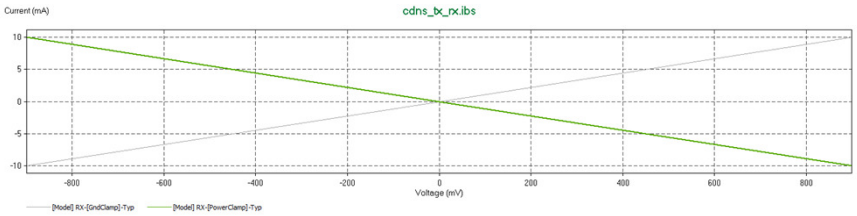
cadence

IBIS of the Dummy Buffer

Check the RX IBIS model, which is generated along with the AMI model, to see if it's a 100Ohm terminator between positive node and negative node:

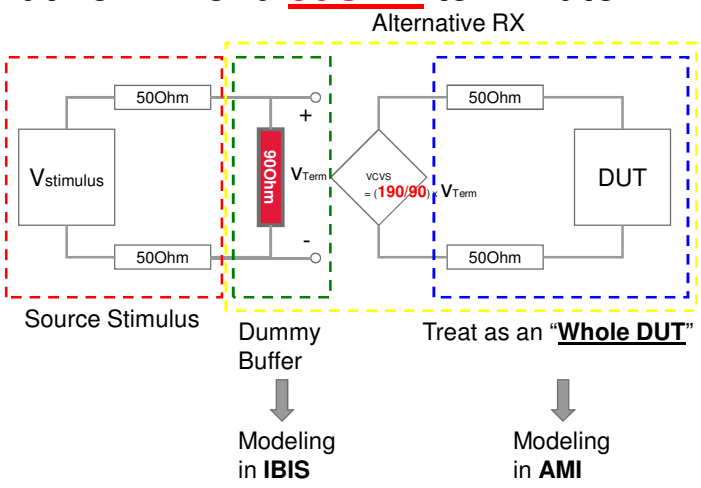


For example, some AMI generation tools generate RX IBIS model with 90Ohm terminator between positive node and negative node – tell from the [Power Clamp] and [Ground Clamp]:



cadence

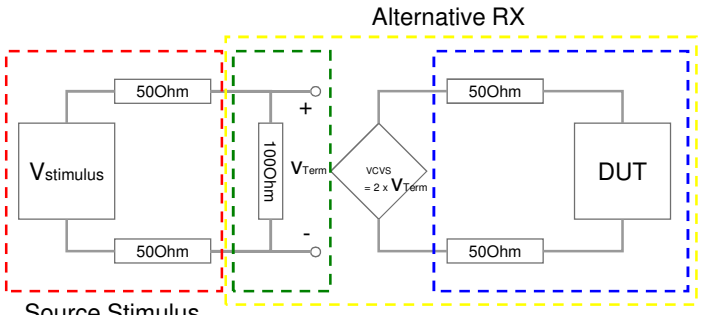
Alternative RX for a 90Ohm terminator



Or……

cadence

IBIS model of 100Ohm terminator



And now, you don't need to model the IBIS part or use the non-100Ohm terminator IBIS model. You just use the files here attached:


rx100term.ibs


R_100.ckt

cadence

IBIS model of 100Ohm terminator (Cont'd)

The content of these files:


rx100term.ibs

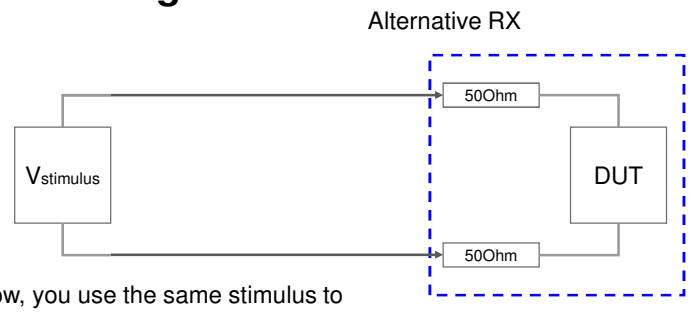
```
[Model] RX
Model_type Input_diff
[Voltage Range]          1.000V          1.0V          1.0V
[Ramp]
| variable       typ                  min                  max
dV/dt_r 0.120/0.001n        0.120/0.001n        0.120/0.001n
dV/dt_f 0.120/0.001n        0.120/0.001n        0.120/0.001n
R_load = 50.000
|
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name (.subckt name)
Corner    Typ          R_100.ckt   R_100
Corner    Min          R_100.ckt   R_100
Corner    Max          R_100.ckt   R_100
|
| Ports List of port names (in same order as in SPICE)
Ports A_puref A_pdref A_signal_pos A_signal_neg
|
| A_to_D d_port port1 port2 vlow vhigh corner_name
A_to_D D_receive A_signal_pos A_signal_neg -0.0 0.1 Typ
A_to_D D_receive A_signal_pos A_signal_neg -0.0 0.1 Min
A_to_D D_receive A_signal_pos A_signal_neg -0.0 0.1 Max
|
[End External Model]
[Algorithmic Model]
Executable Windows_VisualStudio_64 RX_HyperCore.dll RX_HyperCore.ami
[End Algorithmic Model]
|
[End]
```


R_100.ckt

```
1  .subckt R_100 DVDD DVSS pos neg
2
3  Rp pos gnd 1e+15
4  Rn neg gnd 1e+15
5  Rdiff pos neg 100
6
7  .ends
```


cadence

Characterizing:



Now, you use the same stimulus to characterize the circuit inside the Blue Dashed Box, that is:

1. The same voltage swing
2. Fast rising time – 1e-21sec (1e-9ps)
3. Small time steps, no more than 1ps

Which we use to characterize the channel.

Treat as an "**Whole Equalizer**"

Modeling in **AMI**

cadence

Characterizing - Normalizing:

```
( RX_HyperCore
    ( CTE
        ( csvfilt
            ( file D:\Case_CDNS_20160616_IBIS_AMI\Modelize_RX\CTLE_TRAN_0_5
            ( sel 0 )
            ( input 0.57 )
        )
        ( module_off 0 )
        ( csvid_file csvid.txt )
        ( td_filter_out cte_td_out.txt )
        ( adapt_cte_sel_file cte_out.txt )
    )
```

```
24  .subckt TX_50OUT pos neg pwr in ngnd
25
26  E1 pos ngnd volt='0.47+0.57*v(in,ngnd)'
27  E2 neg ngnd volt='1.04-0.57*v(in,ngnd)'
28
29  .ends
```

Normalize to the voltage swing you use to characterize the channel and the equalizer.

cadence

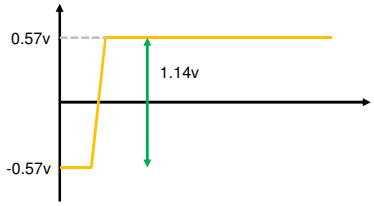
Characterizing – Normalizing (Cont'd):

Beware!!:

```
( RX_HyperCore
    ( CTE
        ( csvfilt
            ( file D:\Case_CDNS_20160616_IBIS_AMI\Modelize_RX\CTLE_TRAN_0_5
            ( sel 0 )
            ( input 0.57 )
        )
        ( module_off 0 )
        ( csvid_file csvid.txt )
        ( td_filter_out cte_td_out.txt )
        ( adapt_cte_sel_file cte_out.txt )
    )
```

```
24  .subckt TX_50OUT pos neg pwr in ngnd
25
26  E1 pos ngnd volt='0.47+0.57*v(in,ngnd)'
27  E2 neg ngnd volt='1.04-0.57*v(in,ngnd)'
28
29  .ends
```

You may wonder the input stimulus is 2x0.57=1.14V,

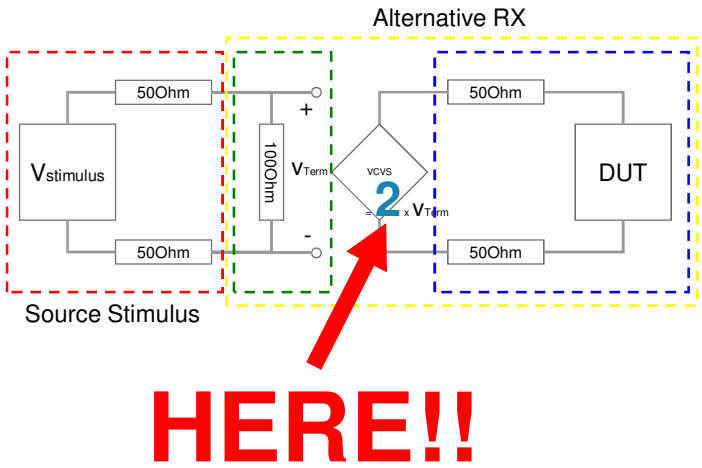


Why do we normalize it to **0.57v**?

cadence

Characterizing – Normalizing (Cont'd):

The answer is:



HERE!!

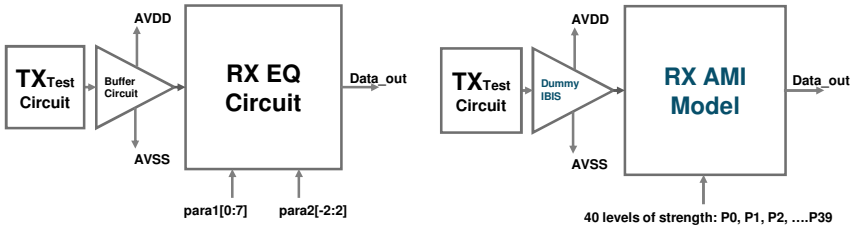
Question: What if you are using an IBIS model which is equivalent to a 90Ohm terminator instead of a 100Ohm?

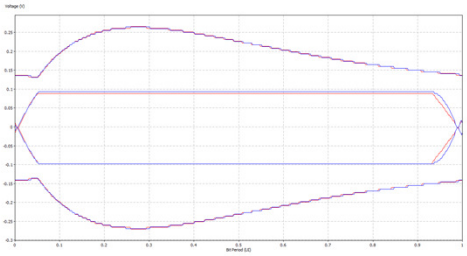
cadence

Correlation – Channel Analysis

between the IBIS-AMI and the Transistor Netlist

Under a simple test environment:





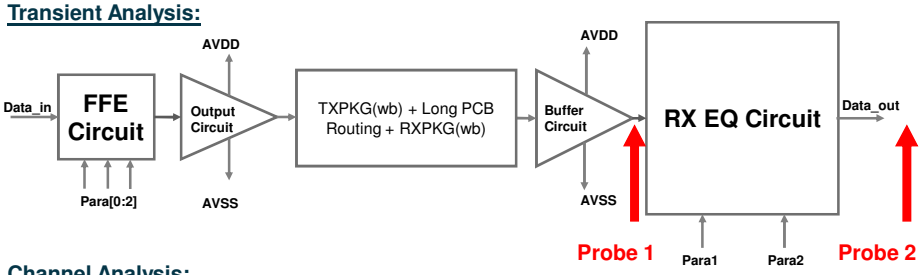
Red: Eye Contour of Transistor Netlist under Channel Analysis

Blue: Eye Contour of IBIS-AMI model under Channel Analysis

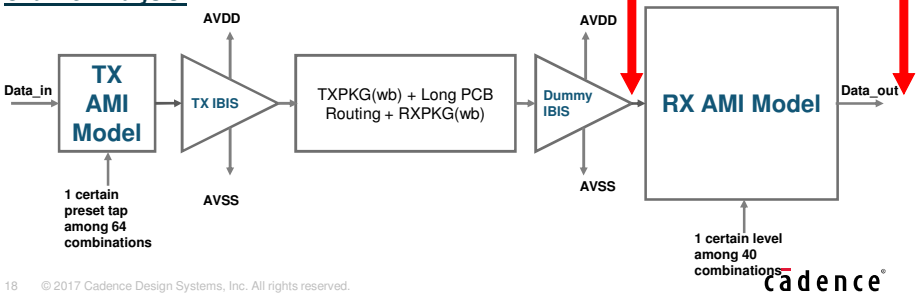
cadence

Correlation – Mid Length Channel

Transient Analysis:

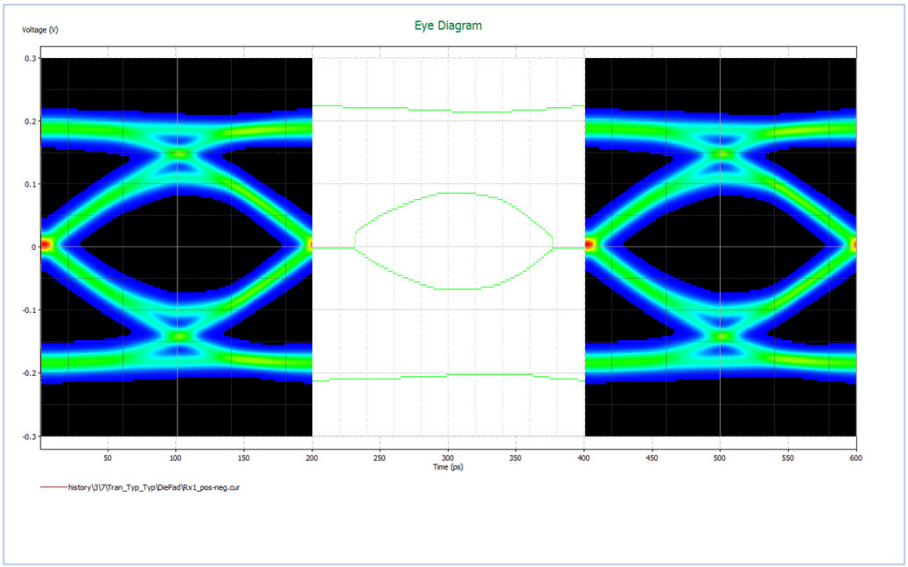


Channel Analysis:



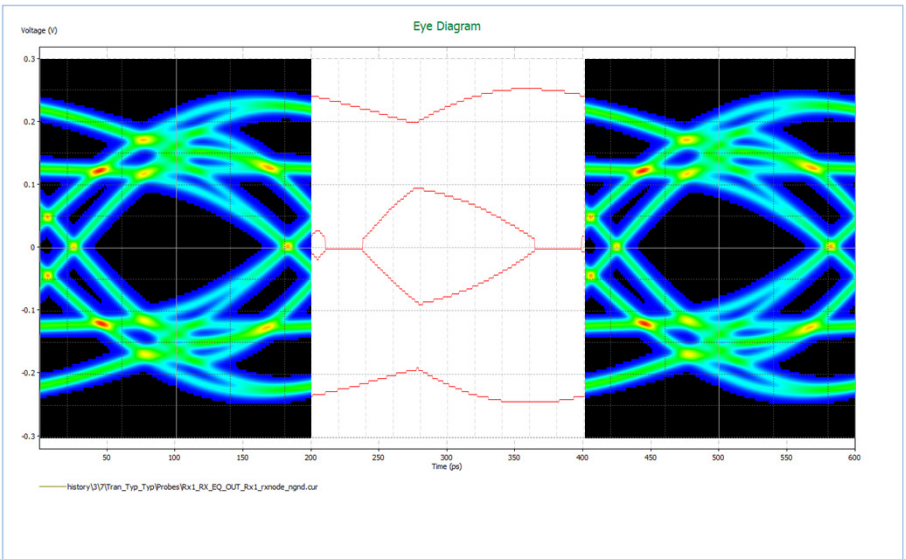
cadence

Correlation – Mid Length Channel (Probe 1)



cadence

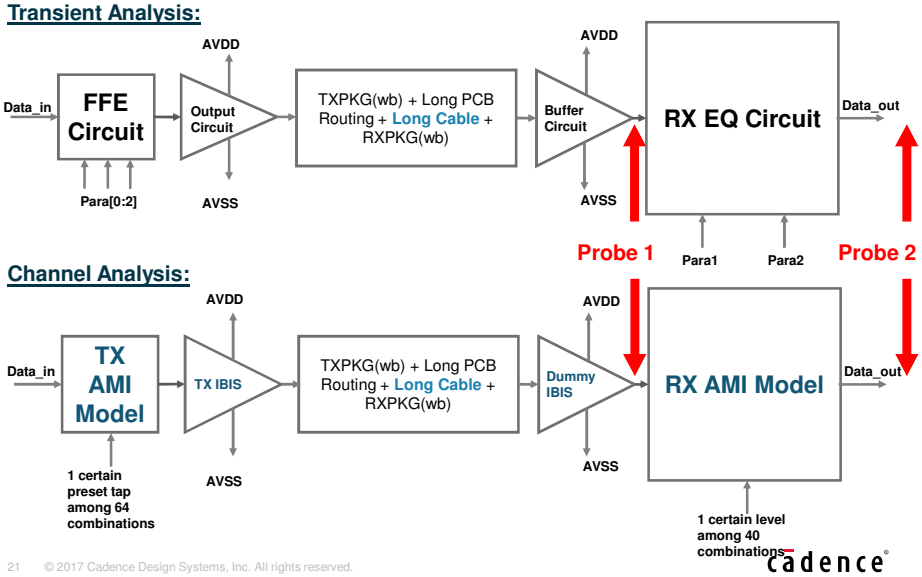
Correlation – Mid Length Channel (Probe 2)



cadence

Correlation – Long Length Channel

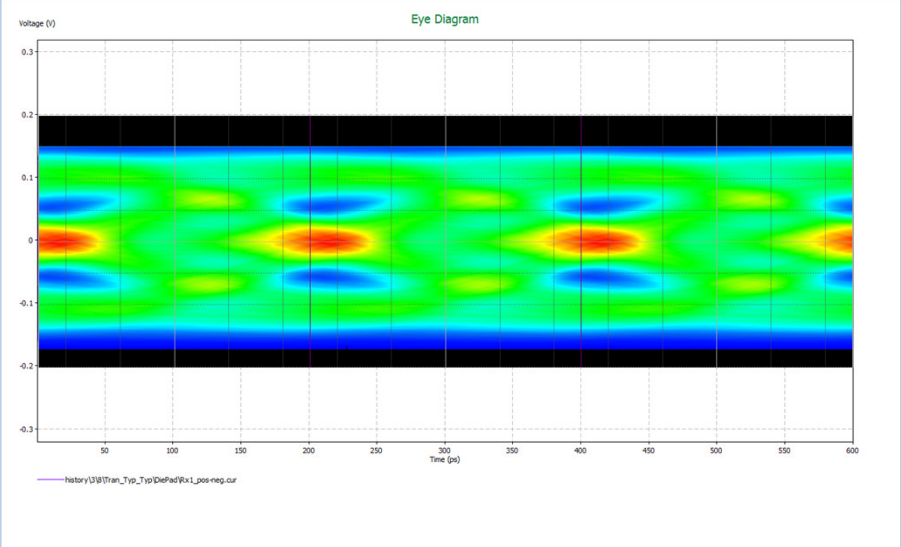
Transient Analysis:



Channel Analysis:

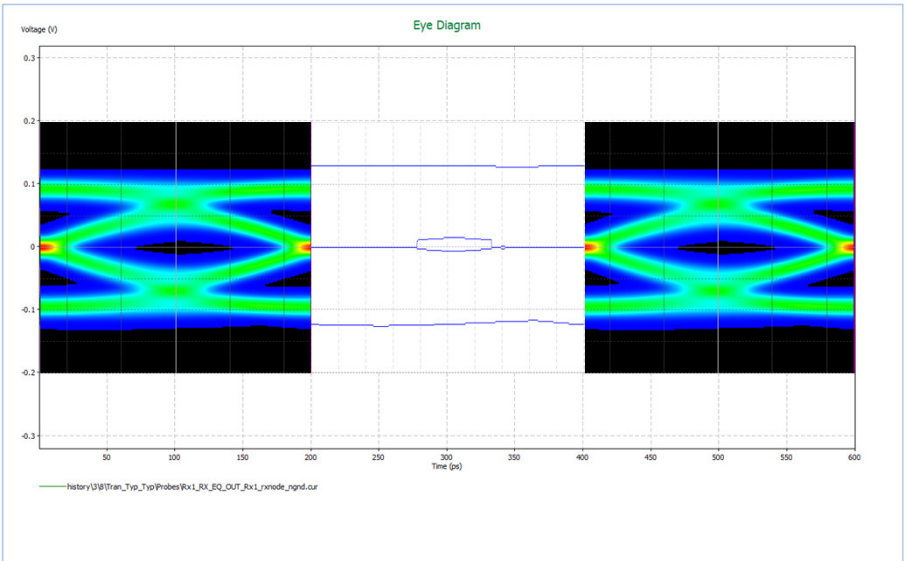
cadence

Correlation – Long Length Channel (Probe 1)



cadence

Correlation – Long Length Channel (Probe 2)

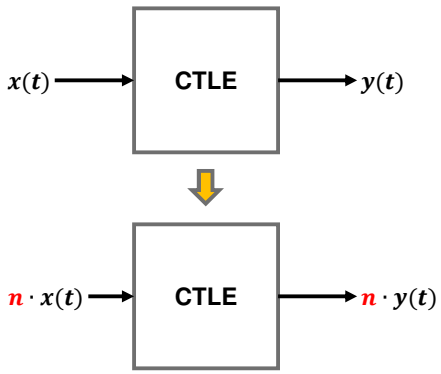


cadence

Limitation

This method is only valid while being applied to a pure CTLE which is composed of linear components, such as R, L, C, Linear E(VCVS), Linear F(CCCS)…etc.

Or in short, a CTLE which satisfies:



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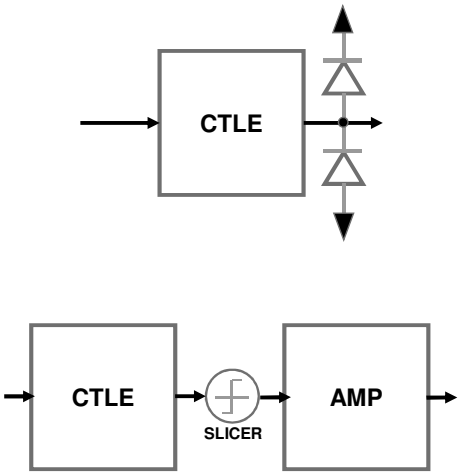
Limitation (Cont'd)

There're still lots of circuits not suitable for this method. For example:



cadence

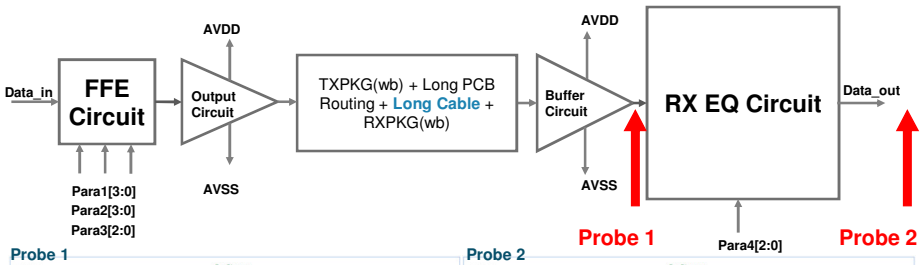
Conclusion

- Cutting/Dividing the whole design is a necessary process during RX IBIS-AMI modeling. This slides provides a method which guarantees the combination of the sub-designs so-divided is exactly equivalent to the original whole design.
- Also, the method in this slides benefits modelers that they will no longer need to model a RX IBIS model. A dummy IBIS will be used for all cases while the buffer characteristics has been modeled into the AMI model. No cutting/dividing is needed any more.
- This slides provides a method to generate IBIS-AMI simply by characterizing the V/T of the netlist – away more accurate than generating IBIS-AMI by inputting parameters values.
- However, this method is only valid while being applied to a purely linear equalizer, that is, there exists a purely linear relationship between the input and output of the equalizer.
- What else? Can a TX FFE be modeled simply by characterizing? Can an non-linear RX CTE be modeled simply by characterizing?

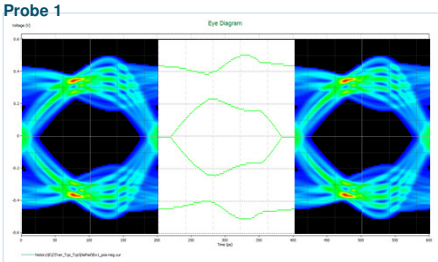
cadence

Correlation – Mid Length Channel

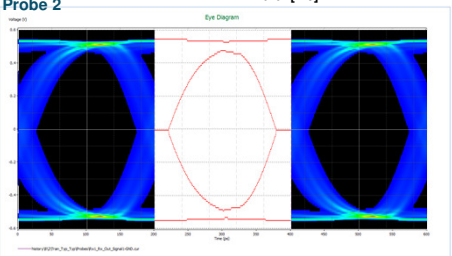
In fact, now we've even developed a flow which can successfully model a **non-linear DFE-free** RX EQ with very good accuracy simply by characterizing: **Example 1**



Probe 1



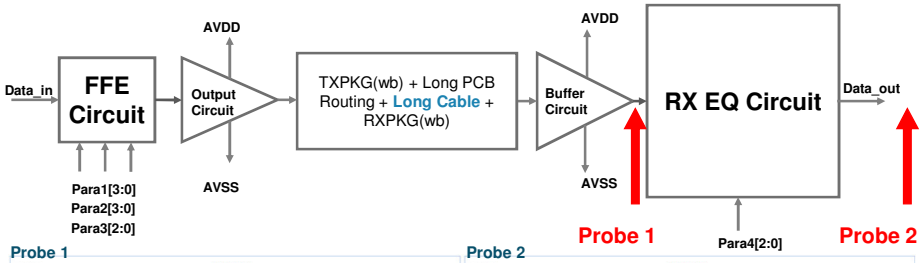
Probe 2



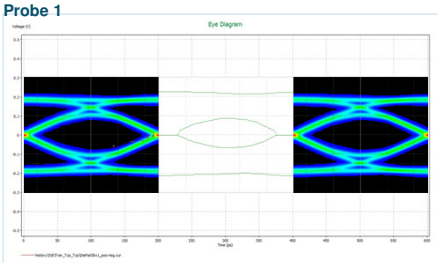
cadence

Correlation – Long Length Channel

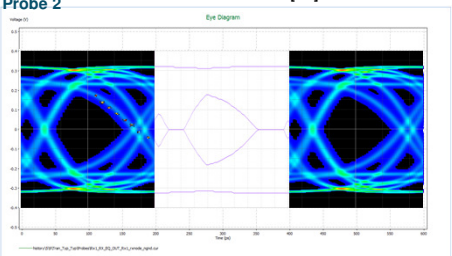
In fact, now we've even developed a flow which can successfully model a **non-linear DFE-free** RX EQ with very good accuracy simply by characterizing: **Example 2**



Probe 1



Probe 2



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See you on IBIS Summit 2018

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Using DATA Files for IBIS-AMI Models

Lance Wang

Asian IBIS Summit
Shanghai, PR China
November 13th, 2017

Outline

This was originally presented in 2017 DesignCon IBIS Summit, and it is with updates.

- Motivation
- Platform/OS dependent DLL, SO
- Using DATA Files for AMI models
- The advantages using DATA Files for AMI models
- Test case for AMI models with DATA Files
- Summary

Special thanks to ANSYS for providing some images in this presentation

Motivation

When we make and use AMI models:

- Who makes AMI executable:
  - Did I write the code that is compatible with all platform/OSs and compilers?
- Who puts everything together into an IBIS file:
  - Did I mess up 64bits and 32bits dll/so files in the IBIS file?
- Who uses AMI models:
  - Why doesn't this AMI model support my OS? Did I do anything wrong with them?

Motivation

- Of course, everyone will blame EDA vendors

Motivation

Can we make everyone a LITTLE happier?

Platform/OS/Compiler Dependent

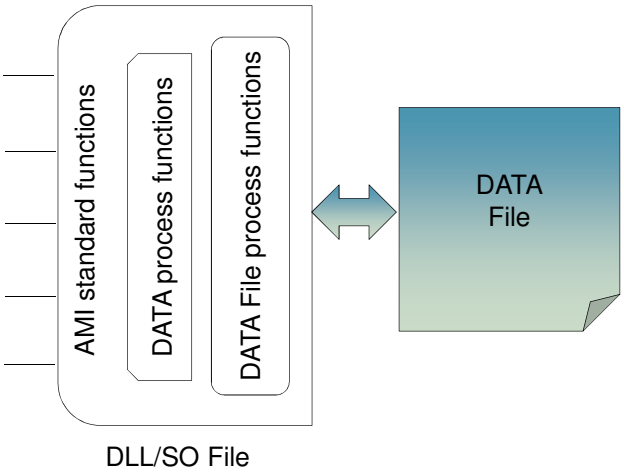
- We have so many platform/OS/Compilers to cover:
  - Windows, Linux, Unix, Mac OS, etc.
  - WinXP, Win8, Win10, Ubuntu, Debian, Fedora, CentOS, Red Hat, etc. Solaris, Solaris 10, HP-UX, OSx, etc.
  - Visual Studio 8 – 11, CC, gcc, etc.
- We also have 32 bit, 64 bit and maybe 128 bit in the future to cover.

This is not all!

Platform/OS/Compiler Dependent

- This makes Designers/Modelers have many headaches:
  - Can my programmed source code be compiled successfully in all platforms?
  - How do I compile and debug my code in all platforms and compilers?
  - Do I need to support all of them?

Using DATA Files for AMI models



Using DATA Files for AMI models

- In DLL/SO
  - AMI standard functions
    - AMI_Init(), AMI_GetWave(), AMI_Close(). Etc.
  - DATA process functions
    - Process the DATA for algorithms
    - Take inputs from AMI standard functions
    - Apply algorithms
    - Put results back to AMI standard functions
  - DATA File process functions
    - Read DATA File
    - Decryption (Optional)

Using DATA Files for AMI models

- In DATA File
  - Software code, and/or
  - Behavioral data, and/or
  - Parameters, or/and
  - Other data
  - Encrypted contents (Optional)

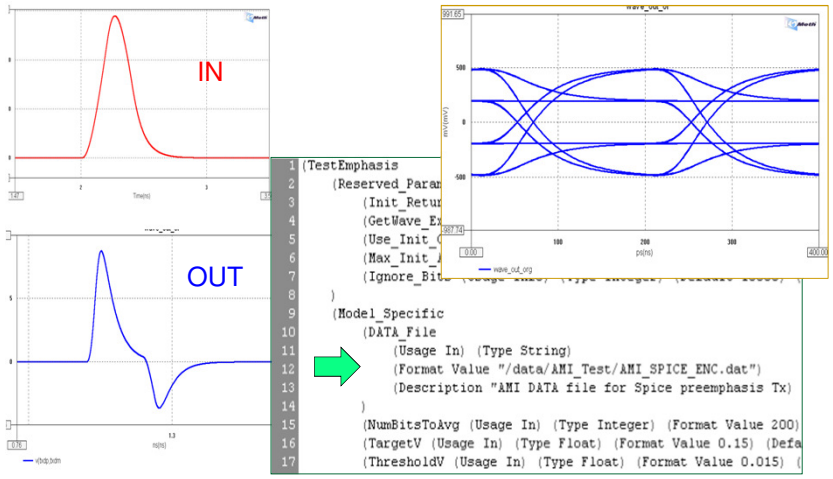
Using DATA Files for AMI models

- The DLL/SO file
  - Could be made by professional software programmers for model vendors or EDA vendors
  - One time job! It can be used for many different DATA Files
- The DATA File
  - Can be created by Designers or Modelers
  - No compilation needed. Platform/OS/Compiler/Bits independent.

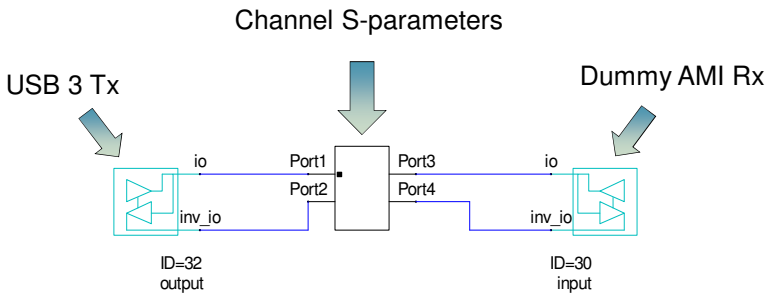
The advantages using DATA Files for AMI models

- DATA File is Platform/OS/Compiler/Bit INDEPENDENT
- Although we will still have to build Platform/OS/Compiler/Bit dependent DLL/SO files to fulfill current IBIS specification, they only need to be built ONCE for model vendor and/or EDA vendor since it can be used for different DATA Files
- The DATA File will be easier to build. And it can be used for different data types that the Model or EDA vendor defines
- The DATA can be securely encrypted with advanced encryption algorithms. It is even more secured than software executables.

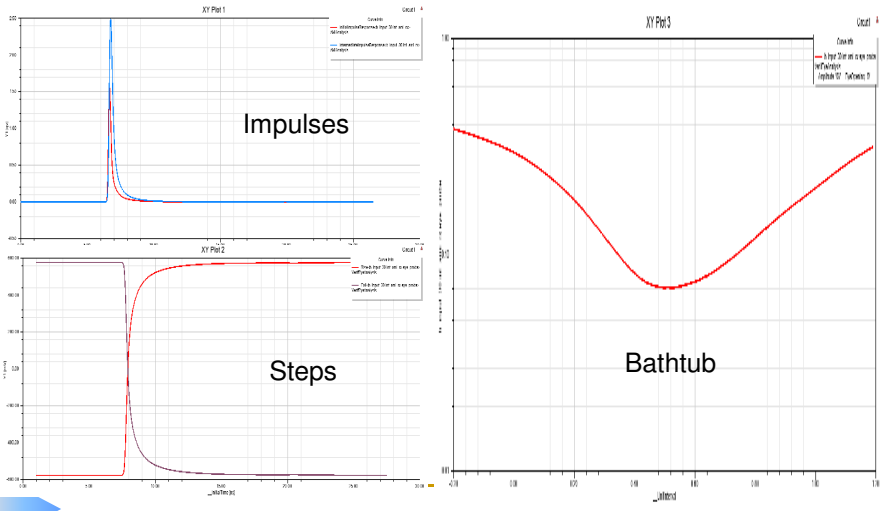
Generic Test case for AMI models with DATA Files



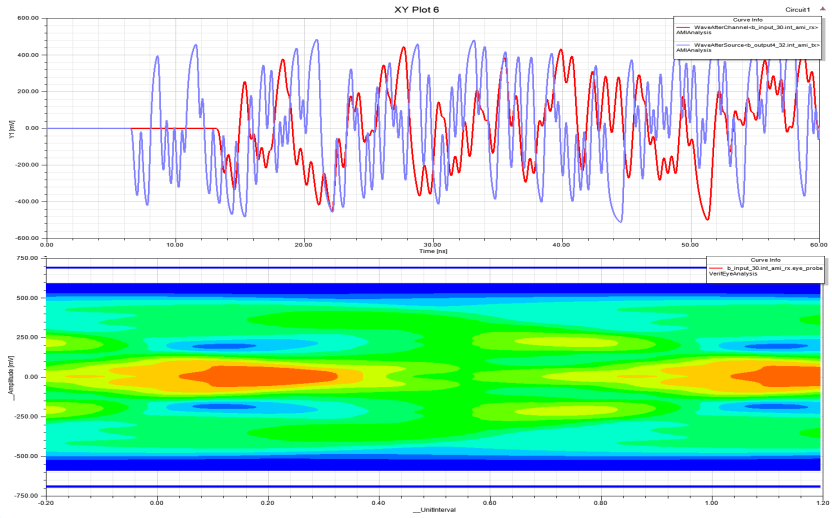
USB3 TX Test case for AMI models with DATA Files



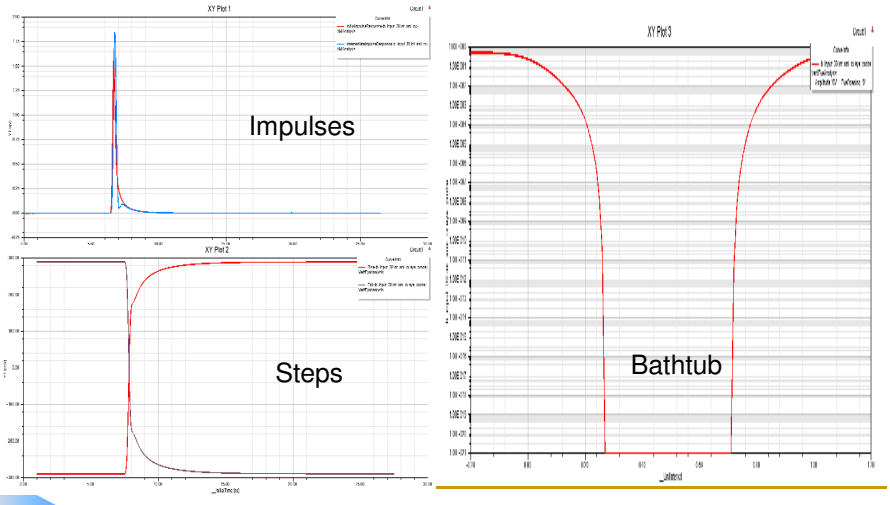
USB3 TX Test case for AMI models with DATA Files – AMP 105 No EQ Applied



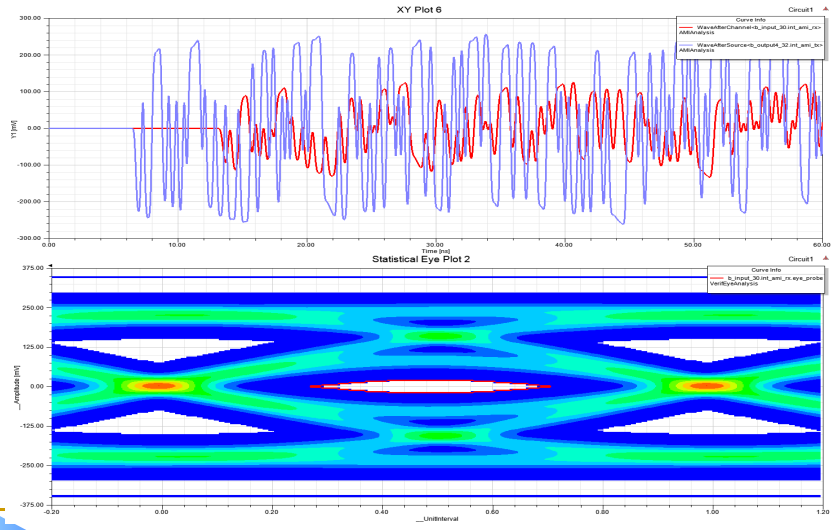
USB3 TX Test case for AMI models with DATA Files – AMP 105 No EQ Applied



USB3 TX Test case for AMI models with DATA Files – AMP 105 EQ 30 Applied



USB3 TX Test case for AMI models with DATA Files – AMP 105 EQ 30 Applied



Summary

- This presentation introduces a DATA File method for IBIS AMI models
  - The DATA File is easier to be created by modeler
  - The DATA File can be very secure through advanced encryption technologies
  - The DLL/SO will only be made by software professional ONCE and used for different DATA files
- This method is currently supported by IBIS specification and works with multiple EDA AMI tools

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Developing the methodologies to make IBIS modeling easy and accurate

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 20

IBIS-AMI Modeling Using Scripts and Spice Models

Asian IBIS Summit
Shanghai, China
November 13th, 2017
(Previously presented October 18th, 2017)

Wei-hsing Huang, SPISim
Wei-hsing.Huang@spisim.com

1

Agenda:

- Motivation
- Background
- IBIS-AMI Modeling Flow
- Modeling with Scripts
- Modeling with Spice models
- Summary
- Q & A

2

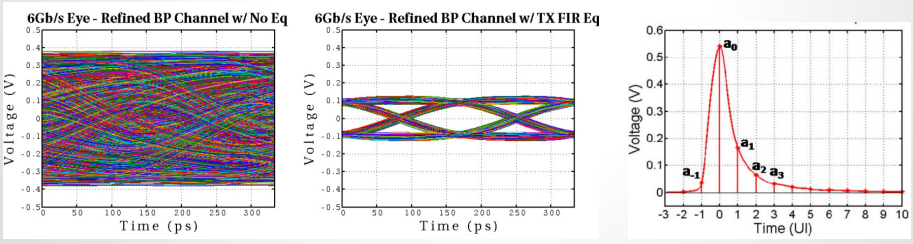
Motivation

- Channel analysis usually requires IBIS-AMI:
  - For internal analysis and/or external model release
- AMI Modeling is technically challenging
  - Requires cross domain expertise
  - Take longer to ramp-up and develop comparing to IBIS
- Can we lower the AMI modeling barriers?
  - Use scripting languages
  - Use existing spice models

3

Background 1/3

- Channel analysis: [1]
  - Mostly have stages beyond traditional IBIS (e.g. Tx/Rx EQ)
  - Analyis methodologies [2]
    - Statistical: for LTI (Linear Time Invariant) circuit, using superposition
    - Time-domain: for NLTV (Non-Linear, Time Variant) circuit, using convolution



4

Background 2/3

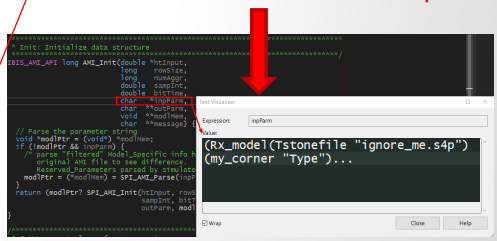
- AMI Model: [3]
  - Includes an .ibs, .ami and .dll/.so files
  - .ibs specifies .ami and .dll/.so files
  - .ami is a plain text file

```
[Algorithmic Model]
| The Model_type for the associated [Model] must be "I/O"
| "I/O_open_drain", "I/O_open_sink", "I/O_open_source", or "I/O_ECL".
|
Executable_Tx Windows_VisualStudio_32 tx_getwave.dll tx_getwave_params.ami
Executable_Tx Solaris_cc_32 libtx_getwave.so tx_getwave_params.ami
|
Executable_Rx Windows_VisualStudio_32 rx_getwave.dll rx_getwave_params.ami
Executable_Rx Solaris_cc_32 libtx_getwave.so rx_getwave_params.ami
|
[End Algorithmic Model]
```

This part is for simulator

This part is for AMI model, passed into .dll/.so as name-value pairs

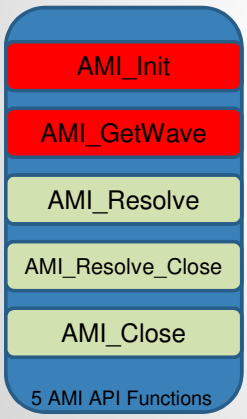
```
(Rx_model
  (Reserved_Parameters
    (Resolve_Exists (Usage Info) (Type Boolean) (Value True)
      (Description "Indicates whether the executable model implements
        AMI_Resolve.”))
    (Model_Name (Usage In) (Type String) (Value “ignore_me”)
      (Description “IBIS model name”))
    (Rx_Receiver_Sensitivity (Usage Out) (Type Float) (Range 0.0 0.0 0.01)
      (Description “Value depends on OP_mode and data rate”))    …
  )
  (Model_Specific
    (Tstonefile (Usage Dep) (Type String) (Value “ignore_me.s4p”)
      (Description “Rx analog model. Value depends on OP_mode”))
    (my_corner (Usage In) (Type String) (Corner “Typ” “Min” “Max”)
      (Description “Informs the executable model what corner is selected by
        user”))
    (OP_mode (Usage In) (Type Integer) (List 0 1 2 3)
      (Description “Operation mode”))
    …
  )
)
```



5

Background 3/3

- AMI Model:
  - .dll/.so may implements these API functions



For LTI processing, when AMI_GetWave does not exist

For LTI or NLTV processing, when AMI_GetWave does exist

These arrays serve as both waveform data input and output!

```
long AMI_Init (double *impulse_matrix,
               long number_of_rows,
               long aggressors,
               double sample_interval,
               double bit_time,
               char *AMI_parameters_in,
               char **AMI_parameters_out,
               void **AMI_memory_handle,
               char **msg)
```

```
long AMI_GetWave (double *wave,
                  long wave_size,
                  double *clock_times,
                  char **AMI_parameters_out,
                  void *AMI_memory)
```

6

AMI Modeling Flow

- Identify model behavior(s)
  - From mathematical equation, simulation or measurements
- Code the behaviors and IBIS-AMI API
  - API implemented MUST follow IBIS spec. and in C
  - Core processing can be in written other languages
- Compile and link as .dll or .so
  - Check library dependencies, different OS bits & linux distros

With Script and/or Spice models for core processing, this AMI model is very reuseable!

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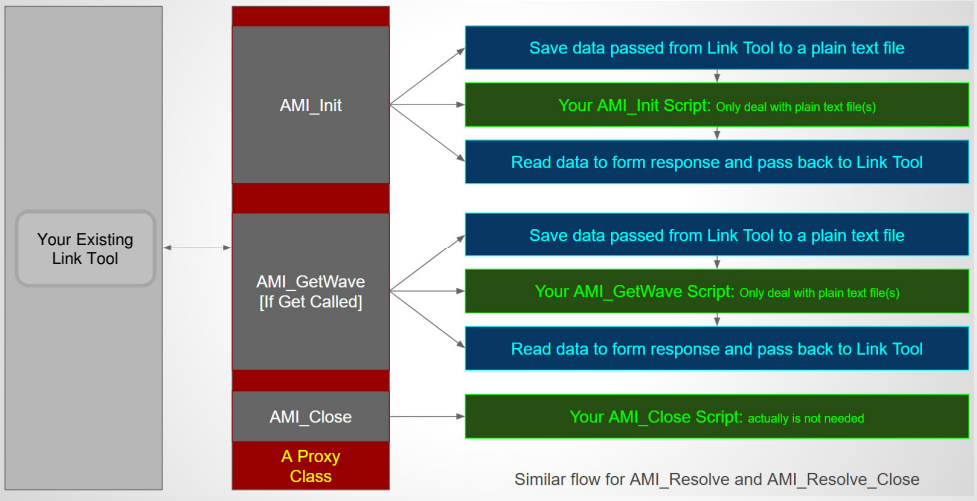
Modeling with Scripts: Flow



[4]

Script path and arguments are passed via .ami file

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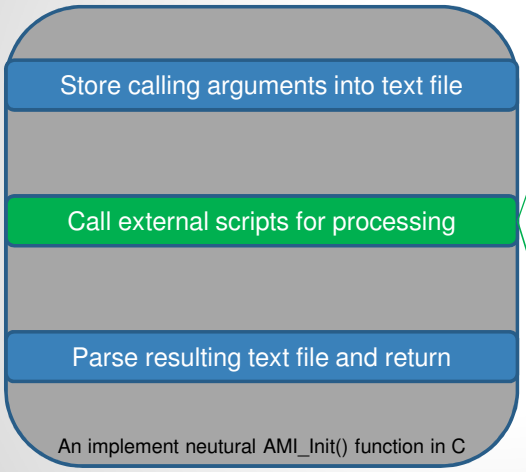
Modeling with Scripts: Example




```
clear
clc

%% file to load data from
inpFile = 'AMI_Init_Inp.txt';
%% file to save data to
outFile = 'AMI_Init_Out.txt';

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
%% Parse waveform data passed from the simulator
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
wave = parseInput(inpFile);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
%% Perform AMI_Init using Matlab
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
sample_per_bit = floor(bit_time / sample_interval);
preTap  = -0.05;
posTap  = -0.1;
mainSig = 1 - abs(preTap) - abs(posTap);
waveInp = wave;
ht = [[1 zeros(1, sample_per_bit-1)] * preTap ...
      [1 zeros(1, sample_per_bit-1)] * mainSig ...
      [1 zeros(1, sample_per_bit-1)] * posTap];
out=conv(wave, ht);
wave = out(1:size(wave, 2));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
%% Store waveform data to return to the simulator
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
storeOutput(wave, outFile)
```

9

Modeling with Scripts: Consideration

- Performance and distribuability:
  - Intepretor performance.
  - Redistributable (license)?
  - Does it require model user to install intrepreter?
- Consider Python! [5]
  - SciPy, NumPy etc for numerical analysis.
  - Embedded python: a single zip file together with AMI models.
  - Performance and extendability.

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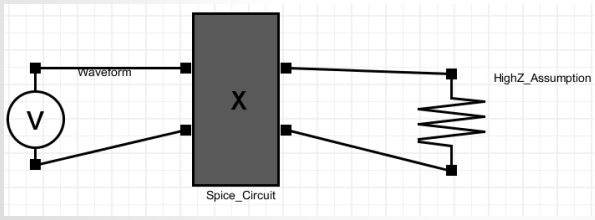
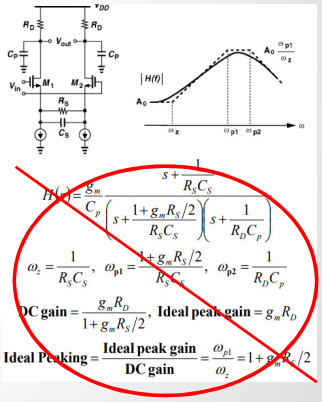
Modeling with Spice: Concept

- Dynamically generated PWL inputs:
  - High-Z assumption
  - Simulate
    - Circuit may need to provide GND.
  - Retrieve waveform and return





No need to code circuit behavior!

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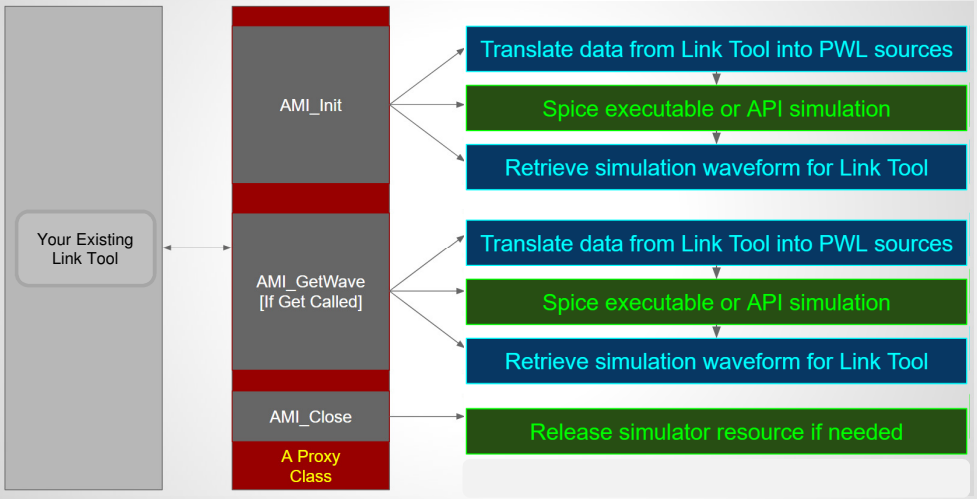
Modeling with Spice: Flow



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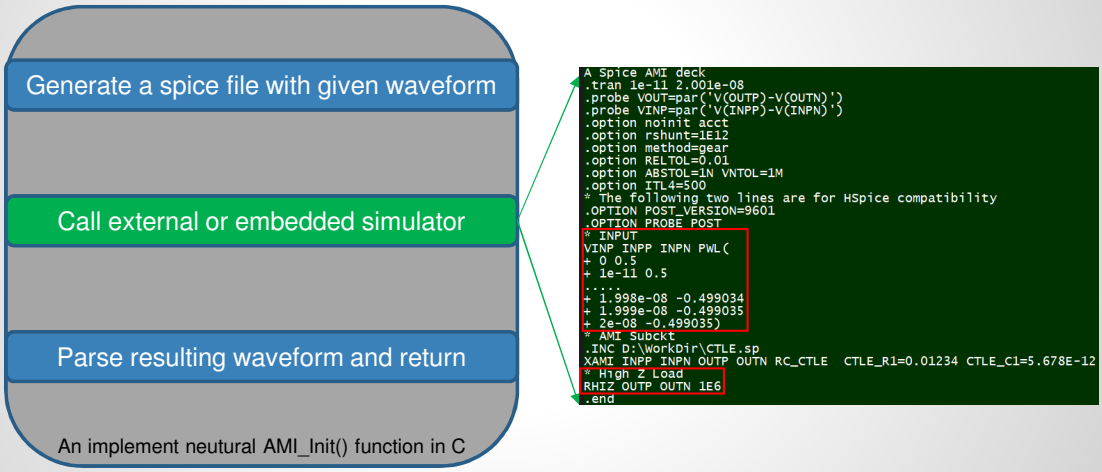
Modeling with Spice: Example



Modeling with Spice: Consideration

- Performance and distribuability:
  - Availability of device models?
  - Redistributable (license)?
  - Does model user need specific simulator?
- Consider open source simulator!
  - NgSpice, QUCS etc all supports API/Shared library [6]
  - The AMI model is basically a circuit simulator
    - Implement once, use many times!
  - Performance vs Accuracy

Summary:

- AMI model using scripts and spice circuit:
  - Doable! (Has been implemented! Example included.)
  - Can reduce AMI modeling time significantly
  - Can serve as an intermediate step toward full C/C++ implementation.
- Considerations:
  - Performance:
    - Not a concern if only AMI_Init is needed (called only once)
  - Model release:
    - Can the model be distributed and used easily?
  - A simple wrapper IBIS-AMI model is needed as a proxy.

15

References:

1. **High-speed Links Circuits and Systems** http://www.ece.tamu.edu/~spalermo/ecen720.html
2. **Simulating High-Speed Serial Channels with IBIS-AMI Models** http://literature.cdn.keysight.com/litweb/pdf/5990-9111EN.pdf?id=2095655
3. **IBIS V6.1 Spec. Section 10** http://ibis.org/ver6.1/
4. **AMI Analysis Using a Proxy Class** http://ibis.org/summits/feb17/
5. **Embedding python in another application** https://docs.python.org/3/extending/embedding.html
6. **NgSPice as a shared library** http://ngspice.sourceforge.net/shared.html

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Q & A

17

18 SPISim is an InSync member.

Leveraging IBIS Capabilities for Multi-Gigabit Interfaces

Ken Willis - Cadence Design Systems
Asian IBIS Summit,
Shanghai, PRC
November 13, 2017

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Overview

- In writing EDI CON paper “Signal Integrity Methodology for Double-Digit Multi-Gigabit Interfaces”, different IBIS modeling techniques were applied
- Wanted to share some of the IBIS modeling methods we’ve been using

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Agenda

- [External Model]
- AMI equalization adaptation
- Backchannel training
- Applying IBIS-AMI to DDR applications

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Agenda

- ***[External Model]***
- AMI equalization adaptation
- Backchannel training
- Applying IBIS-AMI to DDR applications

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Preliminary IBIS Modeling

- Can get started with:
  - Voltage swing
  - Pad capacitance
  - Output impedance
  - Rise time
- Even easier to model using [External Model] syntax

```
|
[Model]     pcie4_out
Model_type  Output
Polarity Non-Inverting
Vmeas =     0.5
|
|
| variable                                  typ         min         max
C_comp                                      0.50pF      0.50pF      0.50pF
[Temperature Range]                         20          80          -50
[Voltage range]                             1.0         1.0         1.0
|
|*****************************************************************************
[Pulldown]
|
|                        Voltage              I(typ)      I(min)      I(max)
|
                        -1.0000e+00          -2.0000e-02 -2.0000e-02 -2.0000e-02
                         0.0000e-00           0.0000e-00  0.0000e-00  0.0000e-00
                         1.0000e+00           2.0000e-02  2.0000e-02  2.0000e-02
|
|*****************************************************************************
[Pullup]
|
|                        Voltage              I(typ)      I(min)      I(max)
|
                        -1.0000e+00           2.0000e-02  2.0000e-02  2.0000e-02
                         0.0000e-00           0.0000e-00  0.0000e-00  0.0000e-00
                         1.0000e+00          -2.0000e-02 -2.0000e-02 -2.0000e-02
|
|*****************************************************************************
[Ramp]
|
| variable          typ               min               max
dV/dt_r        0.60/0.020n    0.60/0.020n    0.60/0.020n
dV/dt_f        0.60/0.020n    0.60/0.020n    0.60/0.020n
|
R_load = 50
|
```


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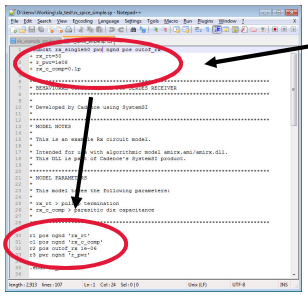
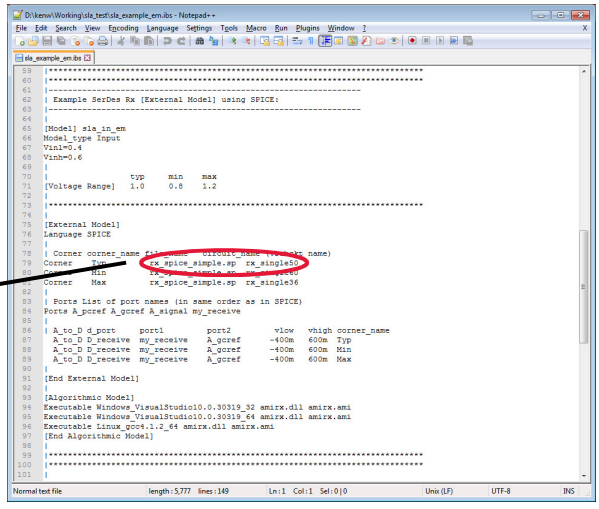
External Model

- Originally introduced in IBIS 4.1 !
- Enabled VHDL, Verilog-A, and Spice syntax to be used for buffer models instead of VI/VT table syntax
- Spice syntax has proven very useful to us





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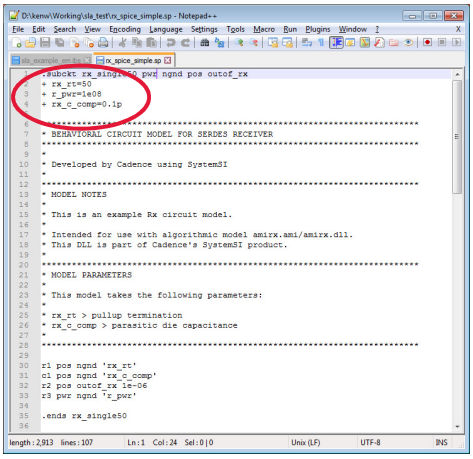
Spice [External Model]s Convenient for Early Feasibility

- Sometimes the IBIS model you want is not available for preliminary / pre-design analysis
- Easy to write (or use) simple parameterized Spice subcircuits for IO buffers when IBIS availability does not align with your project schedule
- Can sweep parameters and cover a big portion of the design space quickly and easily



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Analog Buffer Model Extensions

- Incorporated into IBIS 6.0

```
[External Model]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner    Typ          cdnstxrx.cir   tx_subckt
|
| List of parameters
Parameters  TSFile1     = cdns_tx.param(CDNS_Tx(Model_Specific(Tstonefile)))
Parameters  Tx_Rseries     = cdns_tx.param(CDNS_Tx(Model_Specific(Tx_R)))
|
| List of converter parameters
Converter_Parameters  Vtx_h = cdns_tx.param(CDNS_Tx(Model_Specific(Tx_V)))
|
| Ports List of port names (in same order as in SPICE)
Ports A_signal_pos A_signal_neg my_driveP   A_pdref  A_puref
|
| D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name polarity
D_to_A  D_drive  my_driveP  A_pdref  0  Vtx_h  0.05n  0.03n  Typ
|
|
[End External Model]
```

- Tx/Rx Model described in external file
  - Replaces the VI/VT curves
  - Can now be parameterized when Language 'IBIS-ISS' is used
- Parameter Definition is in a separate file
  - Similar to AMI Parameters
  - Can be in .ami or any other file
  - User Selects Parameter Values from GUI
- Parameter Value is passed to Simulator
  - Using.param, the parameter value is passed to the simulator
  - Converter_Parameters are used appropriately in the stimulus/D_to_A

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Agenda

- [External Model]
- ***AMI equalization adaptation***
- Backchannel training
- Applying IBIS-AMI to DDR applications

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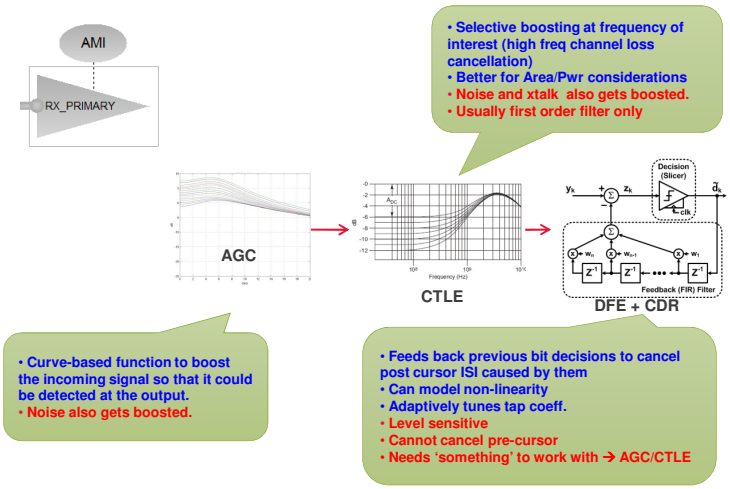
Anatomy of a Receiver AMI Model

- These different modules typically adapt at different rates
- Initial modules usually adapt more slowly than later ones



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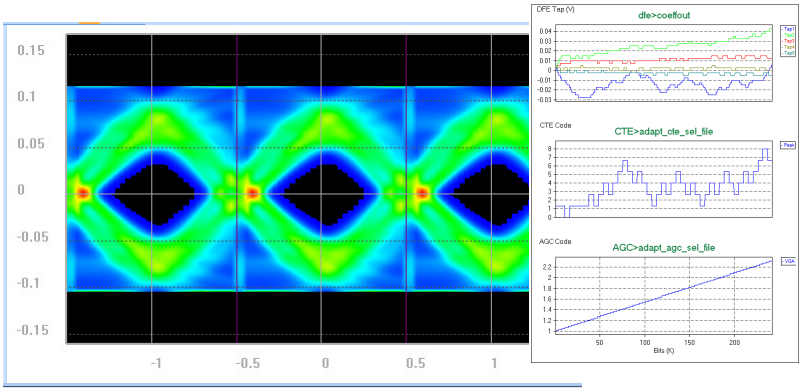
Rx With Default Adaptation

- Note that adaptation coefficients don't converge



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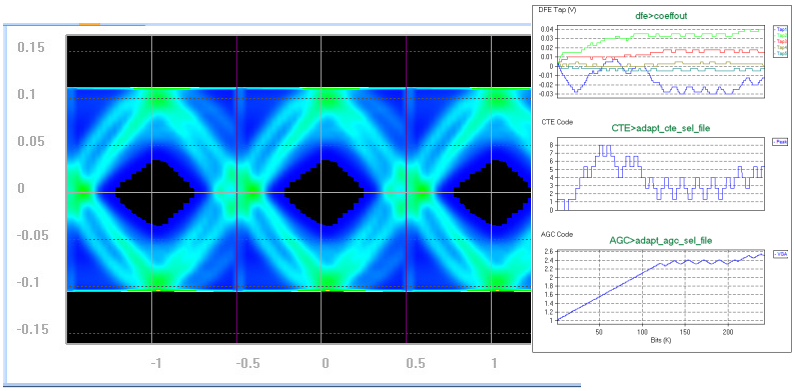
With Faster AGC Adaptation

- Coefficients converge, but after 150k bits of traffic are passed



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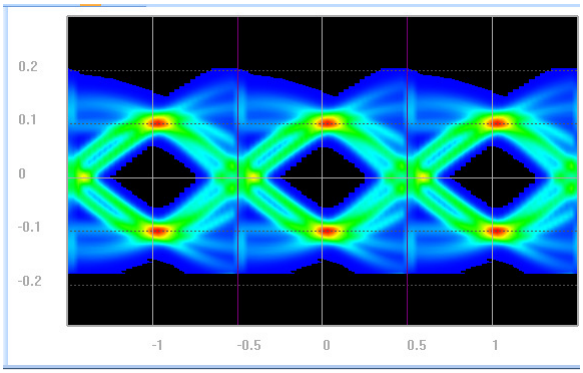
Ignoring the First 150k Bits

- Default was to ignore the first 40k bits
- Eliminates the noise from before coefficients converged
- Very important to be able to visualize how the adaptation is converging



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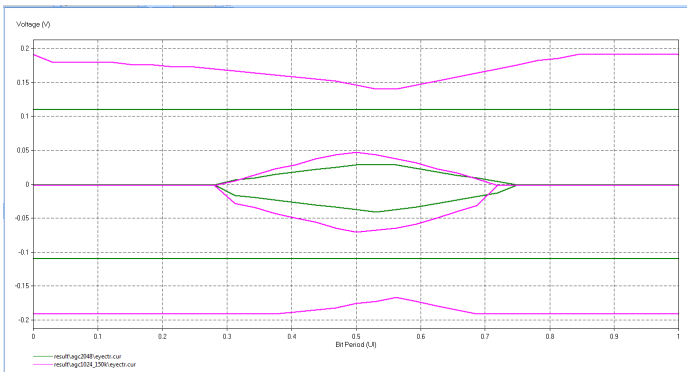
Original Eye Contour vs. Final

- Adjusting AGC adaptation time and Ignore_Bits made a significant difference in eye height



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Agenda

- [External Model]
- AMI equalization adaptation
- ***Backchannel training***
- Applying IBIS-AMI to DDR applications

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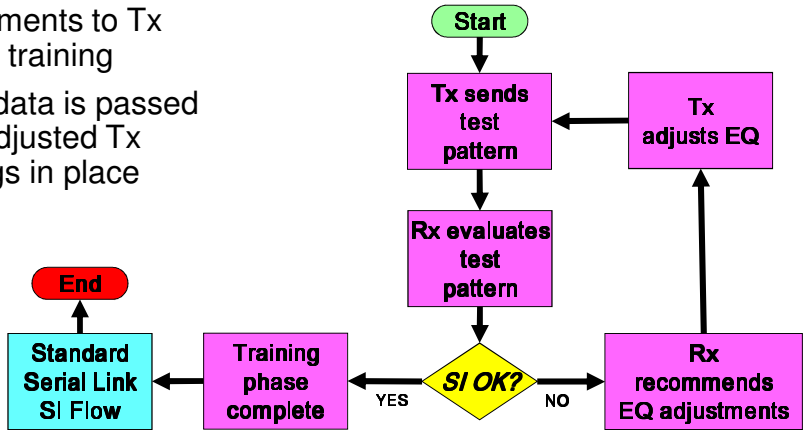
Backchannel Training (IBIS BIRD 147, in IBIS 7.0)

- Rx feeds back EQ adjustments to Tx during training
- Then data is passed with adjusted Tx settings in place



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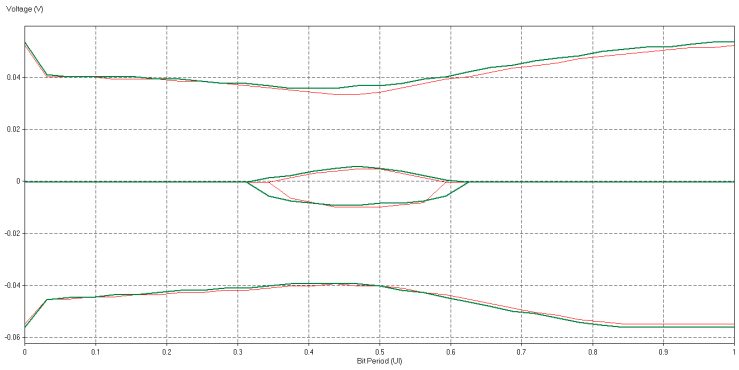
With and Without Backchannel

- Backchannel turned down Tx FFE settings somewhat
- Leaves more “heavy lifting” to Rx and its advanced adaptation
- Improves overall signal quality significantly



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Agenda

- [External Model]
- AMI equalization adaptation
- Backchannel training
- ***Applying IBIS-AMI to DDR applications***

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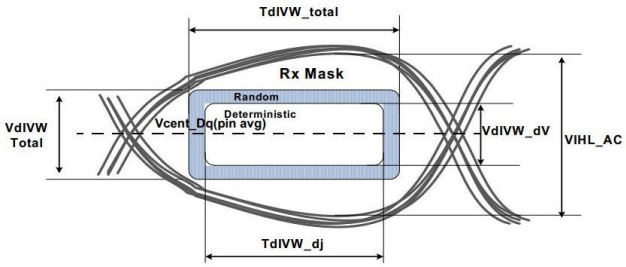
DDR4 Brought Some New Requirements

- Specified DQ mask compliance checking at a particular BER
- BER analysis requires extrapolation (bathtubs)
- Extrapolation requires a lot of traffic to be passed (need a lot of samples)
  - Channel simulation can be applied
- Started to see equalization used at Controller side
  - AMI modeling can be applied
- Worked with IP division to develop AMI model for DDR4 IP



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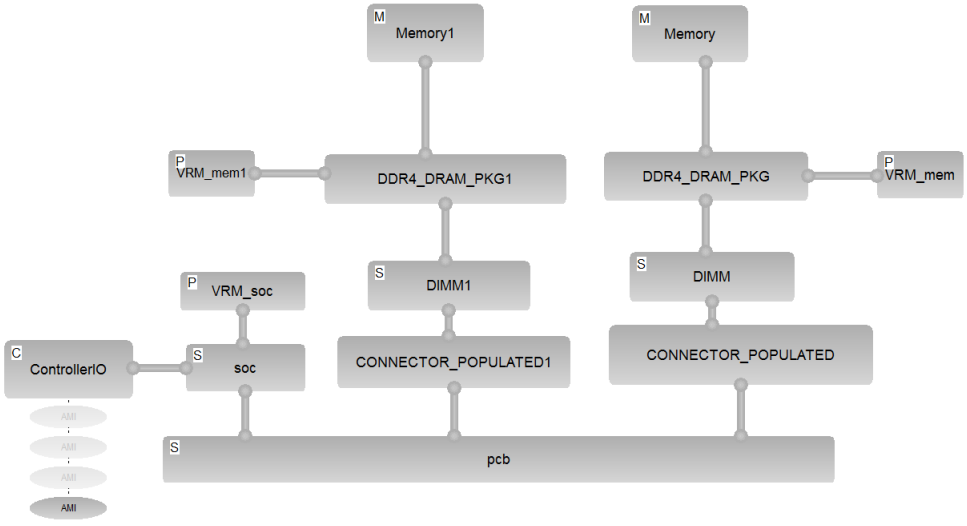
Simulation Testbench



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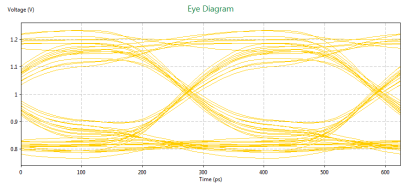
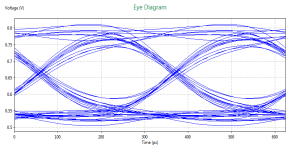
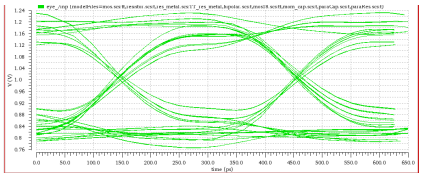
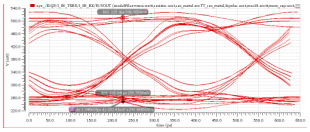
CTLE Correlation: 3200Mbps

	Input of receiver @pad	Output of CTLE
IBIS-AMI channel sim		
Transistor-Level circuit sim		

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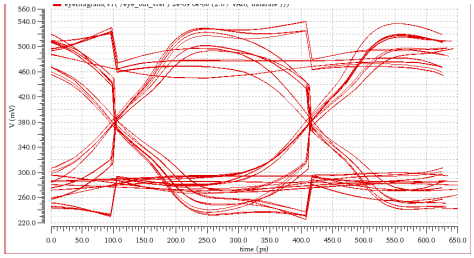
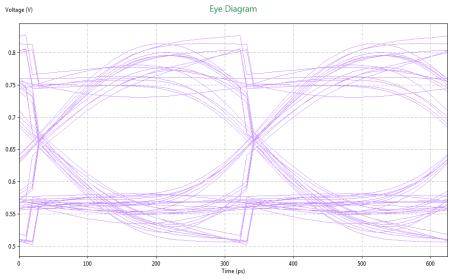
CTLE + DFE Correlation: 3200Mbps



Transistor-Level circuit sim



IBIS-AMI channel sim

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Summary

- External Model syntax can be very useful for pre-design modeling, when detailed IBIS models are not available, and has had some recent additions in capability
- Building IBIS-AMI models is not the obstacle it used to be
- Adaptive equalization often has interplay between multiple sub-modules in real devices, and therefore also in AMI models
- If adaptive, understand if your EQ coefficients converge during simulation
- Backchannel training enables interplay between the Tx and Rx in simulation, and can produce more realistic results for devices that use backchannel
- Channel simulation and AMI modeling has been successfully applied to DDR4 IP (and more of this is expected with DDR5)

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