Asian IBIS Summit, Tokyo, Japan

Simulation Technology for Memory Designers in DDR4/5

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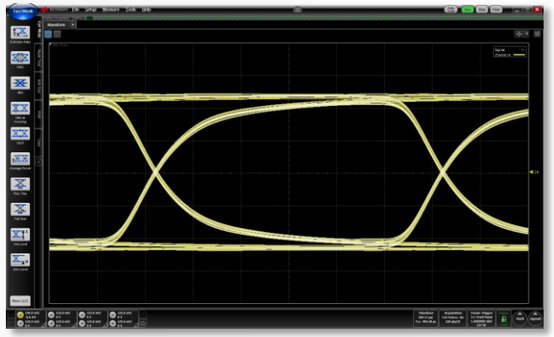
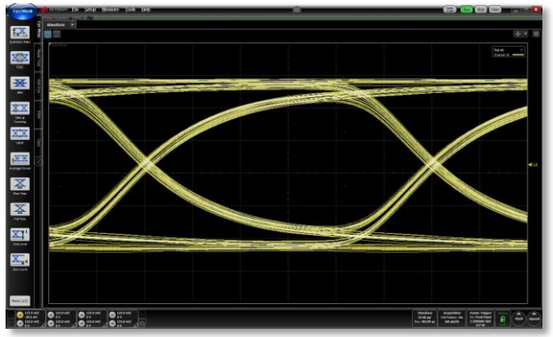
DDR5 is coming

The data eye is closing



1600



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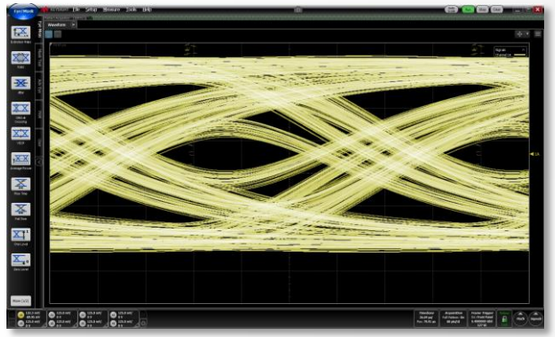

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- Memory channel BW limited
- Rj improving slowly
- Xtalk effects increasingly severe

ISI + Jitter + Xtalk → Closed Eye

Agenda

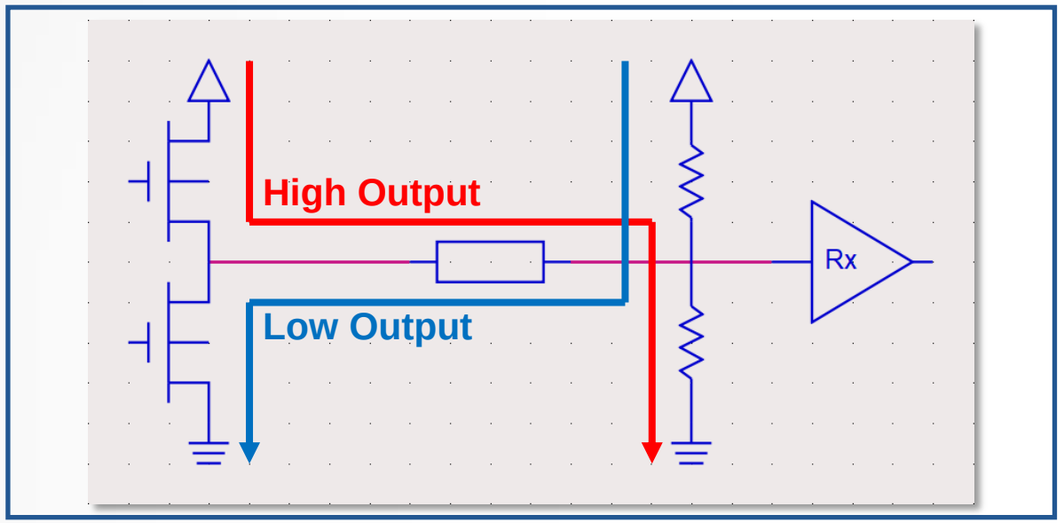
- DDR4 Highlights
- 4 challenges for memory designers in DDR4/5
- A Look at JEDEC’s current DDR5 proposal
- How will we model DDR5 devices in simulation?
- A side-by-side comparison of some approaches for DDR5 simulation

LP/DDRx Highlights

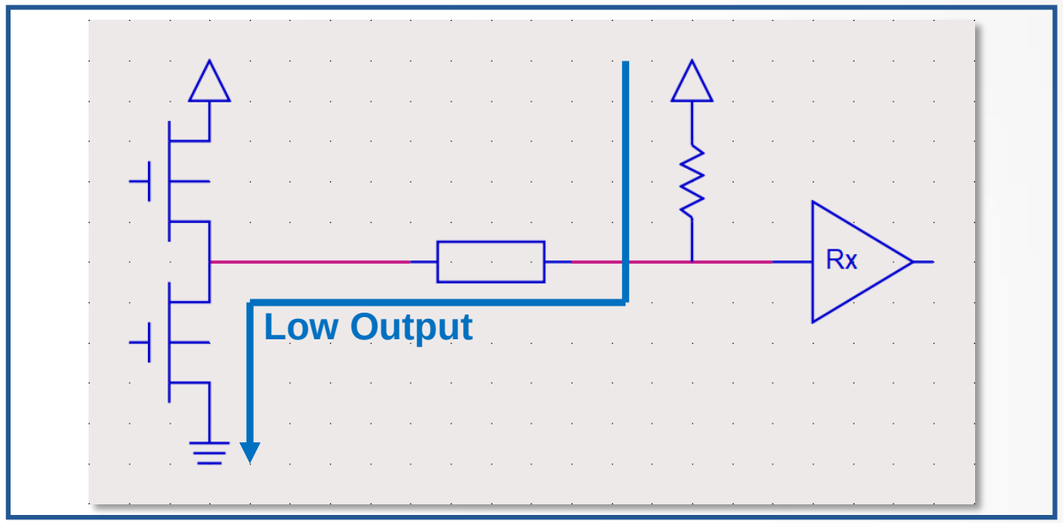
Specification	DDR3	DDR4	LPDDR4
Data Rate / Pin (Mbps)	800 - 2133	1600 - 3200	1333 - 4266
Bus Width	4, 8, 16	4, 8, 16	2, 4, 16, 32
Voltage	1.5 / 1.35	1.2	1.1
Vref	External Vref (=Vref/2)	Internal Vref	Internal Vref
Signal Evaluation	Setup/Hold time	Mask (considered BER)	
Data I/O	CTT (Center Tapped Termination)	POD (Pseudo Open Drain)	LVSTL (Low Voltage Swing Terminated Logic)

LP/DDRx Highlights

DDR3 - CTT (Center Tapped Termination)

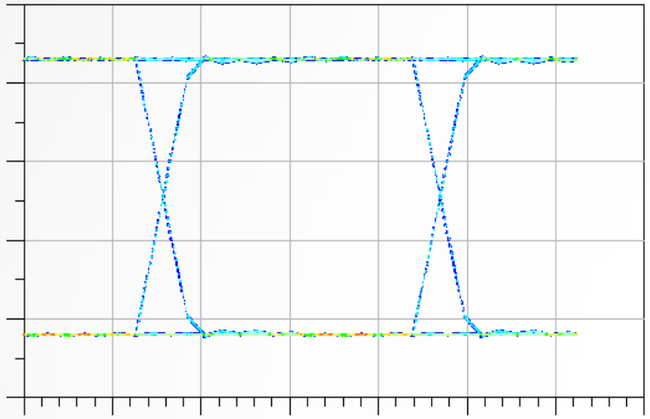


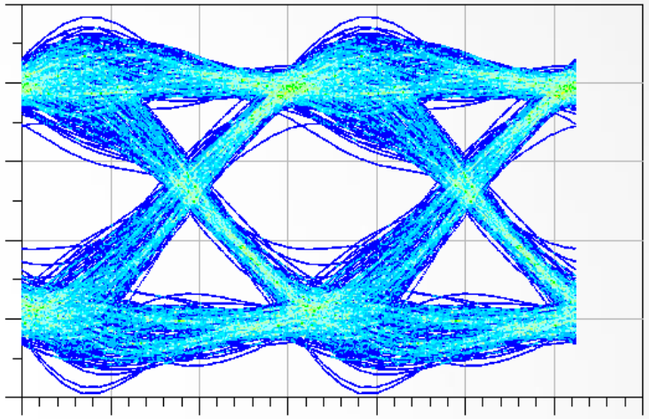
DDR4 - POD(Pseudo-Open Drain)

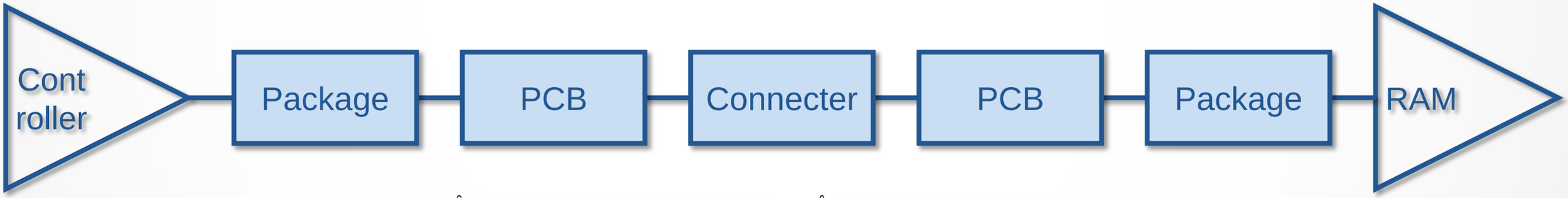


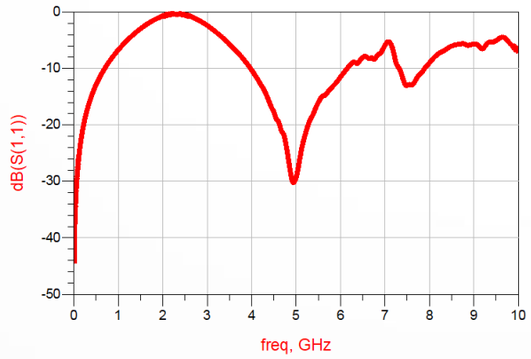
- Lower VDD voltage and Pseudo-Open Drain (POD) reduces power consumption by 40%.
- Internal VREF training performed within the IC receiver, to optimize VREF level. Retraining at regular intervals.
- Data lines are calibrated at the IC, to reduce their skew to the strobe.
- Data Bus Inversion (DBI).

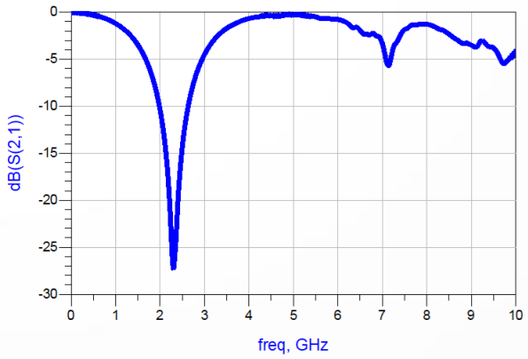
Shrinking eye due to package, PCB and connectors





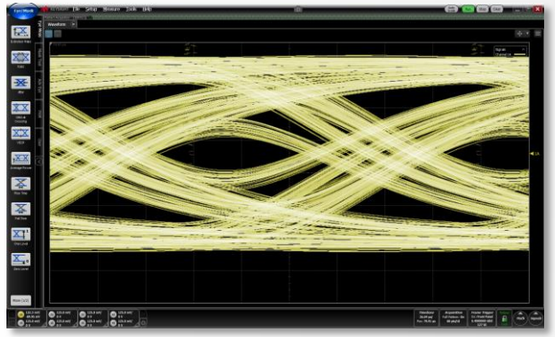






Today's Disruption

The fuzzy eye takes over



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LP/DDR4 receiver requirements defined by masks instead of setup / hold and DC voltage swings

LPDDR4

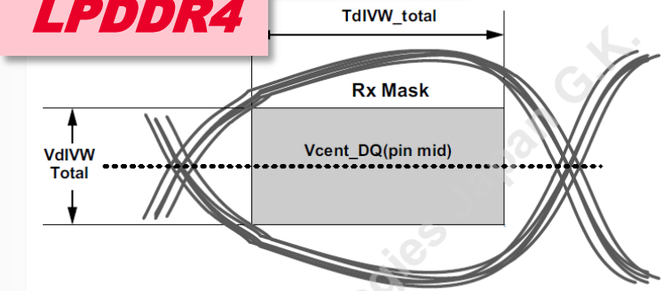


Figure 177 — DQ Receiver(Rx) mask

DDR4

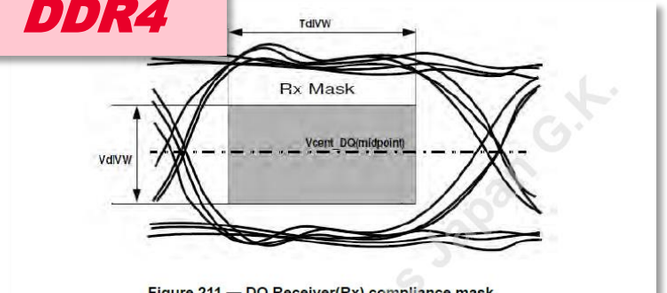


Figure 211 — DQ Receiver(Rx) compliance mask

Source : JEDEC Standard JESD209-4B/JESD79-4B

- Simpler definition of DRAM requirements and system design.
- More compatible with LPDDR4 training procedures.
- Eliminates troublesome slew rate derating.
- Bit Error Rate (BER) spec recovers timing and noise margin.

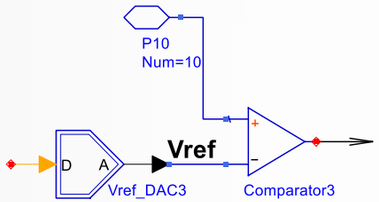
Fundamental paradigm shift with DDR4

What is a mask ?

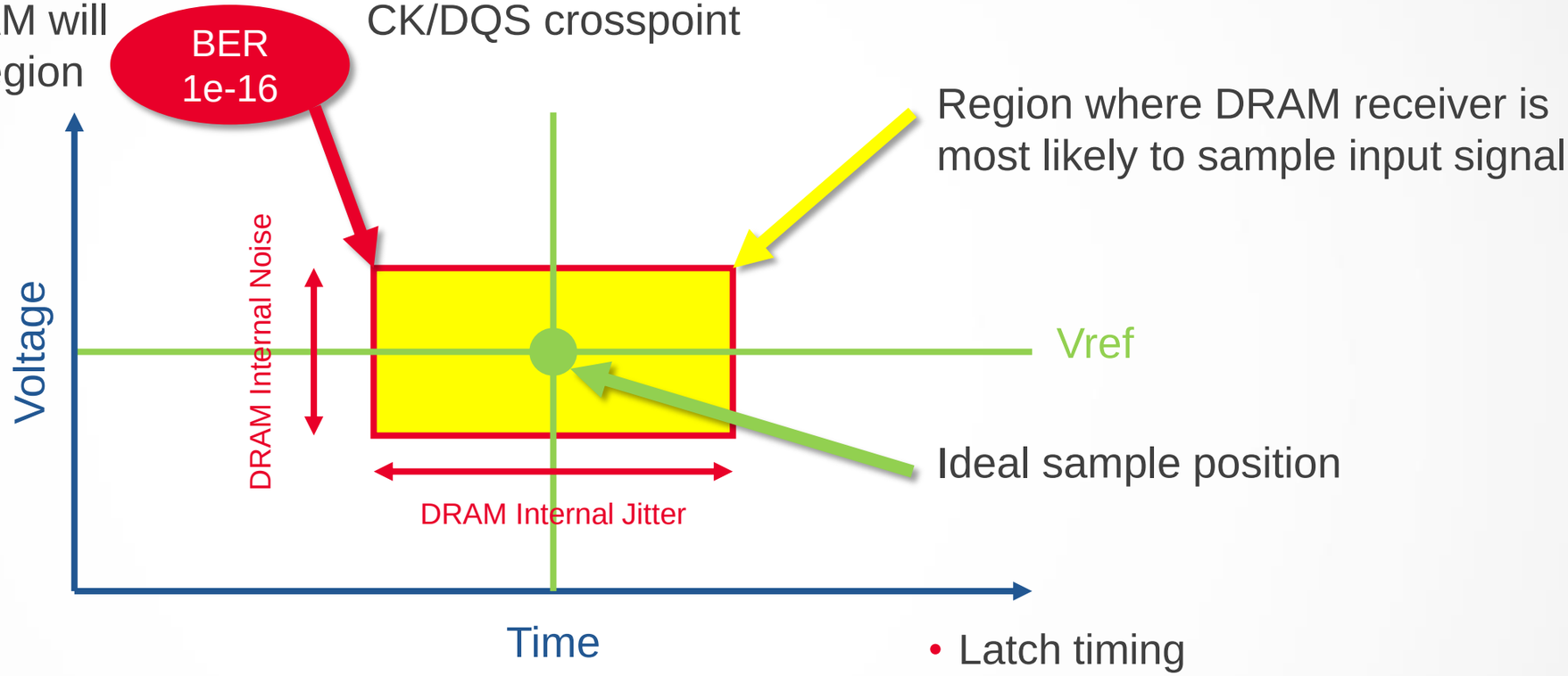
Source : JEDEC Standard JESD209-4B

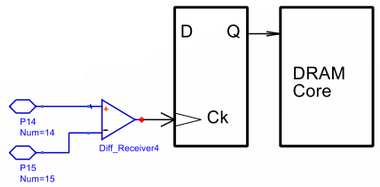
NOTE 2 The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.

BER = Probability that DRAM will sample outside the mask region



- DAC quantization error
- Comparator hysteresis
- Comparator offset error
- Internal noise and crosstalk





- Latch timing
- Clock receiver hysteresis
- DRAM internal skews
- Internal noise converted to jitter

Challenges for DDR4/DDR5

Challenge #1

Timing margin will be further eroded by ISI and RJ; The Rx Mask becomes the contract between Controller and DRAM in order to achieve at least prescribed BER (1e-16 for DDR4).

Source : JEDEC Standard JESD209-4B

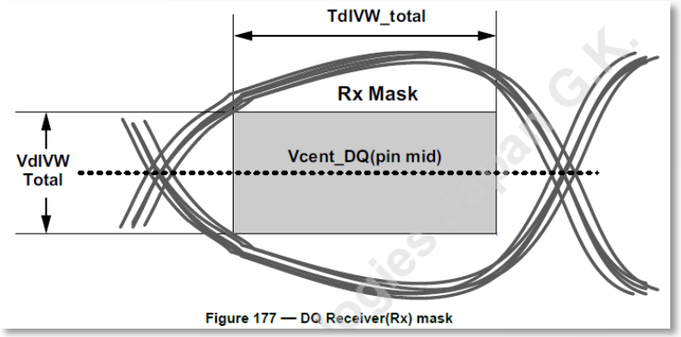
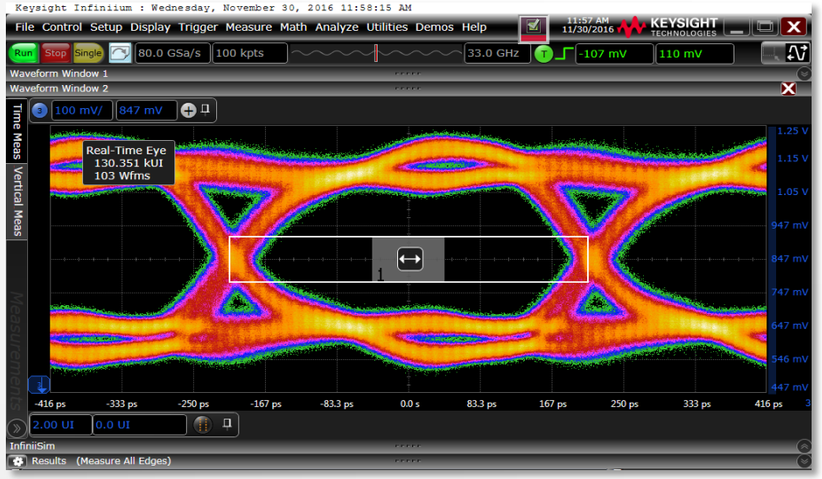
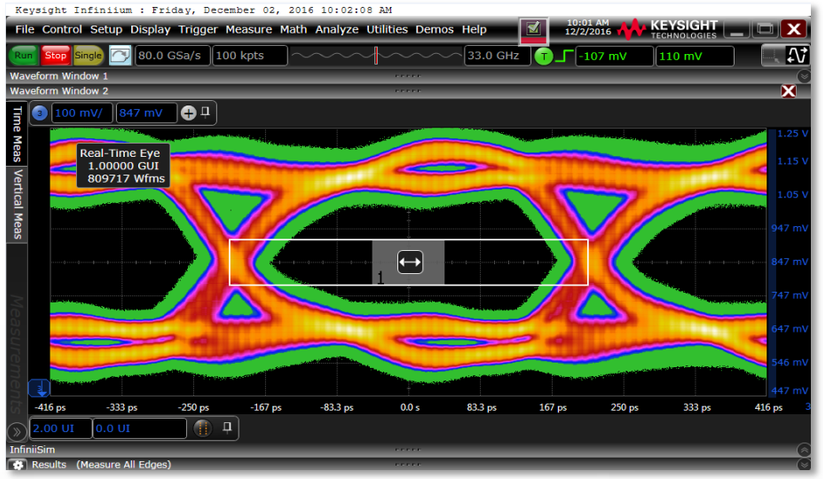


Figure 177 — DQ Receiver(Rx) mask

EH and EW keep shrinking at lower BER



13,000bits



1e9bits

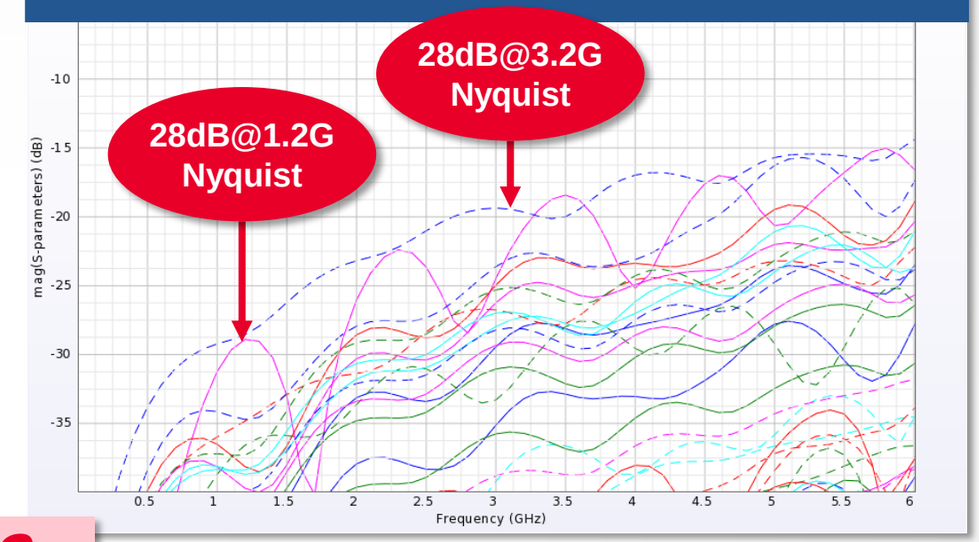
Number of UI	BER	Eye Width	Eye Height
1.3e5	7.69e-6	352.72 ps	310.9 mV
2.80e6	3.57e-7	347.52 ps	288.3 mV
6.31e7	1.58e-8	339.70 ps	275.8 mV
1.10e8	9.13e-9	339.06 ps	271.1 mV
1e9	1e-9	336.45 ps	265.6 mV

Challenges for DDR4/DDR5

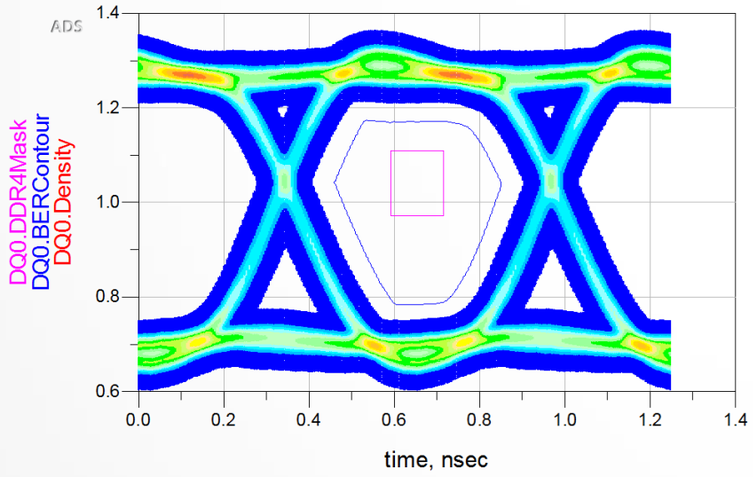
Challenge #2

Crosstalk.
As the speed increases, so does the amount of coupling between adjacent neighbors.

NEXT & FEXT in PCB routing

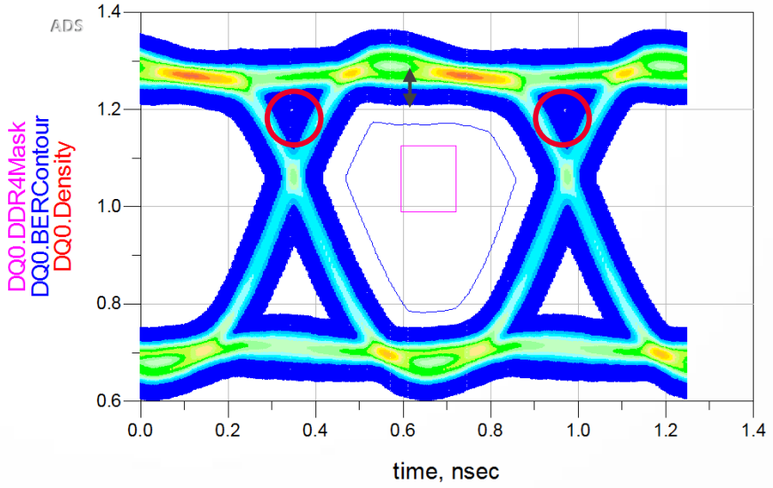


DQ0



1600MHz DDR4 No XTalk

DQ0



1600MHz DDR4 Active Byte-Lane of DQ Signals (Xtalk)

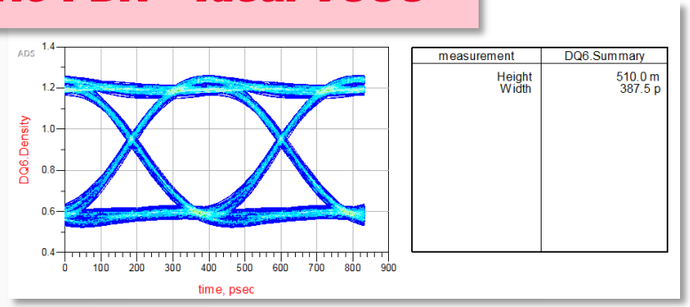
Even at slow speed grades the additional noise reduces margin to mask!

Challenges for DDR4/DDR5

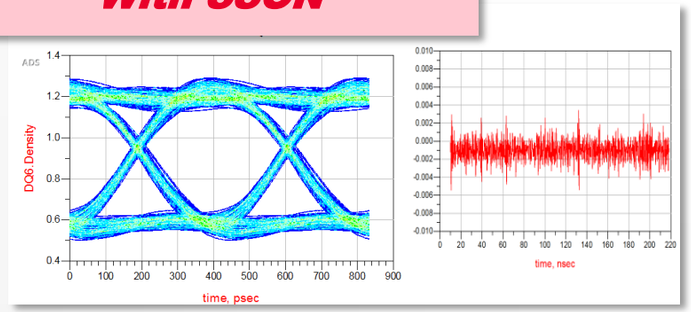
Challenge #3

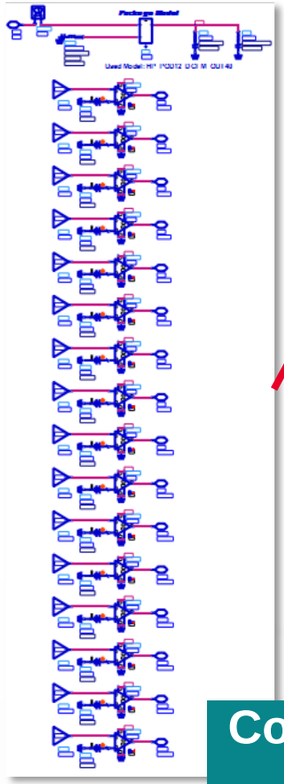
Additional jitter and amplitude noise due to Simultaneous Switching Noise (SSO/SSN) and other time-varying distortions.

No PDN – Ideal VCCO

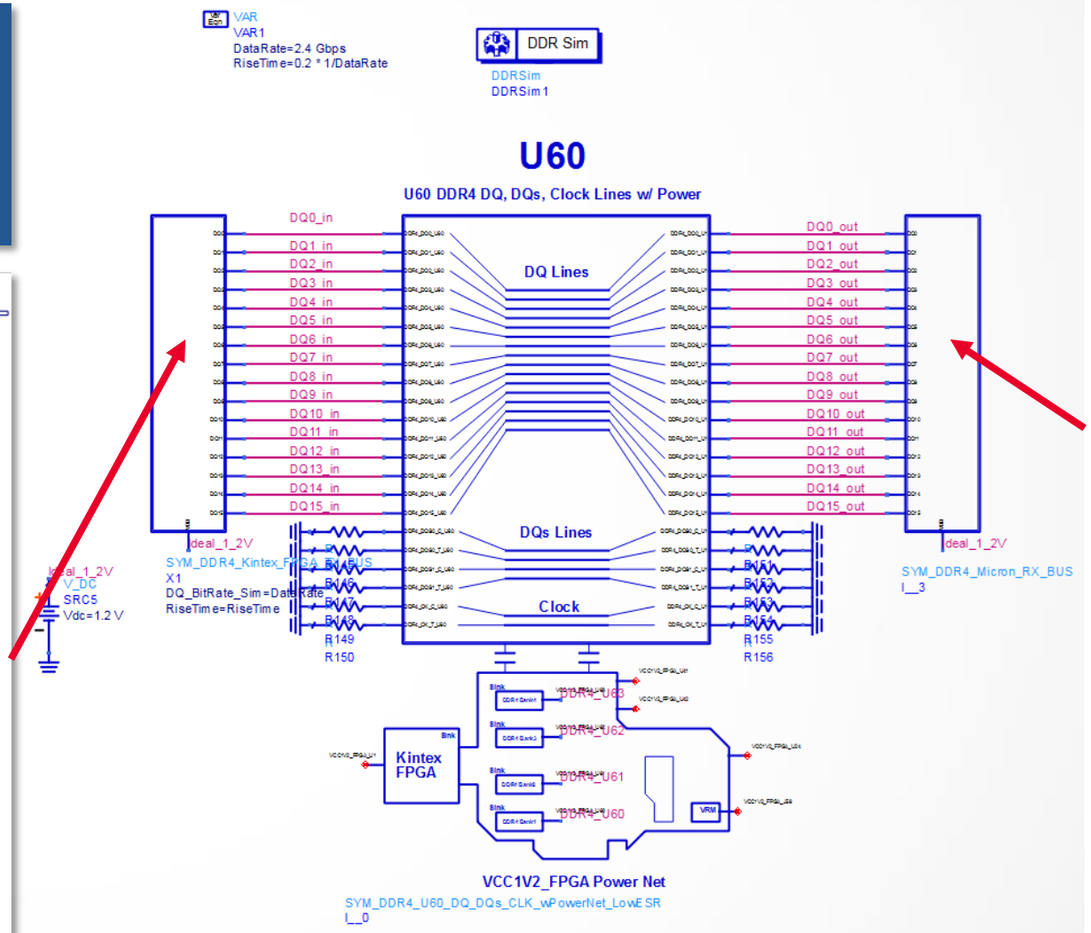


With SSON





Controller IBIS

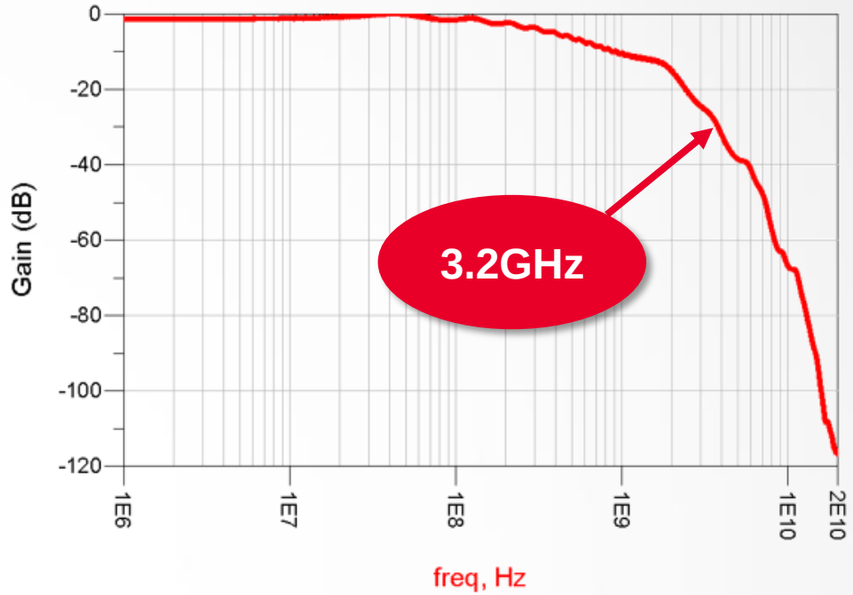


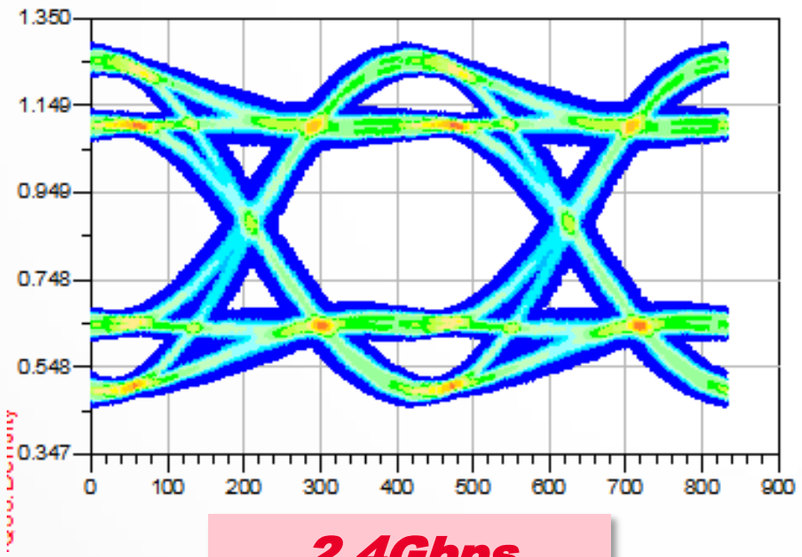
RAM IBIS

Challenges for DDR5

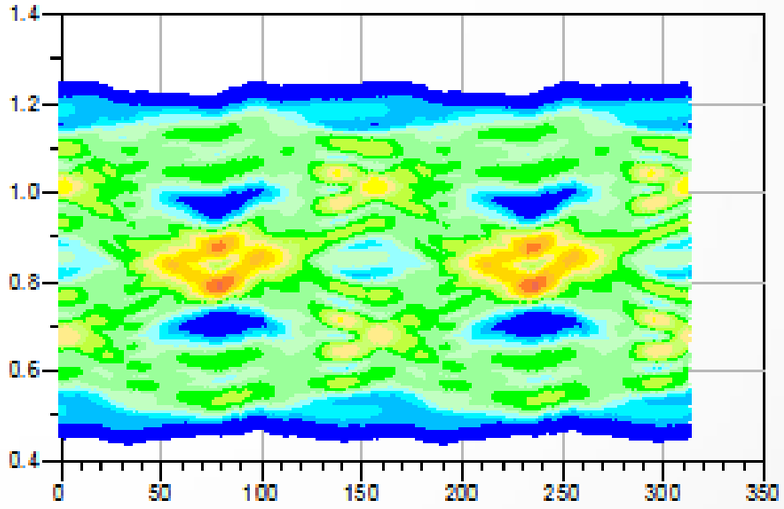
Challenge #4

Channel attenuation and ISI becomes more significant so tunable Equalization (De-emphasis, DFE) on Tx and Rx become necessary to deal with closed eyes.



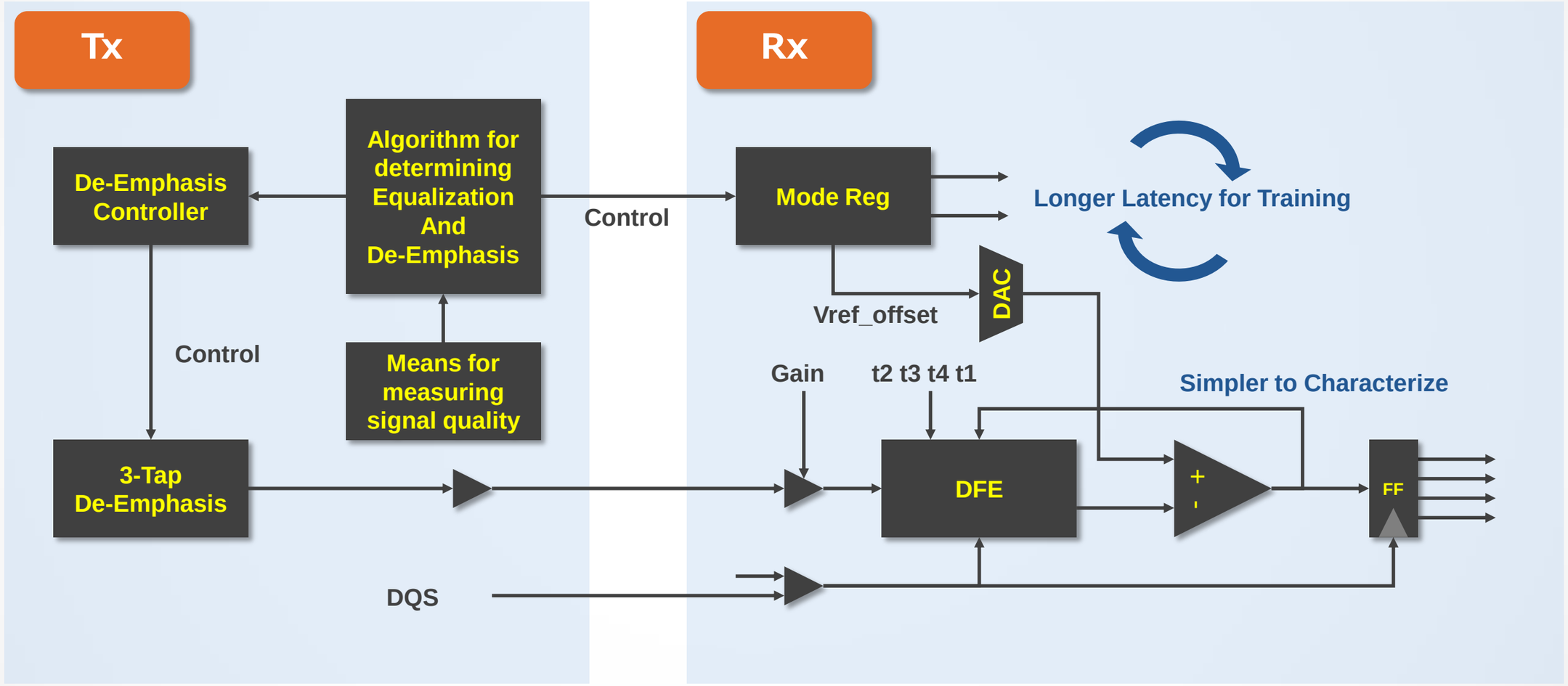


2.4Gbps

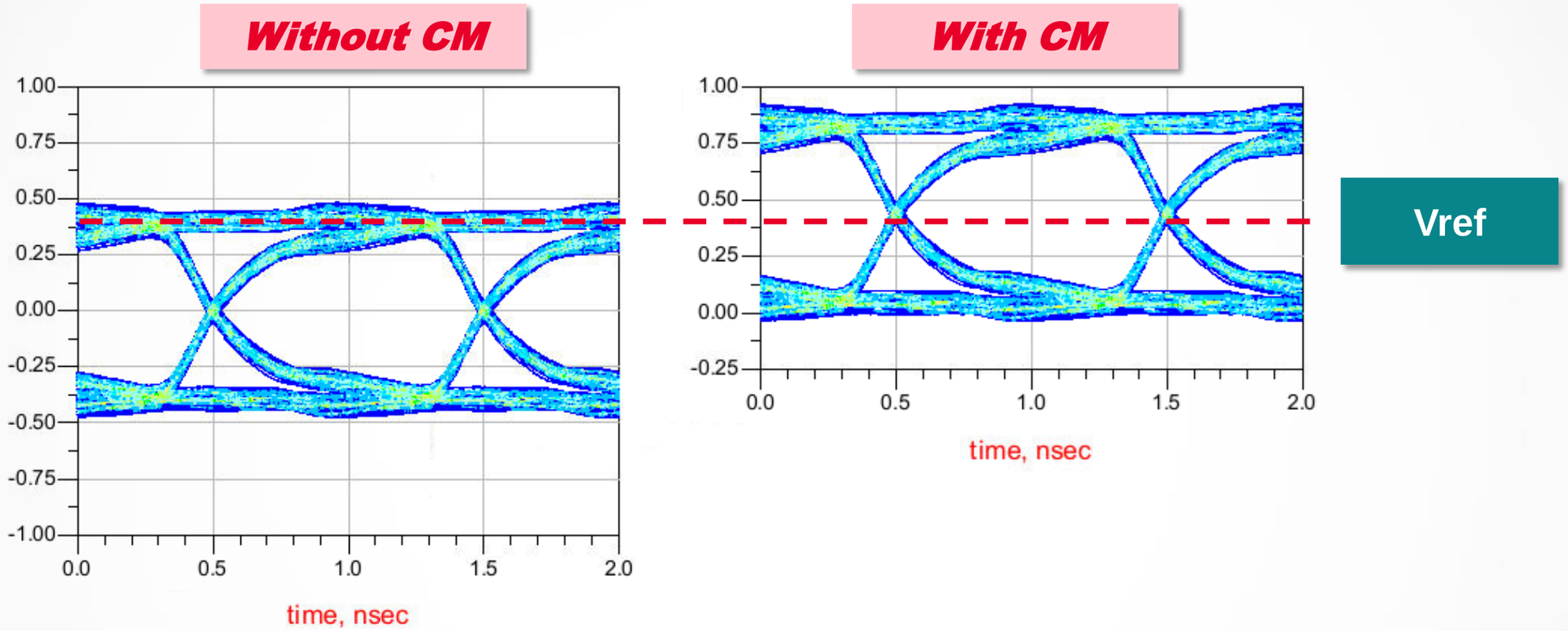


6.4Gbps

DDR5 current proposal



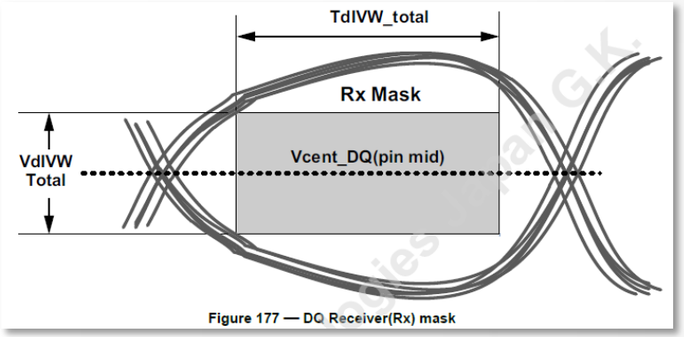
Common-mode problem in IBIS-AMI



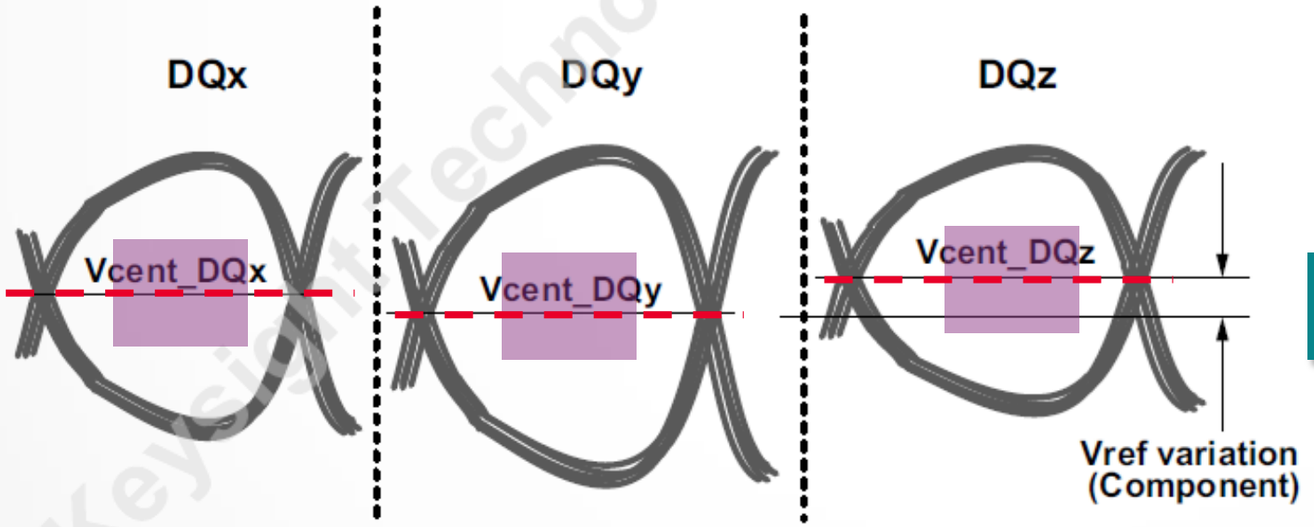
- IBIS-AMI only defines differential signal.
  Common-mode (CM) in single-ended (SE) signal is undefined and thrown away.
- IBIS-AMI waveform always centers at 0V.
  Signal level is off compared to Vref.

Common-mode implications

- One of the key implications of having the DC offset thrown away, is that margin to the **Rx BER Mask requires correct DC offsets** (to know where to place the mask).
- In other words, there is a single Vref for the entire byte-lane. The spec defines the Rx Mask to be centered on Vcent_DQ.



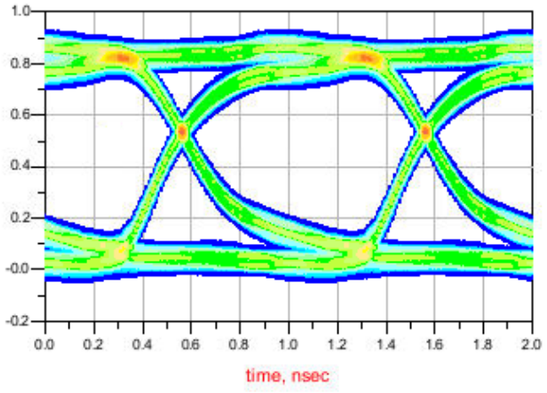
Source : JEDEC Standard JESD209-4B



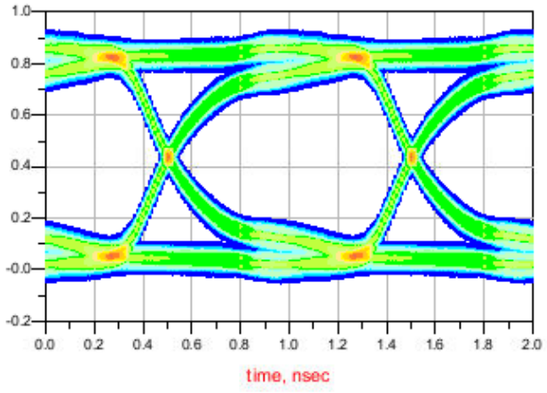
Vcent_DQ

Asymmetric Rise and Fall Edges in Single-ended Signal

Rise time < Fall time



Rise time = Fall time



- Asymmetric rise and fall edges lead to data DCD jitter and crossing level shift, degrading timing and voltage margins with respect to Rx mask.
- Pull-up and pull-down behaviors depend on the analog channel and therefore must be included in analog channel response characterization.
- AMI has only one impulse response and can't capture difference between rise and fall edges. Response needs to be characterized separately for each edge.
- Asymmetry between rise and fall edges is much more severe in single-ended signal than in differential signal. It gets worse as data rate increases.
- With different responses for different edges, IBIS-AMI's convolution scheme is no longer applicable. Moreover, Tx GetWave output waveform becomes useless as a result.

Current Proposals in the EDA Community

DDR5 approaches

Statistical DDR Bus

- Sim speed: Very Fast

- Pros:
  - Calculates **ultralow BER contours** (e.g. 1e-16) for Rx BER mask
  - **Correct Eye Shape** and **DC offset!**
  - Finds **optimal DFE tap** weights
  - In the future can be extended to support Bit-by-Bit mode
  - Simplicity of EQ modeling

- Cons:
  - **No non-linear or time-varying effects**.
  - IP protection not standardized

IBIS-AMI

- Sim speed: Fast

- Pros:
  - Well-defined **model interface** / concealment of IP
  - Can support both **statistical** and **bit-by-bit** simulations
  - Future possibility for back-channel adaption

- Cons:
  - **Incorrect Eye-shape** and DC offset
  - **Complexity** of modeling
  - **No non-linear or time-varying effects**

SPICE + Verilog-A

- Sim Speed: Very Slow

- Pros:
  - Captures all **non-linear and time-varying effects**

- Cons:
  - **Impractical** to simulate enough bits to ever extrapolate BER contours accurately to 1e-16!
  - Sharing of **encrypted HSPICE** models requires HSPICE
  - Verilog-A implementation **complexity** and requires compiled Verilog-A for IP protection (not supported in all tools)
  - Simulator support for **sweeps?**

KEYSIGHT
TECHNOLOGIES