How to Fix DDR4 Signal Integrity Issue about “Pin”and “Die”

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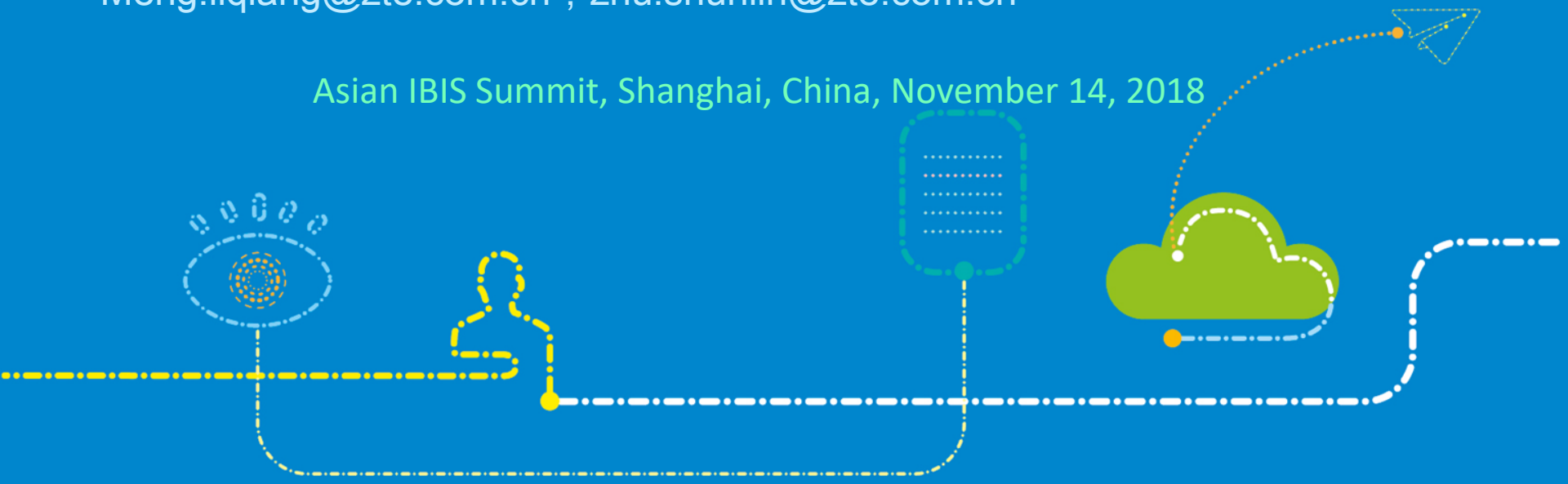


Agenda

- Overview
- “Pin” and “Die” Specification in IBIS Model
- Comparative Analysis of two Simulation Cases
- Design Considerations for the Next Generation of DDR
- Summary

Overview DDRx Evolution Trend

JEDEC Standards for DDRx

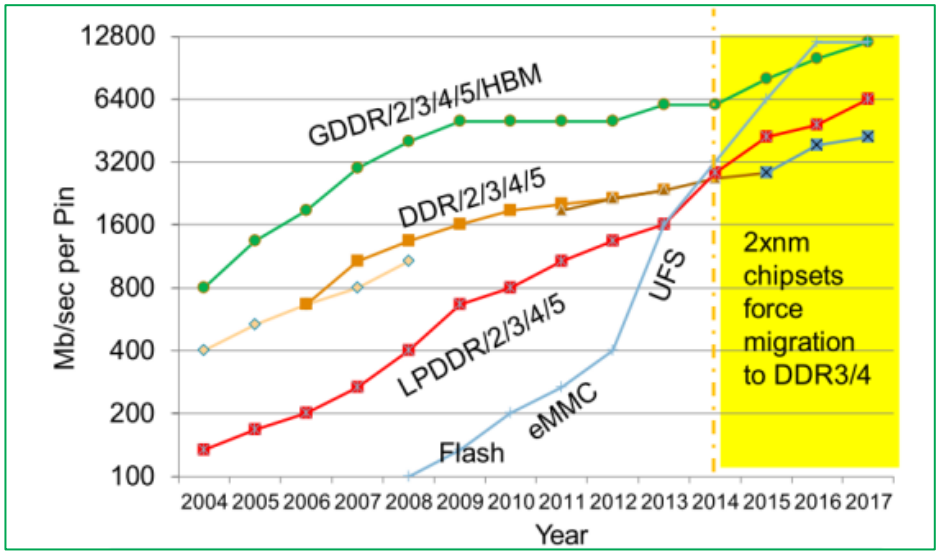
- DDR4 JESD79-4B JUNE 2017
- DDR5 publication is forecasted for 2018 [Ref2]

DDRx Speed

- DDR4 3200MT/S
- DDR5 reach up to 6400MT/S

DDRx Model

- DDR4 [IBIS ver] 5.1
- DDR5 [IBIS ver] ?



[Ref1]

Ref1: DDR4/LPDDR4: A Practical Design Methodology or High-Speed Memory Systems ,April 12th, 2015， page7, Keysight, Stephen Slater，
https://www.keysight.com/upload/cmc_upload/All/HSDSeminarPaper1.pdf
Ref2 :https://www.jedec.org/news/pressreleases/jedec-ddr5-nvdimm-p-standards-under-development

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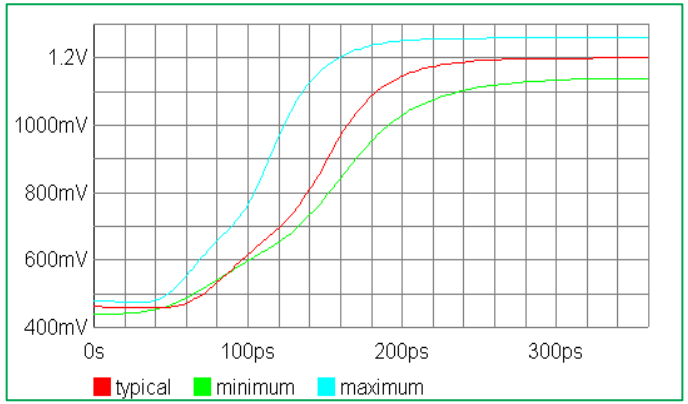
[Package]& [Pin] Information in IBIS Model

- The [Package Model] data overrides the values in the [Package] keyword. Regardless, the data listed under the [Package] keyword must still contain valid data.
- Six columns for Pin can be used to override the default package values (specified under [Package]) FOR THAT PIN ONLY. When using six columns, the headers R_pin, L_pin, and C_pin must be listed.[Ref3]
- Priority ranking [Package Model] > [Pin] > [Package]

```
[Package]
| variable       typ                min                max
R_pkg            200.00m            100.00m            300.00m
L_pkg            2.00nH             1.00nH             3.00nH
C_pkg            1.35pF             1.20pF             1.50pF
|
[pin]   signal_name          model_name R_pin           L_pin          C_pin
AM56    DDRA_A0_A7A8         d4_addr    3.30E+03mOhm    5.33E+00nH     2.81E+00pF
AN51    DDRA_A10             d4_addr    2.56E+03mOhm    4.19E+00nH     1.62E+00pF
AT54    DDRA_A11             d4_addr    3.28E+03mOhm    5.16E+00nH     2.57E+00pF
AR54    DDRA_A12             d4_addr    3.31E+03mOhm    5.20E+00nH     2.60E+00pF
AN49    DDRA_A13             d4_addr    1.84E+03mOhm    3.24E+00nH     1.54E+00pF
```

```
[Pin]     signal_name       model_name  R_pin  L_pin  C_pin
A31       c0_ddr4_dqs_c[3]  |HP_POD12_DCI_F_OUT40_IN60_PE2400
|
[Package Model]      Controller D
```



- There may be some misunderstanding between R_pin /L_pin/C_pin and R_pkg/L_pkg/C_pkg when running corner simulation,Which one will the tool call?

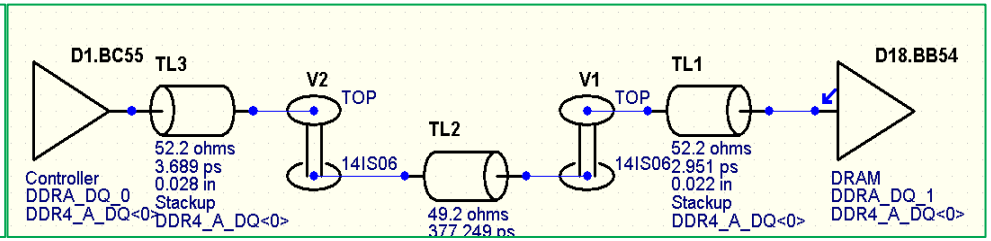
Ref3：I/O Buffer Information Specification IBIS Version 6.1 page 21， http://ibis.org/ver6.1/ver6_1.pdf

[Package]& [Pin] Information in IBIS File

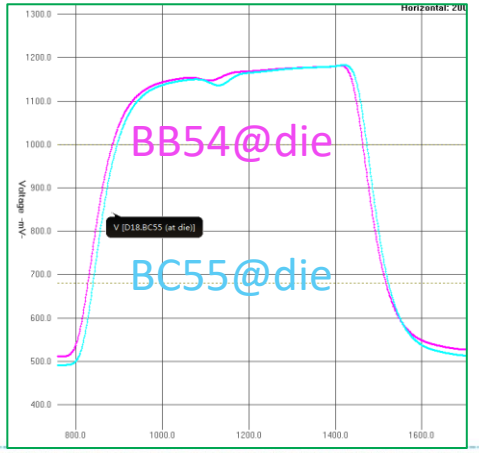
There may be some misunderstanding between Package typ min max in model and Slow-Weak ,Typical , Fast -Strong mode in simulation because R_pin/L_pin/C_pin has only one value for specified pin, but [Package] has three different value.

The typical (typ) column must be specified. If data for the other columns are not available, they must be noted with “NA”, so three experiments show that R_pin, L_pin, and C_pin only override the default package typical values. For example, experiment 2 with/without Package model under slow corner simulation, they have the same waveform.

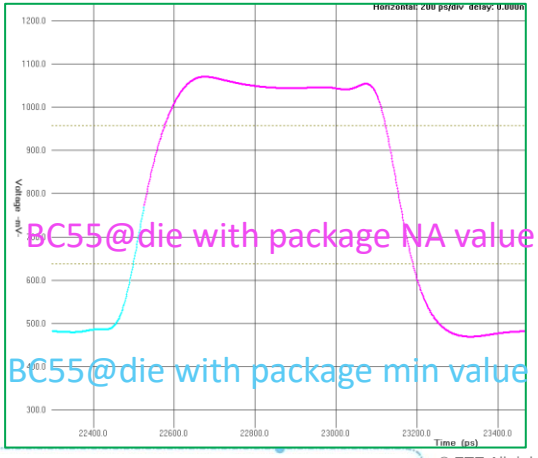
```
[Component]      DRAM
[Manufacturer]   VendorC
|Package         Generic
[Package]
| variable       typ              min              max
R_pkg            0.0001m          99.3m            1875m
L_pkg            0.0001nH         1.39nH           11.94nH
C_pkg            0.0001pF         1.44pF           5.68pF
|
[pin]   signal_name      model_name R_pin          L_pin          C_pin
BC55    DDRA_DQ_0        d4_dq      NA     NA     NA
BB54    DDRA_DQ_1        d4_dq      3.77E+03mOhm   6.02E+00nH     2.73E+00pF
AM56    DDRA_A0_A7A8     d4_addr    3.30E+03mOhm   5.33E+00nH     2.81E+00pF
```



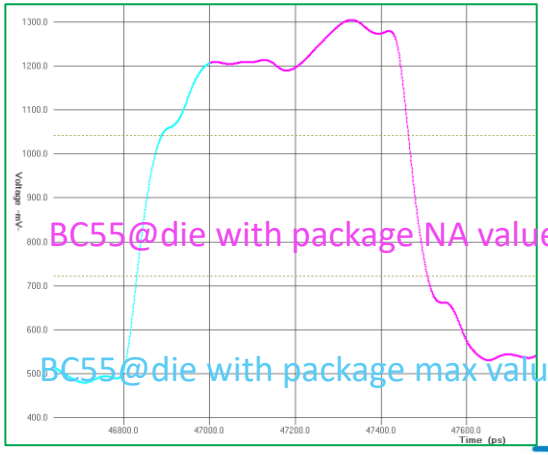
Experiment 1 Using BC55 and BB54 pin for typical corner simulation



Experiment 2 Using BC55 for Slow corner simulation by setting Packge min wtih default and NA value



Experiment 3 Use BC55 for Fast - Strong corner simulation by setting Packge max wtih default and NA value



Si_location and Timing_location

Model default loaction

- Si_location pin
- Timing_location pin

5 COMPONENT DESCRIPTION

Keyword: **[Component]**

Required: Yes

Description: Marks the beginning of the IBIS description of the integrated circuit named after the keyword.

Sub-Params: Si_location, Timing_location

Usage Rules: If the .ibs file contains data for more than one component, each section must begin with a new [Component] keyword. The length of the component name must not exceed 40 characters, and blank characters are allowed.

NOTE: Blank characters are not recommended due to usability issues.

Si_location and Timing_location are optional and specify where the Signal Integrity and Timing measurements are made for the component. Allowed values for either subparameter are "Die" or "Pin". The default location is at the "Pin".

Example:

```
[Component]      7403398 MC452
|
Si_location      Pin     | Optional subparameters to give measurement
Timing_location Die      | location positions
```

Modify for auto measurement

- Si_location Die
- Timing_location Die

```
[Component]       DDR4_Controller
Timing_location Die
[Manufacturer]    A
|Package          Generic
[Package]
| variable        typ                min                max
R_pkg             200.00m            100.00m            300.00m
L_pkg             2.00nH             1.00nH             3.00nH
C_pkg             1.35pF             1.20pF             1.50pF
|
[pin]    signal_name          model_name R_pin           L_pin          C_pin
AM56     DDR4_A0_A7A8         d4_addr    3.30E+03mOhm    5.33E+00nH     2.81E+00pF
AN51     DDR4_A10             d4_addr    2.56E+03mOhm    4.19E+00nH     1.62E+00pF
AT54     DDR4_A11             d4_addr    3.28E+03mOhm    5.16E+00nH     2.57E+00pF
AR54     DDR4_A12             d4_addr    3.31E+03mOhm    5.20E+00nH     2.60E+00pF
```

Ref3：I/O Buffer Information Specification IBIS Version 6.1 page 20， http://ibis.org/ver6.1/ver6_1.pdf

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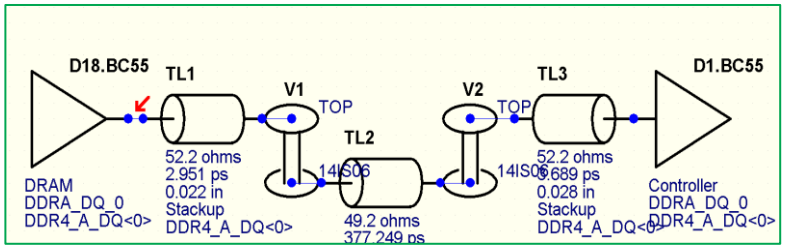
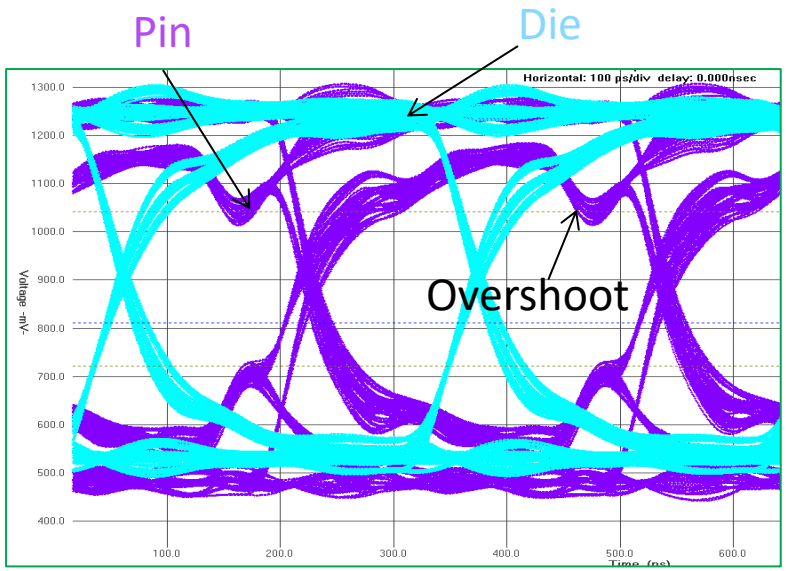
Introduction of Two DDR4 Simulation Cases

Case1: Pin VS Die

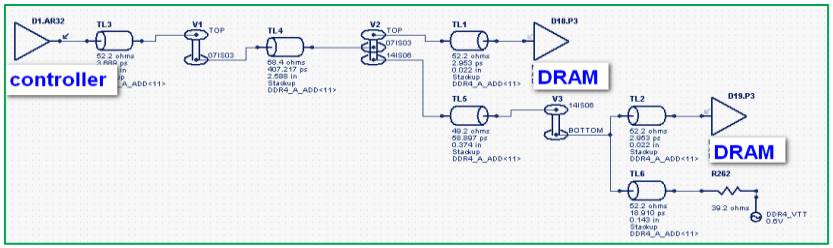
- DQ read
- Simulation @3200Mbps
- Point to Point

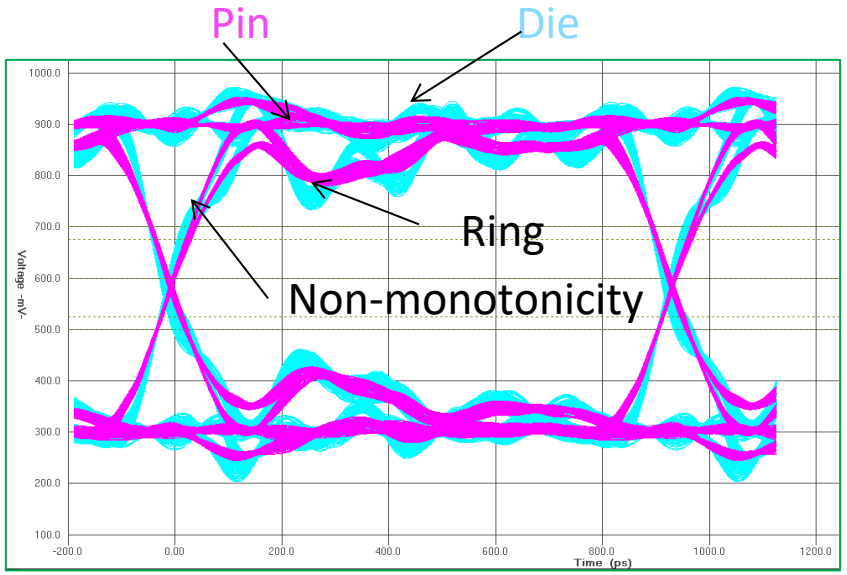




Case2: Pin VS Die

- CMD
- Simulation @2133Mbps 1T mode
- T Topology

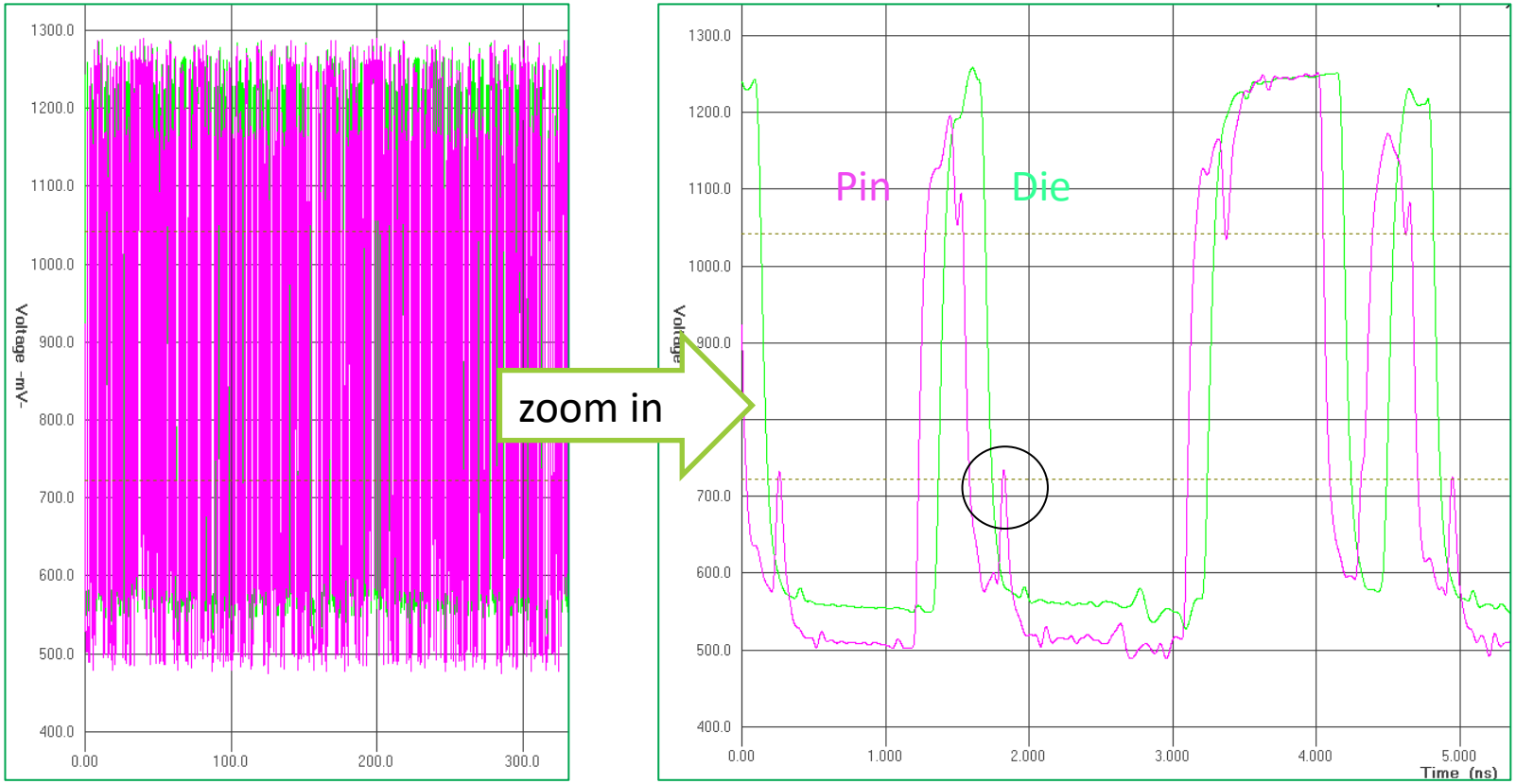




Package can cause rings and non-monotonicity when doing simulation or testing

What is the Root Cause of this Signature for Case1 Pin Vs Die

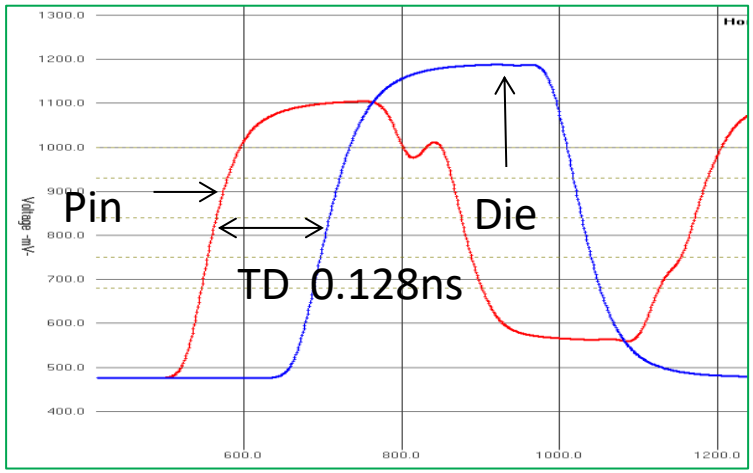
- Simulation @3200Mbps, 1T mode
- PRBS 7



What is the Root Cause of this Signature for Case1 Pin Vs Die

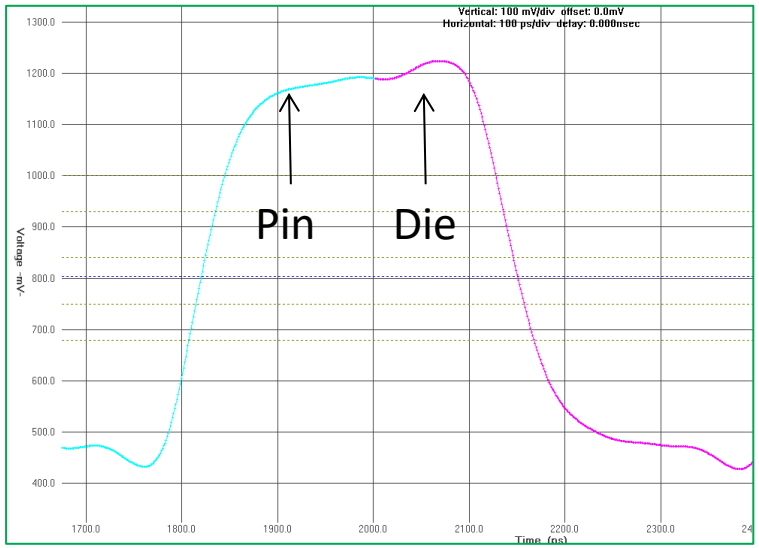
- Pin Information： L_pin and C_pin value contribute the TD of the package

```
[Package]
| variable        typ                 min                 max
R_pkg             200.00m             100.00m             300.00m
L_pkg             2.00nH              1.00nH              3.00nH
C_pkg             1.35pF              1.20pF              1.50pF
|
[pin]   signal_name         model_name R_pin              L_pin           C_pin
BC55    DDRA_DQ_0           d4_dq      3.77E+03mOhm       6.02E+00nH      2.73E+00pF |
AM56    DDRA_A0_A7A8        d4_addr    3.30E+03mOhm       5.33E+00nH      2.81E+00pF
AN51    DDRA_A10            d4_addr    2.56E+03mOhm       4.19E+00nH      1.62E+00pF
```

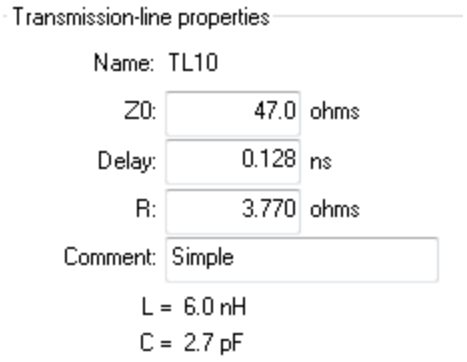


- Verification： Set R_pkg/L_pkg/C_pkg to Zero, the waveform is same between Pin and Die

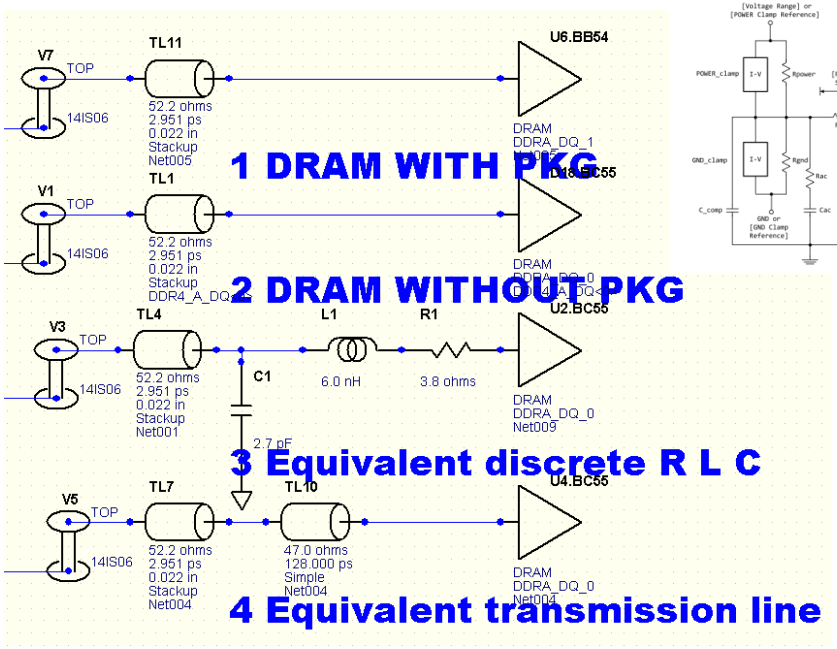
```
| variable        typ                 min                 max
R_pkg             0.001m              NA                  NA
L_pkg             0.001nH             NA                  NA
C_pkg             0.001pF             NA                  NA
|
[pin]   signal_name         model_name R_pin              L_pin           C_pin
BC55    DDRA_DQ_0           d4_dq      NA     NA     NA
AM56    DDRA_A0_A7A8        d4_addr    3.30E+03mOhm       5.33E+00nH      2.81E+00pF
```

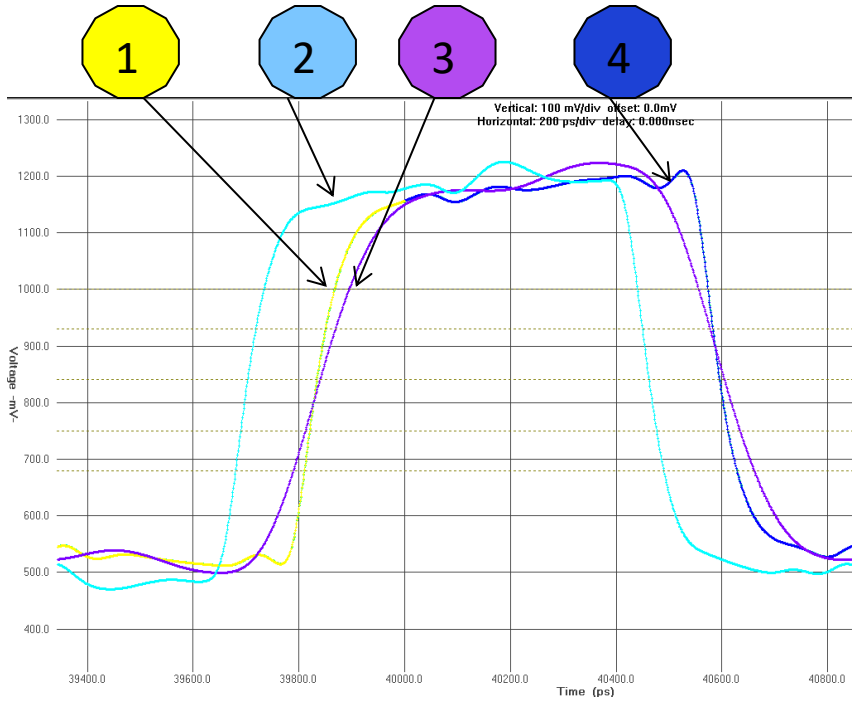


What is the Root Cause of this Signature for Case1 Pin Vs Die



- Simulation @667Mbps
- R_pin = 3.77mohm, L_pin = 6.02nH, C_pin = 2.73pF
- Use transmission line TL10 matching pin parameter well
- Equivalent discrete R L C value R/L/C_pin have Similar envelope as T LINE
- All observation points are at the die





What is the Root Cause of this Signature for Case1 Pin Vs Die

Transmission-line properties

Name: TL10

Z0: 47.0 ohms

Delay: 0.128 ns

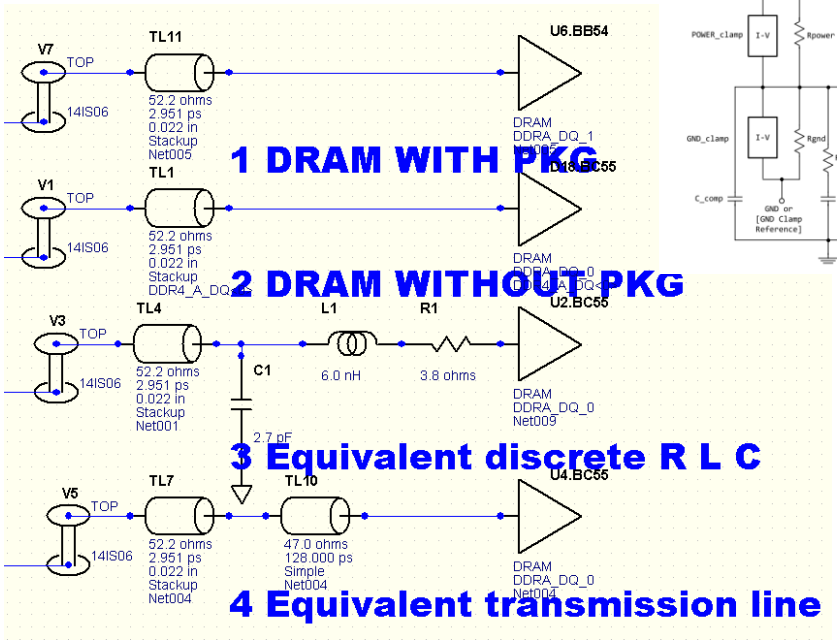
R: 3.770 ohms

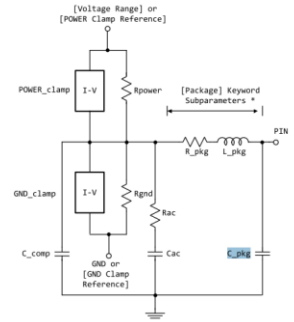
Comment: Simple

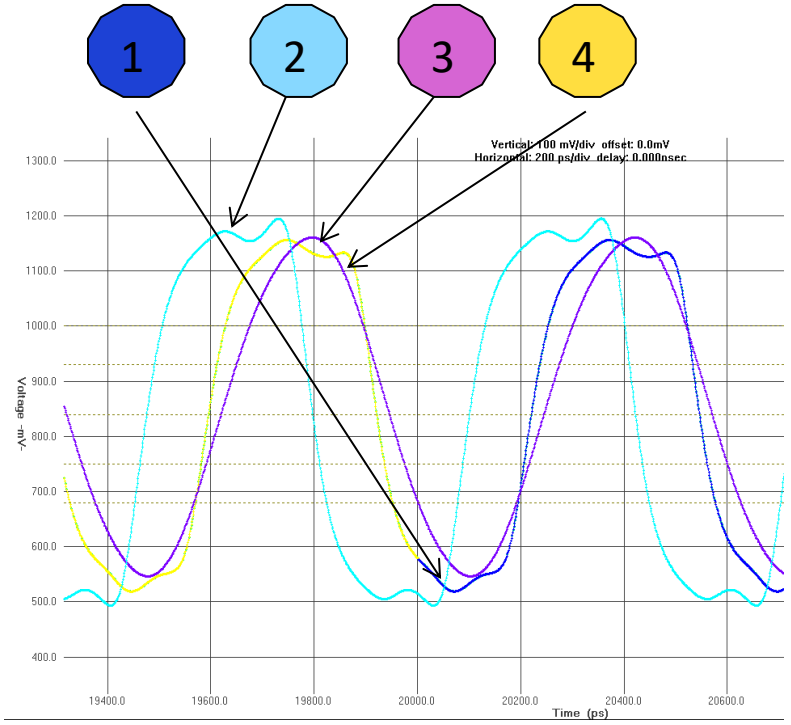
L = 6.0 nH

C = 2.7 pF

- Simulation @3200Mbps
- Transmission line TL10 still works well
- Equivalent discrete R L C value distorts the waveform as the frequency goes up
- If a transmission line that has a time delay of TD, we wish to approximate it with an n-section lumped-circuit model
- All observation points are at the die







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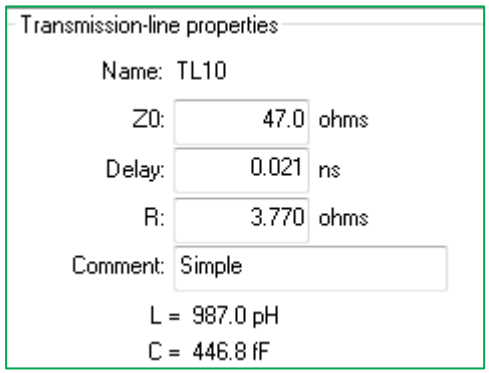
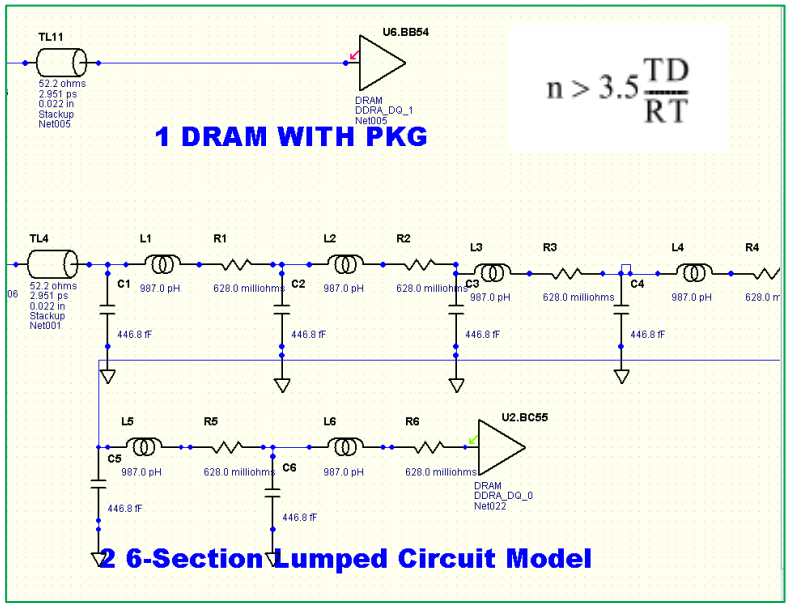
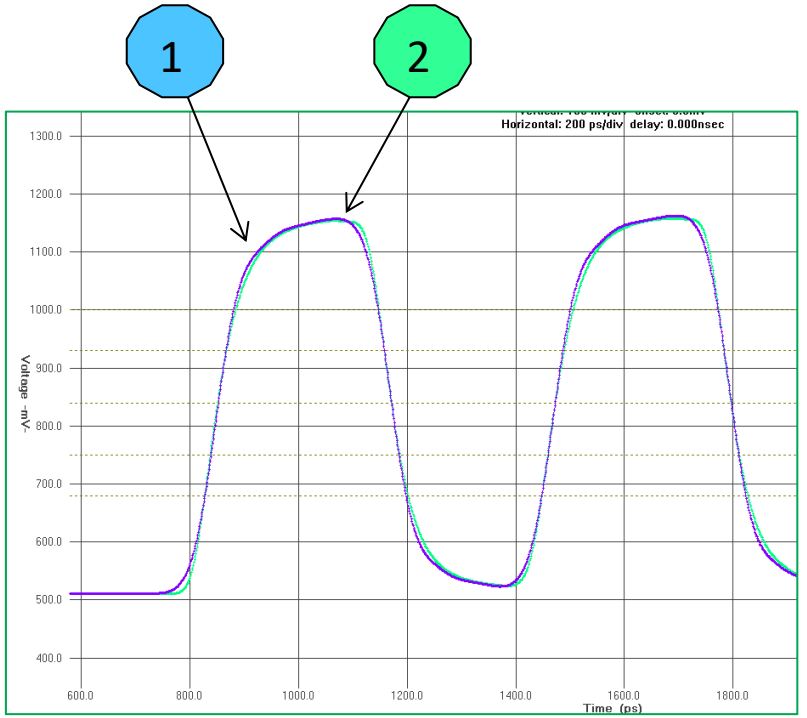
What is the Root Cause of this Signature for Case1 Pin Vs Die



- Simulation @3200Mbps
- If a transmission line that has a time delay of TD and we wish to approximate it with an n-section lumped-circuit model
- Ctotal = TD/Z0 = 0.128ns/47Ohm = 2.7pF
- Ltotal = Z0XTD = 47*0.128 = 6.016nH
- n > 3.5*0.128/0.072 (20%~80% rise time) = 6
- 6-Section Lumped Circuit Model compared with the T line well

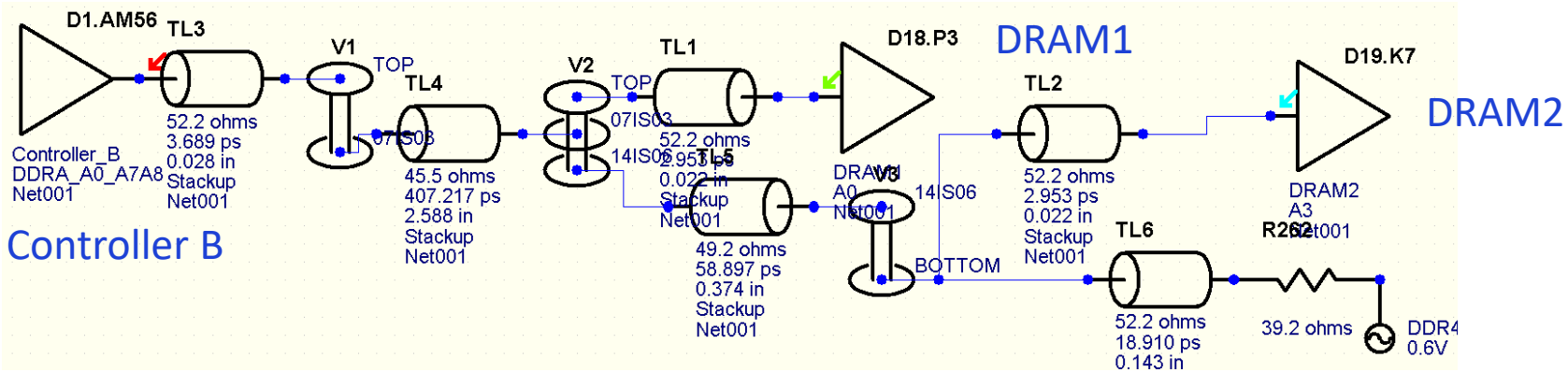


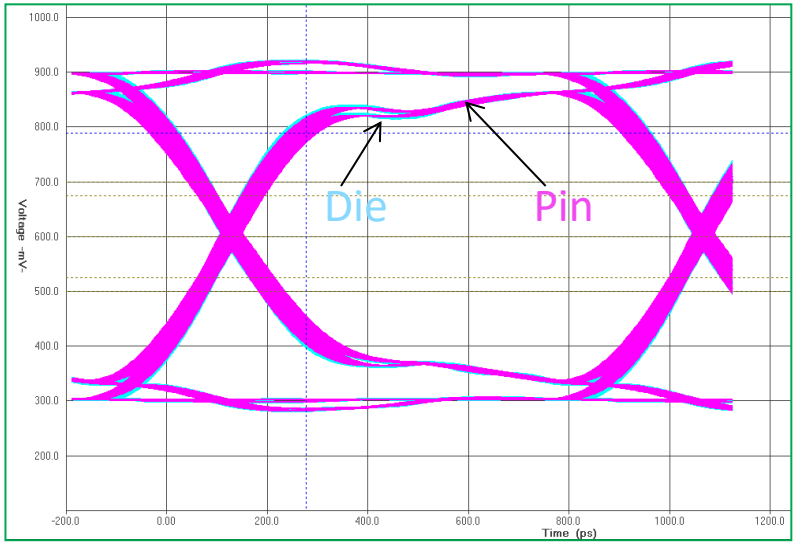


from SIGNAL AND POWER INTEGRITY–SIMPLIFIED SECOND EDITION Eric Bogatin page 305

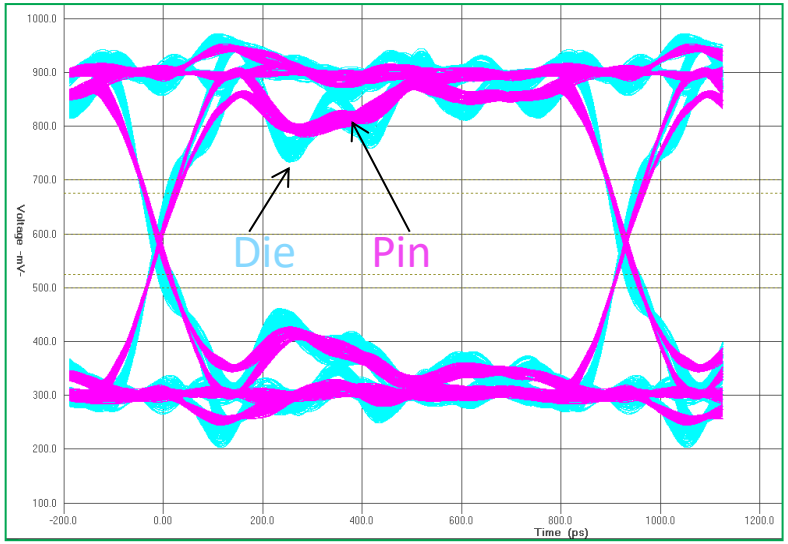
What is the Root Cause of this Signature for Case2 Pin Vs Die

Measurement base the same topology with 2133Mbps DDR4 1T mode





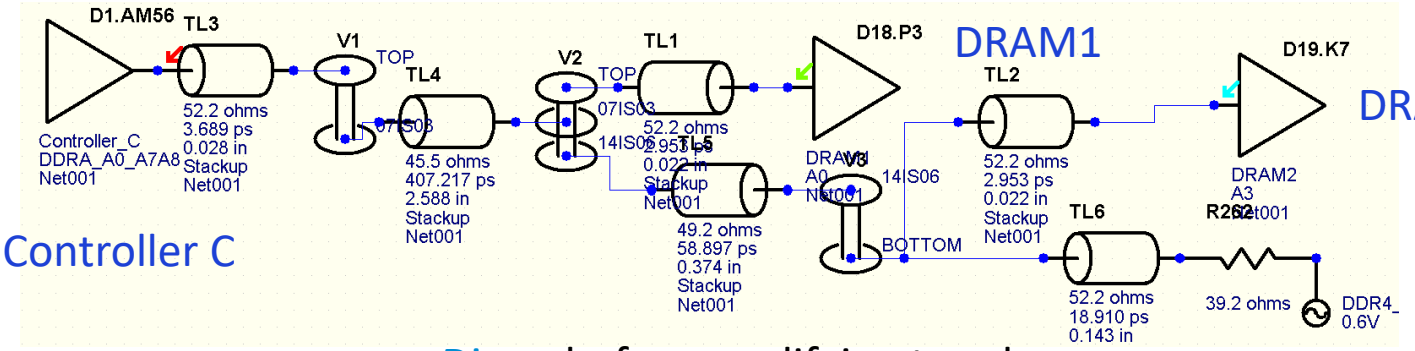
With medium controller model



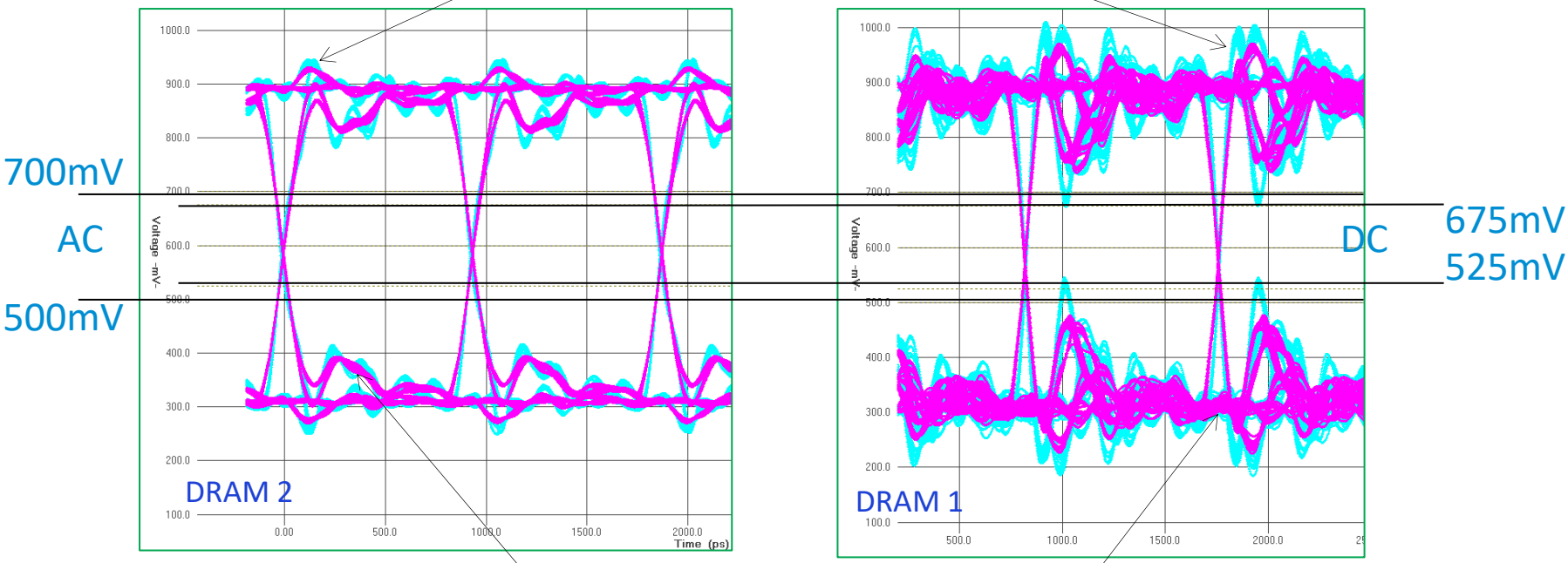
With fast controller model

What is the Root Cause of this Signature for Case2 Pin Vs Die

Measurement on same topology with 2133Mbps DR4 1T mode, Controller C
Unfortunately, just have one type controller mode. Topology needed adjustment.



Die： before modifying topology



Die: after modifying topology

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Design Considerations for the Next Generation of DDR

- System Designers
  - ✓ Impact on DDRX when using “Low loss” and “Ultra-low-loss” materials for high speed I/O design
  - ✓ Short, more reflective channel, wider lines
  - ✓ Different load, DRAM number from 1 to 9, single or twin Die
  - ✓ SI-PI “co-simulation”
  - ✓ Full coverage for both all DDRx nets and different vendor models
- Model Creators
  - ✓ [Pin] name is physical pin name A1, A2, A3, B1; Not 1, 2 ,3
  - ✓ Tx: FIR； Rx: CTLE, FFE, DFE for ISI
  - ✓ Types of effects need to be simulated, Simultaneous Switching Noise with Power Aware
  - ✓ Power Delivery (PDN) Network
  - ✓ Single ended and differential signals
- EDA Tool Vendors
  - ✓ Support SI-PI “co-simulation”
  - ✓ Multi channels simulations
  - ✓ Batch simulation
  - ✓ Automatic measurement and report generation

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Summary

- The non-monotonic waveform of the pin is a common phenomenon in the test sections and simulation
- Use transmission line matching Package parameters well
- The deterioration of pin waveform over “Die” is in accordance with the expected simulation, but there are exceptions
- From system application's perspective, it is recommended that the coming DDR5 models and tools can support all the DDRx nets and SI-PI co-simulation

Thank you!

5G 先锋