Celestica 112G SI Channel Study for 800G Switch

Bowen Shi /Sophia Feng of Celestica
bowens@celestica.com

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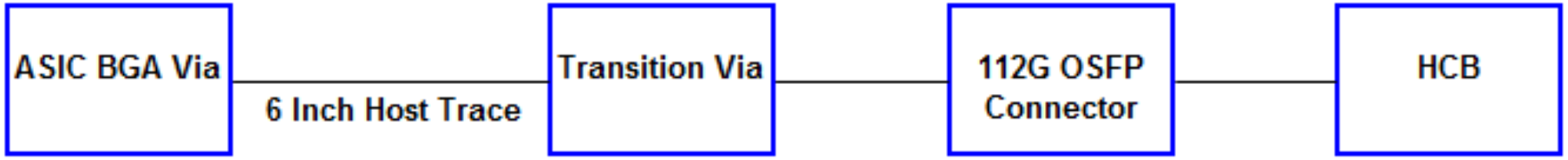
Think Bigger.
Reach Further.

Agenda

- 112G Passive Channel Modeling: C2M and CR loopback.
- COM Simulation for 100G-CR loopback channel.
- Conclusion

Passive Channel Modeling

802.3ck C2M Host Channel Modeling



Host board PCB is 26 Layers, total 4mm thickness, M7N level material.

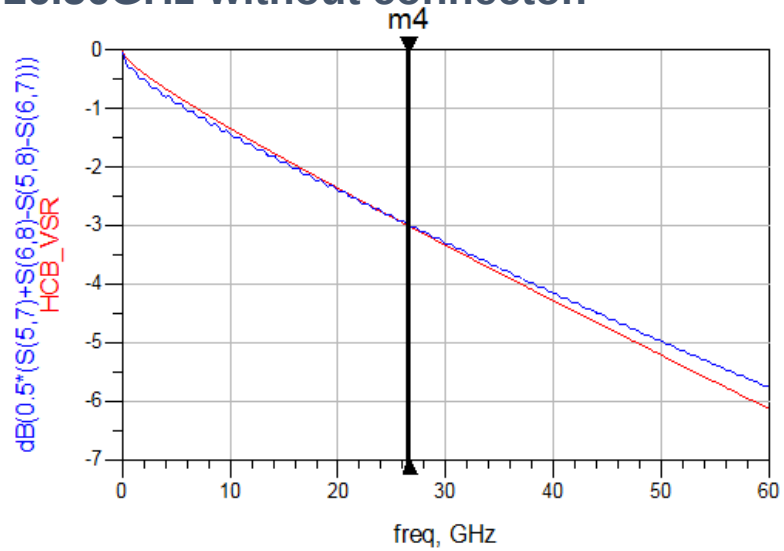
Host trace width/spacing is 8mil/10mil, 6inch of trace includes 0.8inch neck-down (4mil/4mil).

Vias stub modeled as 6mils, long via length, solution frequency up to 80GHz.

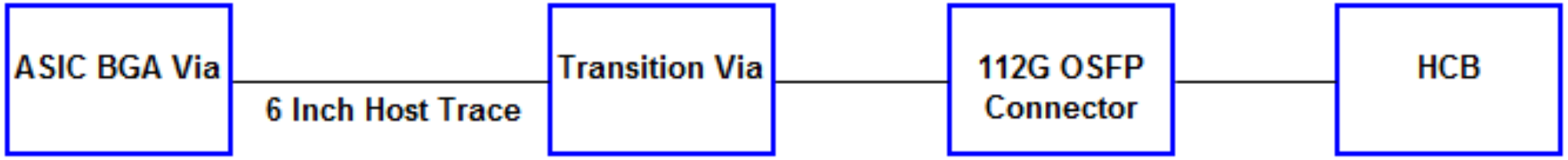
Referred to diminico_3ck_01a_0719, host channel insertion loss budget is 7dB@26.56GHz without connector.

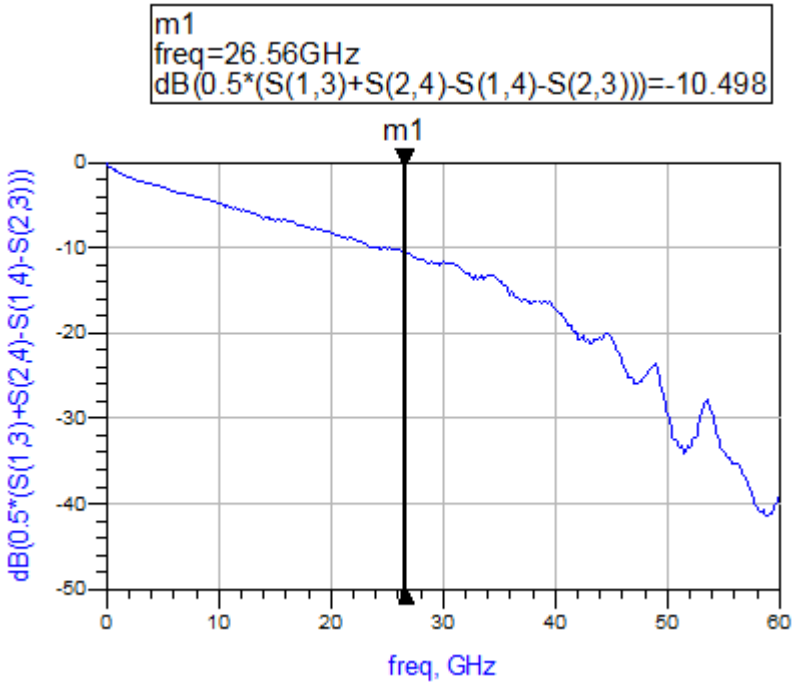
HCB (Host compliance board) modeled using simulation tools, 3dB@26.56GHz.

m4
freq=26.56GHz
HCB_VSR=-3.002
dB(0.5*(S(5,7)+S(6,8)-S(5,8)-S(6,7)))=-3.004

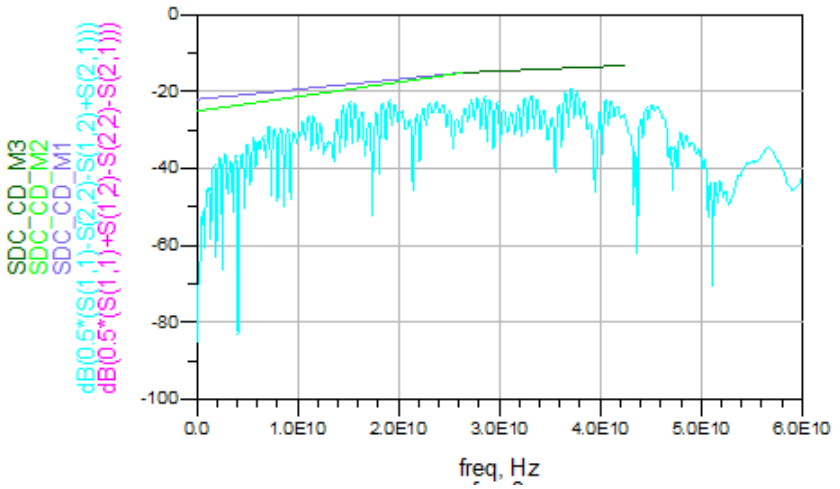


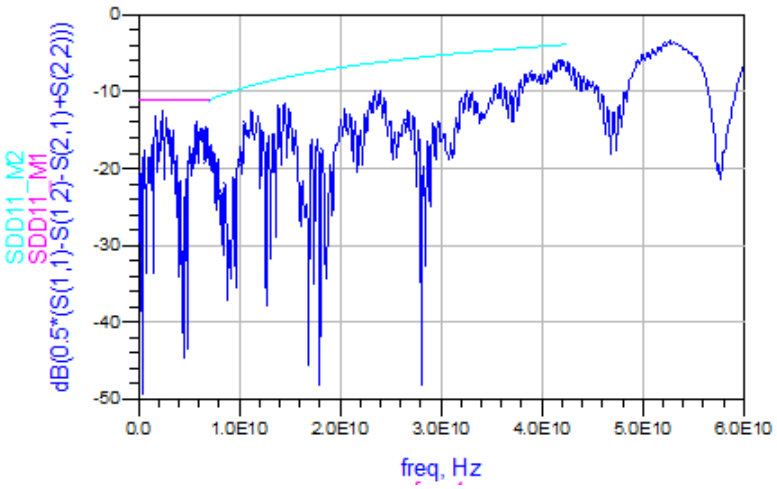
802.3ck 100G_C2M Host Channel Modeling





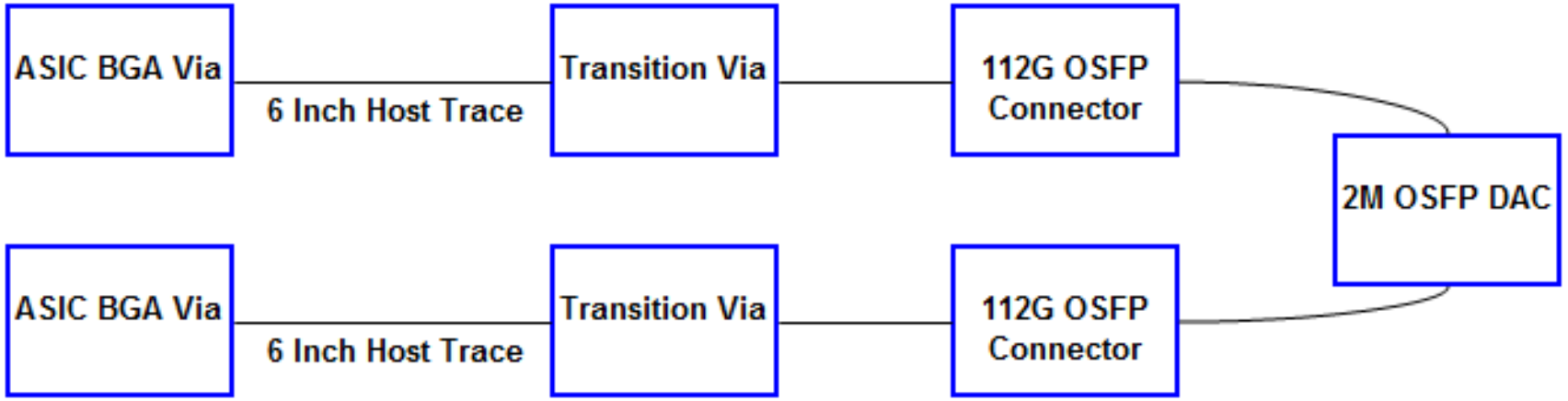
Host channel Insertion Loss





Host channel Return Loss

802.3ck 100G_CR Host Channel Modeling



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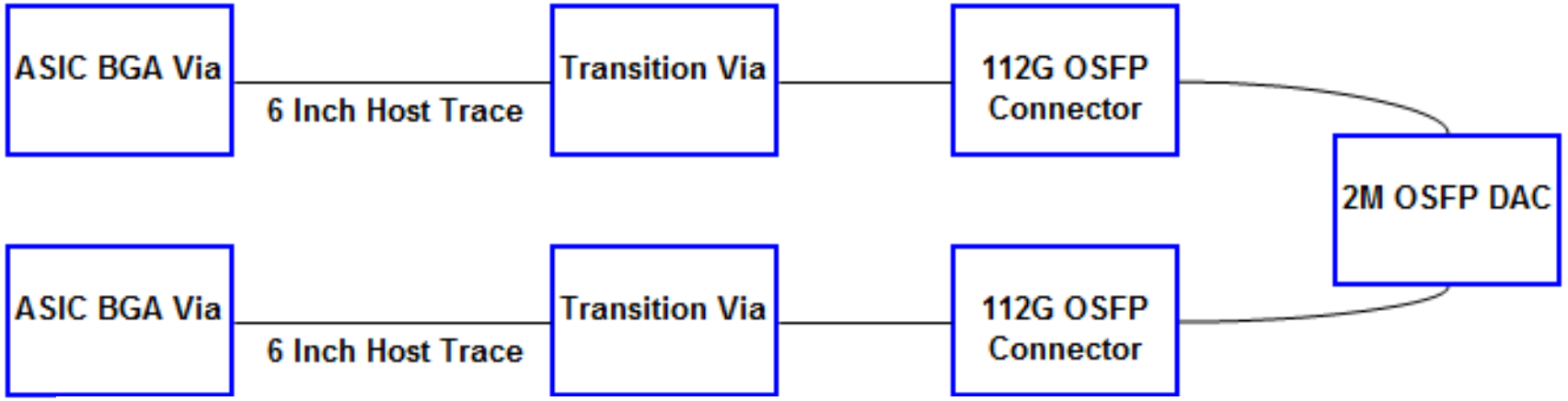
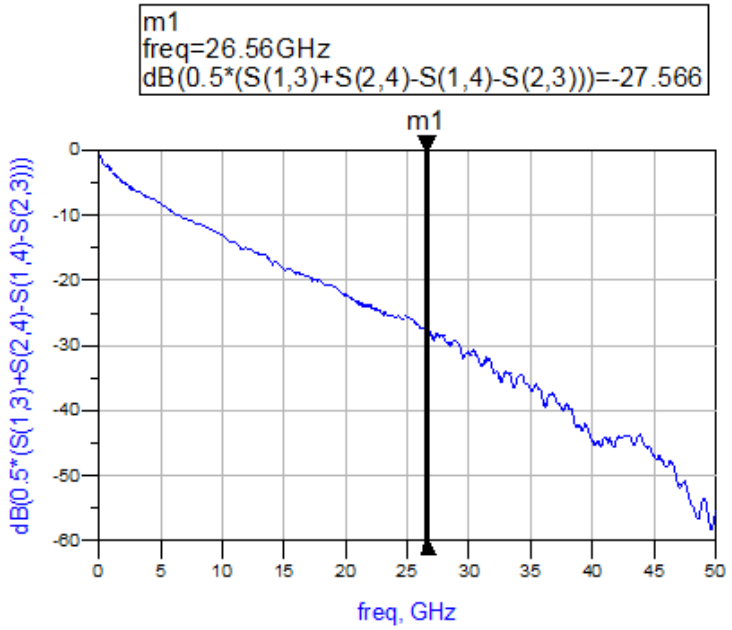
Referred to diminico_3ck_01a_0719, host channel insertion loss budget is 7dB@26.56GHz without connector.

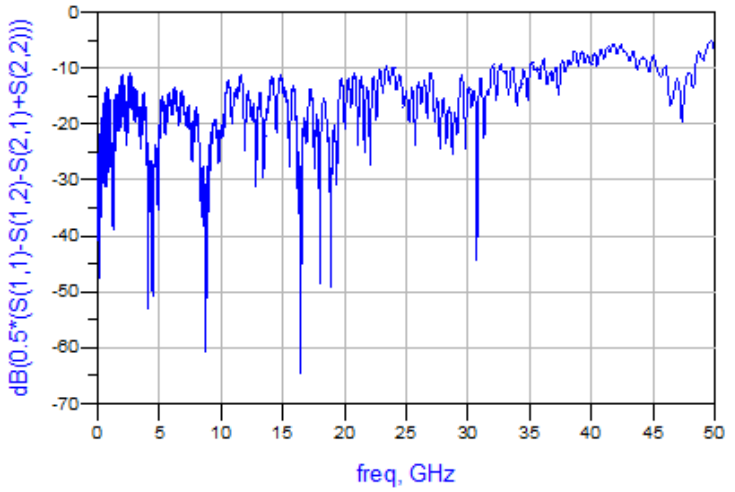
End to end insertion loss target is less than 28.5dB@26.56GHz.

802.3ck 100G_CR Host Channel Modeling





Loopback channel Insertion loss

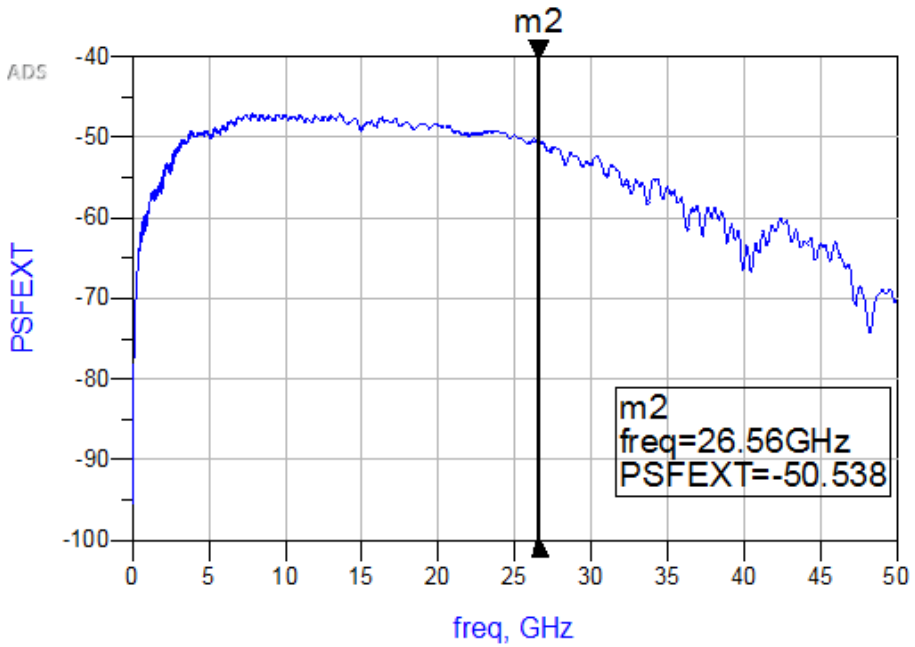


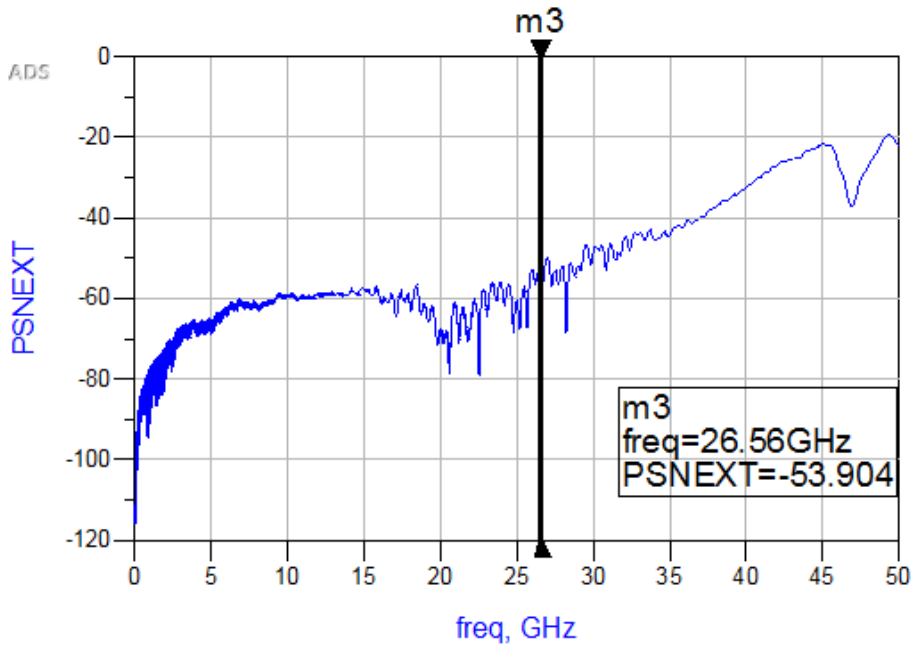
Loopback channel return loss

100G-CR COM Simulation

802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback

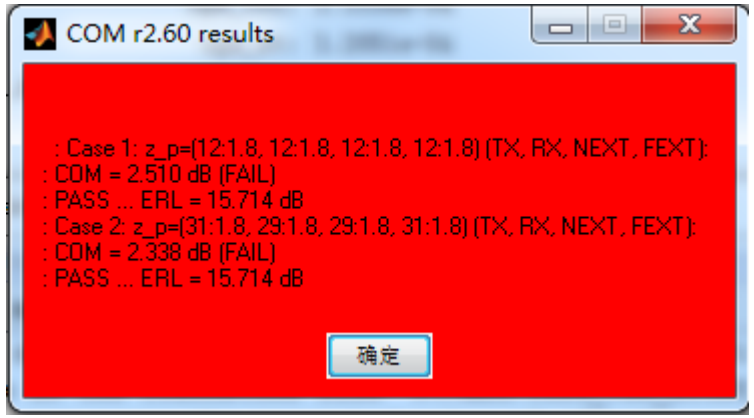
- The Channel Operating Margin (COM) has been defined in IEEE802.3ck, and the channel margin shall be greater than or equal to 3dB after COM calculation for 100G-CR/KR Channel. Note that the COM code is the draft version from IEEE802.3ck Task Force (**Code version: mellitz_3ck_02_0319_COM2p60, 3ck_KR_mellitz_06_12_2019_2**).
- 5 aggressor FEXT channel and 3 aggressor NEXT channel on both sides of victim channel are considered for the COM crosstalk analysis.
- The victim is the 27.56dB 2M OSFP loopback channel in the previous section.
- Crosstalk power sum results as follows:





802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback

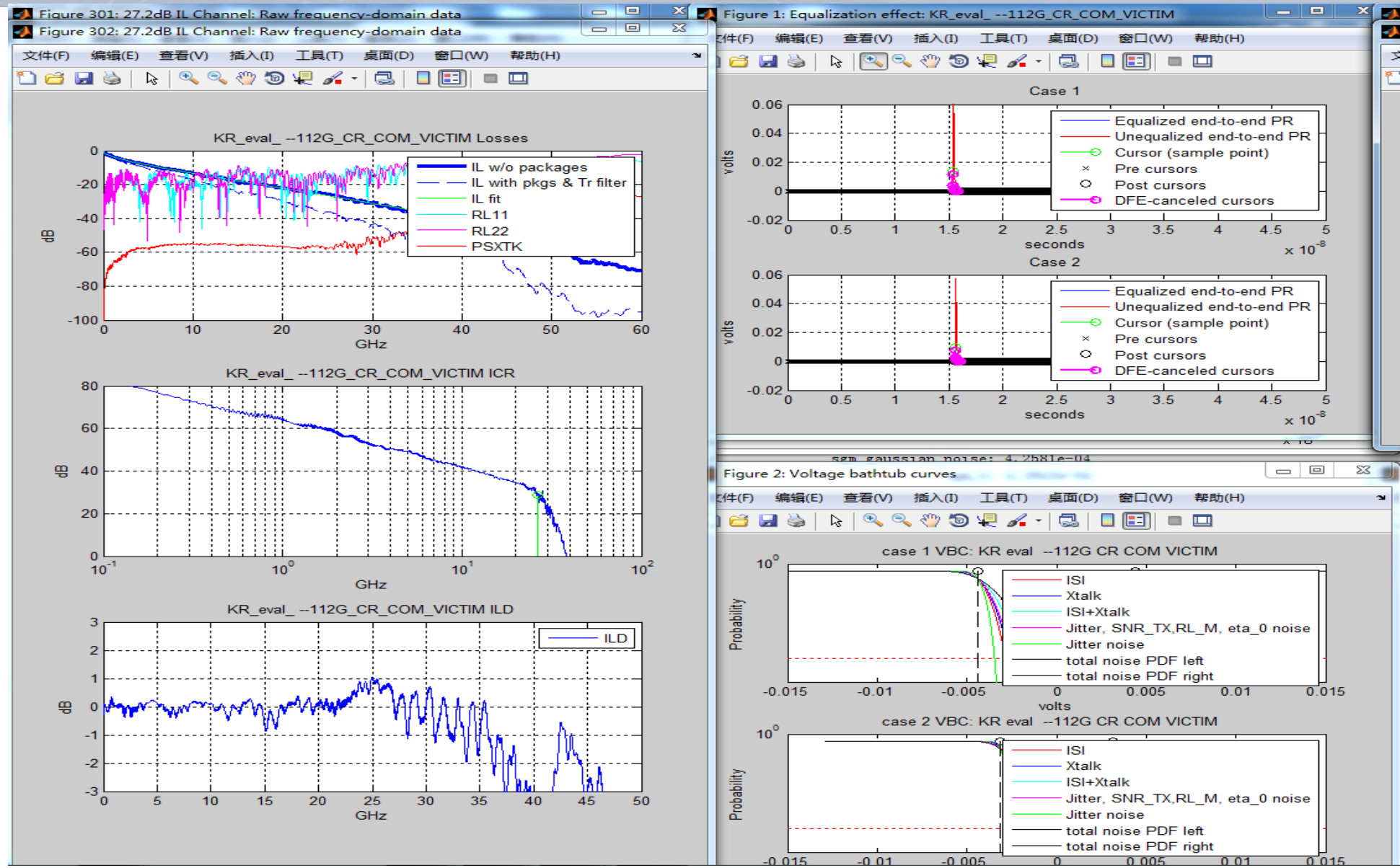
```
--- Testcase 2 results ---
                code_revision: '2.60'
                      Z11est: 95.0632
                      Z22est: 95.0721
                       ERL11: 15.7669
                       ERL22: 15.7137
                         ERL: 15.7137
                      RxFFE: ''
                   RxFFEgain: ''
                 config_file: 'F:\112G Data\IBIS Submit\112_COM\mellitz
                  file_names: '"KR_eval_ --112G_CR_COM_VICTIM,KR_eval_
                      levels: 4
                  Pkg_len_IX: [31 1.8000 0 0]
                Pkg_len_NEXT: [29 1.8000 0 0]
                Pkg_len_FEXT: [31 1.8000 0 0]
                  Pkg_len_RX: [29 1.8000 0 0]
                   R_diepad: [45 45]
                     pkg_Z_c: [2x4 double]
                         C_v: [0 0]
              baud_rate_GHz: 53.1250
              f_Nyquist_GHz: 26.5625
                        BER: 1.0000e-04
                        FOM: 13.7052
                    sigma_N: 3.5284e-04
                   DFE4_RSS: 0.1715
                   DFE2_RSS: 0.3860
 channel_operating_margin_dB: 2.3381
available_signal_after_eq_mV: 3.1441
          peak_uneq_pulse_mV: 57.2731
          uneq_FIR_peak_time: 1.5612e-08
      steady_state_voltage_mV: 29.1113
                   FOM_ILD: 0.3399
```




```
Peak_ISI_XIK_and_Noise_interference_at_BER_mV: 2.4021
peak_ISI_XIK_interference_at_BER_mV: 1.6790
peak_ISI_interference_at_BER_mV: 1.2011
equivalent_ICI_sigma_assuming_PDF_is_Gaussian_mV: 0.3229
peak_MDXIK_interference_at_BER_mV: 1.1099
peak_MDNEXT_interference_at_BER_mV: 0.8709
peak_MDFEXT_interference_at_BER_mV: 0.5628
ICN_mV: 2.5886
MDNEXT_ICN_92_46_mV: 2.2679
MDFEXT_ICN_92_47_mV: 1.2479
equivalent_ICN_assuming_Gaussian_PDF_mV: 0.2984
SNR_ISI_XIK_normalized_1_sigma: 16.8577
SNR_ISI_est: 32.0779
Pmax_by_Vf_est: 0.4236
CILE_zero_poles: [2.1250e+10 5.3125e+10 2.1250e+10]
CILE_DC_gain_dB: -11
g_DC_HP: -3
HP_poles_zero: 664062500
IXLE_taps: [-0.0200 0.0800 -0.2800 0.6200 0]
DFE_taps: [24x1 double]
sgm_Ani__isi_xt_noise: 6.5327e-04
sgm_isi_xt: 4.6244e-04
sgm_isi: 3.3335e-04
sgm_xt: 3.2051e-04
sgm_noise__gaussian_noise_p_DD: 4.6142e-04
sgm_p_DD: 1.7776e-04
sgm_gaussian_noise: 4.2581e-04
sgm_G: 4.2643e-04
sgm_rjit: 8.9107e-05
sgm_N: 3.5284e-04
sgm_IX: 2.2228e-04
total_IL_wpkgs_dB_at_Fnq: 39.1631
IL_dB_channel_only_at_Fnq: 27.1907
```

802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback

- 24 taps fixed DFE used in the COM simulation. Since the COM configuration is not finalized, it's currently difficult to pass the COM 3dB margin.



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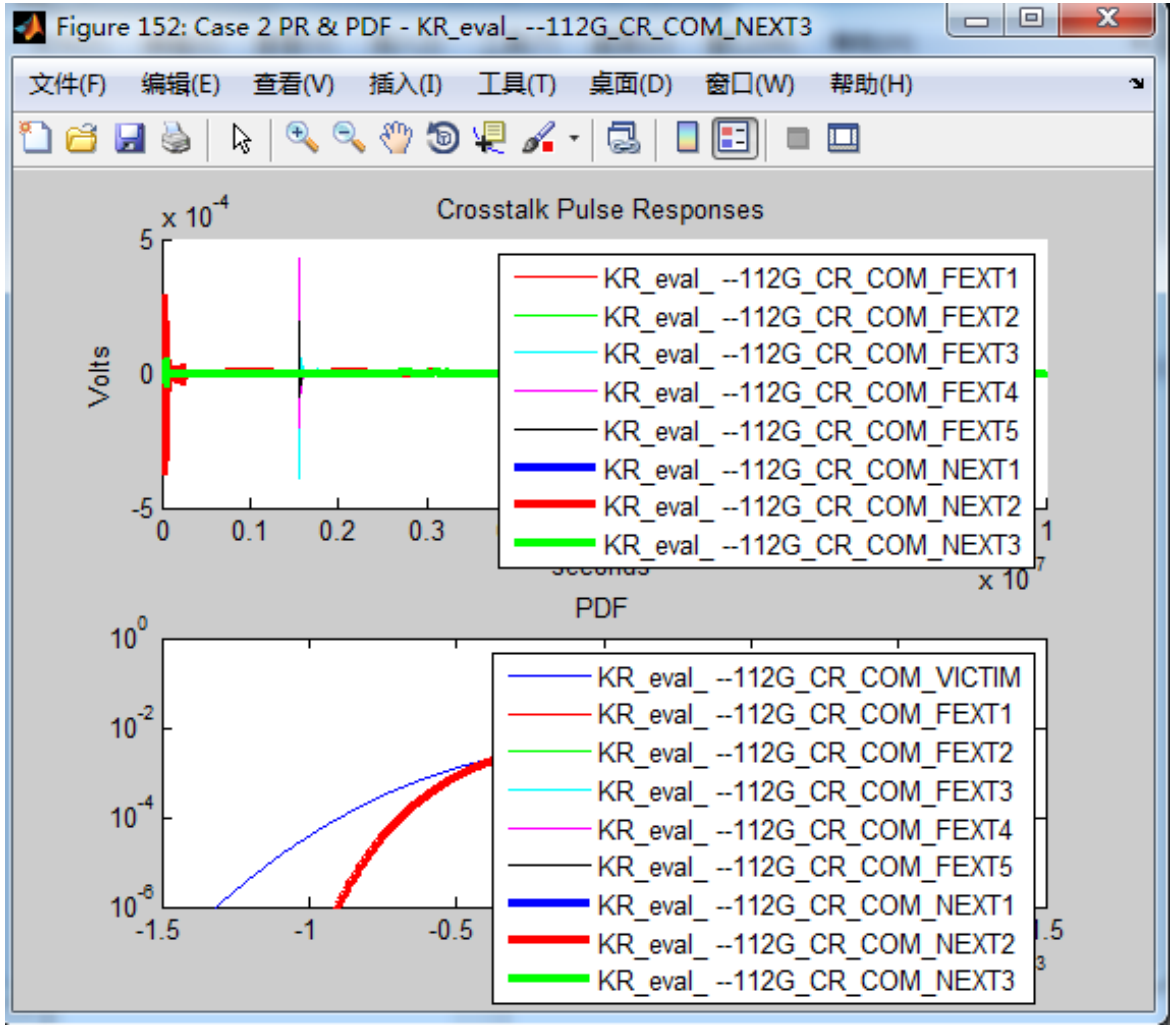

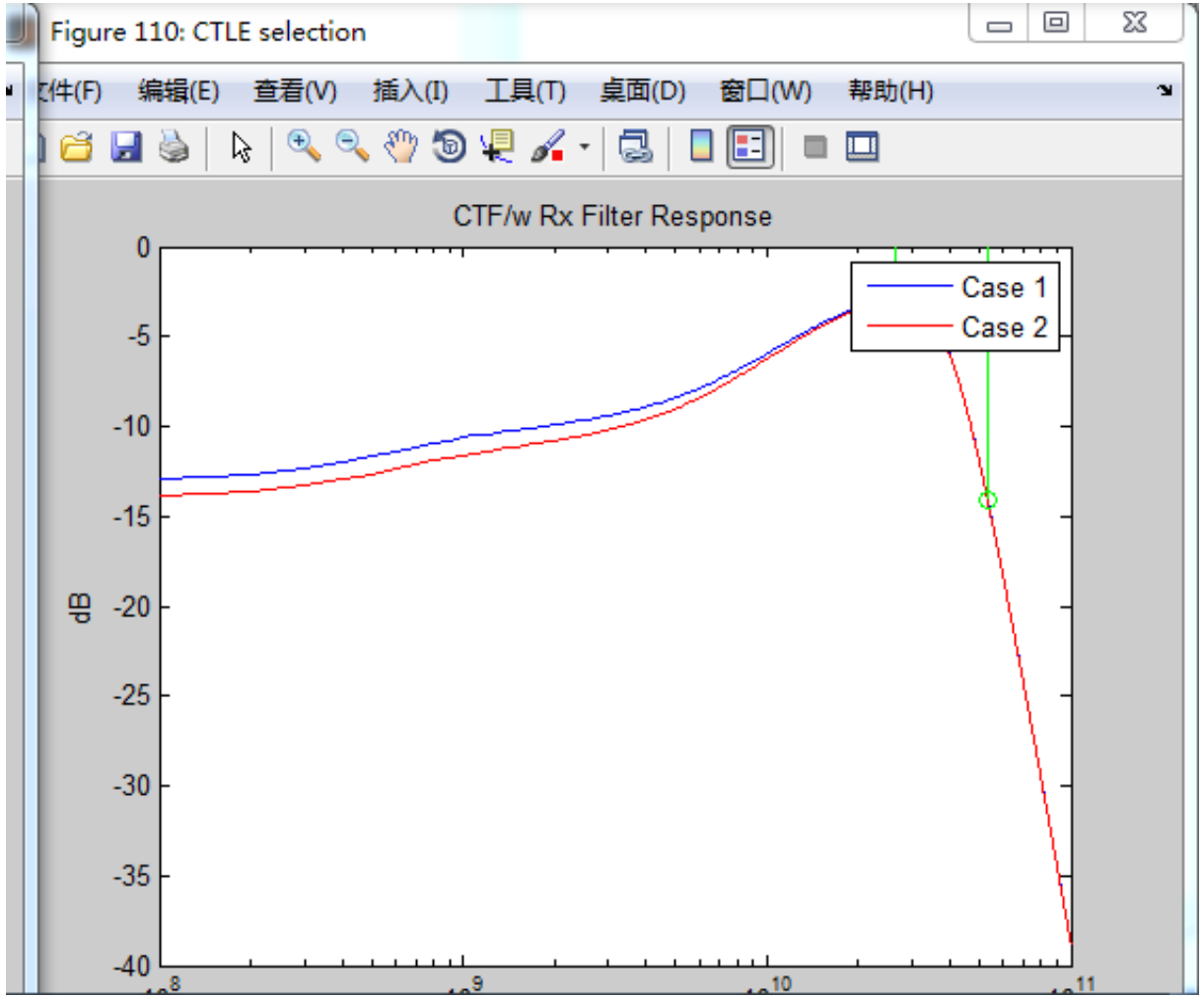

802.3ck_COM Simulation Results_100G-CR 2M OSFP Loopback

- Config_files:

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.5		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	24	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.3		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	**0.25**	
fixture delay time	0	s
TDR_W_TXPKG	0	
N_bx	24	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A? parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92?2 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**0**	**0 1 2 or 3 groups**
N_bf	*0*	taps per group
N_f	40	UI span for floating taps
bmaxg	0.1	max DFE value for floating taps

yellow indicates WIP

Conclusion

- **In the early stage of 112G product development, Celestica is preparing the channel modeling for IBIS-AMI simulation. Most 112G IBIS-AMI model will be available in 2020-Q1.**
- **PCB still can be an option for 112G switch, but the SI performance of the PCB need to be improved (M8 Level).**
- **In our simulation, the host channel trace length is only 6inch, it's difficult to improve the insertion loss performance to get better COM margin, so it has a higher expectation on Xtalk to improve the SNR (BER).**
- **Will continue update the 112G simulation.**

Thank You