

To obtain high accuracy results of IBIS-AMI channel simulation

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Agenda



- Introduction
- **SAMPLES PER BIT**
 - What is SAMPLES PER BIT
 - SAMPLES PER BIT setting in simulation including jitter
- Summary

Introduction



- Channel simulation using IBIS-AMI has become widespread for high-speed serial signals.
- Data rate is also increasing to 5Gbps, 10Gbps, 25Gbps, and above.
- Conversely, Unit Interval becomes shorter to 200ps, 100ps, 40ps, and less.
- Jitter(Dj, Rj of Tx, Rx) is even smaller, from one-thousandth to one-hundredth of Unit Interval.
- For that reason, in simulation that include jitter, special attention must be paid to simulation accuracy.
- SAMPLES PER BIT setting in EDA tool determines simulation accuracy.
- Therefore, this time, investigated the SAMPLES PER BIT setting to obtain accurate simulation result.

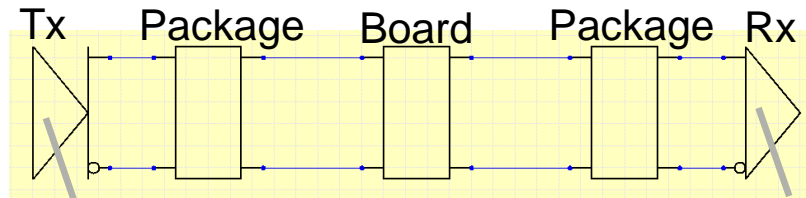
What is SAMPLES PER BIT

SAMPLES PER BIT determines simulation accuracy. Explain it below.

Simulation conditions

- **SAMPLES PER BIT**
Example: 8
- Data rate
Example: 25Gbps
- PRBSn
Example: PRBS31
- Other setting

Topology for Channel simulation



Tx IBIS-AMI
Analog back-end
and
Algorithmic Model

Rx IBIS-AMI
Analog front-end
and
Algorithmic Model

EDA tool

Sampling interval[sec]=(1/Data rate)/SAMPLES PER BIT

Example: (1/25e9)/8=5ps

What is SAMPLES PER BIT

Sampling interval[sec]

How used within EDA tool

In time domain simulation.

- Generate digital input waveform from bit streams
- Output interval of Impulse response
- Output interval of (*)Convolution by input stimulus and impulse response
(*)equal to the analog input waveform to Rx

How used within Algorithmic model(.dll)

In time domain simulation.

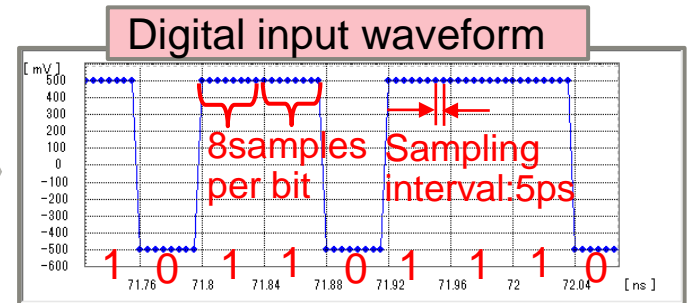
Passed from the EDA tool to the argument “sample_interval” of the function” AMI_Init” of the Algorithmic model.

- Output interval of equalized digital input waveform
- Output interval of equalized Rx output waveform

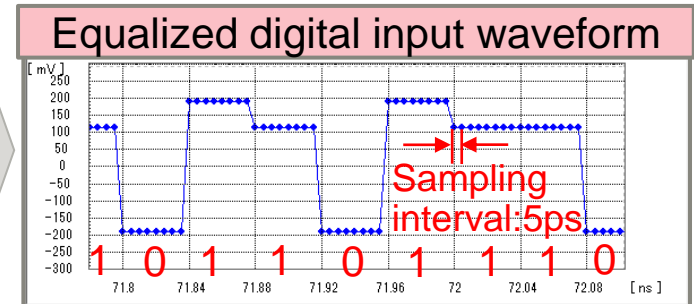
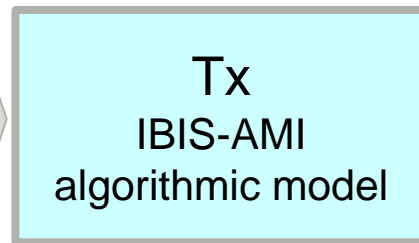
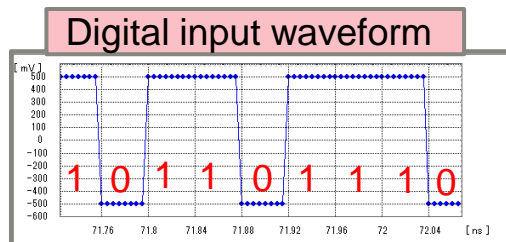
What is SAMPLES PER BIT

- Generate digital input waveform from bit streams

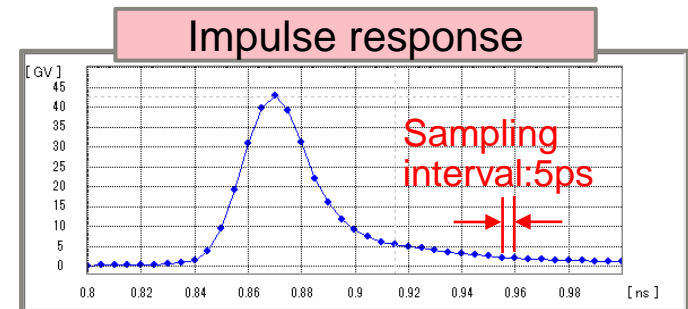
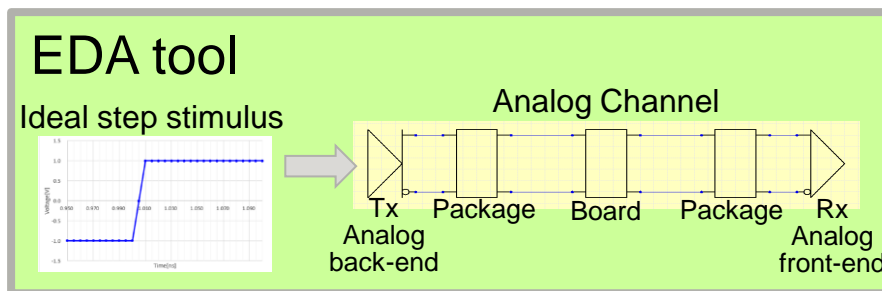
Stimulus : PRBS31
bit streams "...101101110..."
Data rate: 25Gbps(1UI=40)
SAMPLES PER BIT: **8**
Sampling interval: **5ps**



- Output interval of equalized digital input waveform

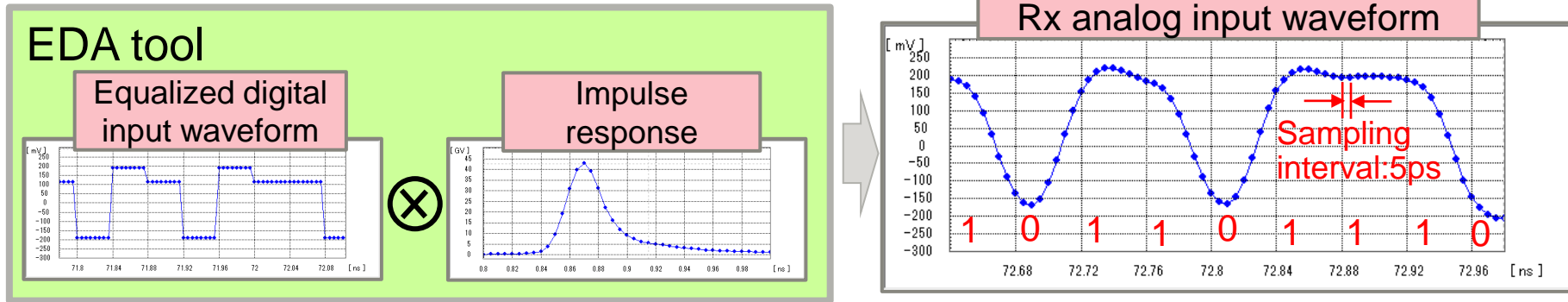


- Output interval of Impulse response

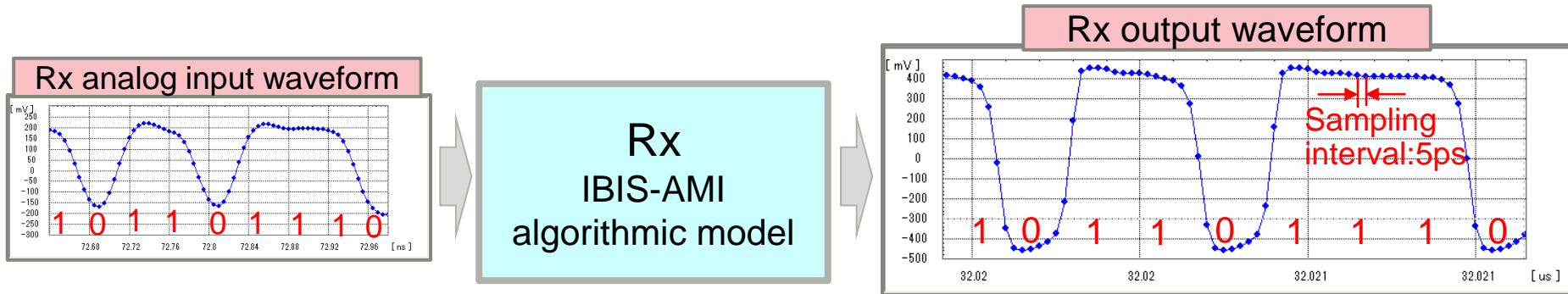


What is SAMPLES PER BIT

- Output interval of Convolution by input stimulus and impulse response (= Rx analog input waveform)



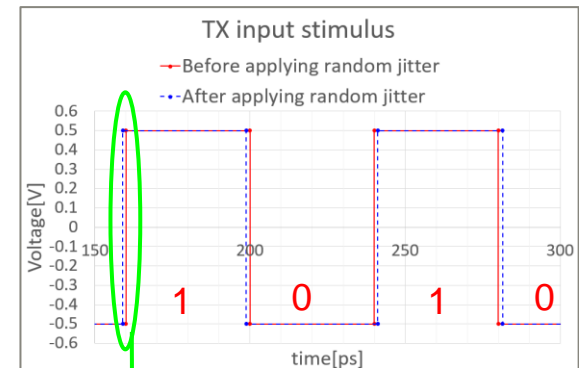
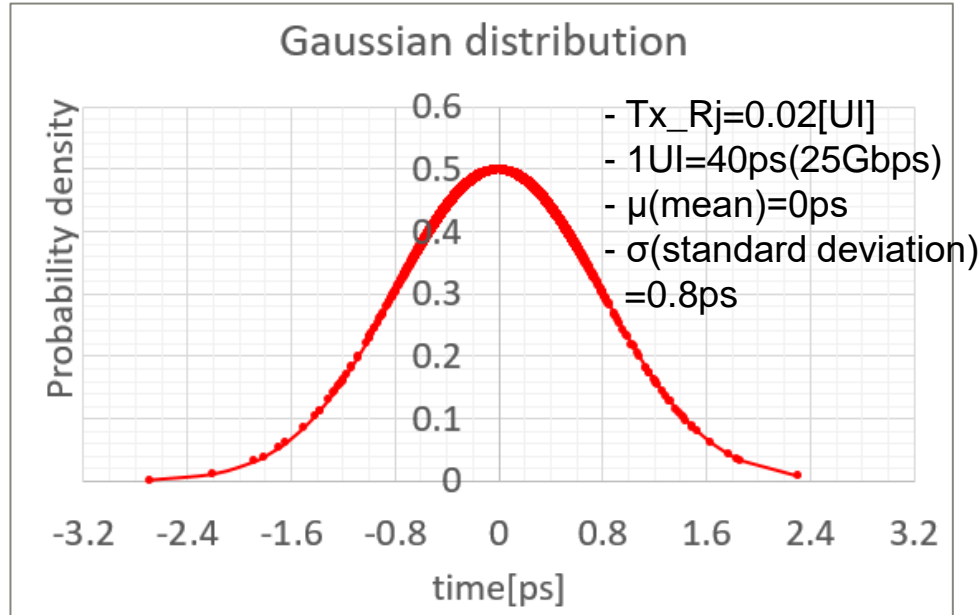
- Output interval of equalized Rx output waveform



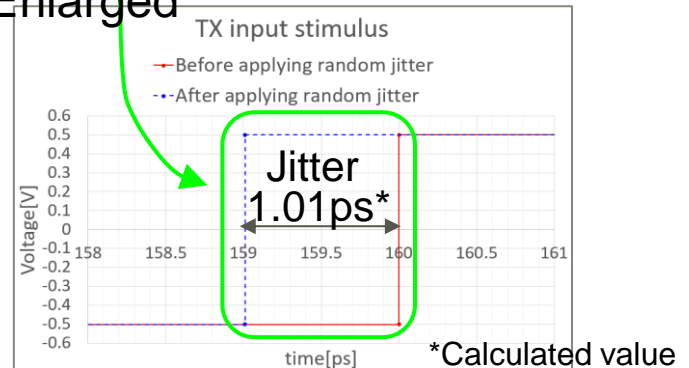
SAMPLES PER BIT setting in simulation including jitter

- Jitter value is very small compared to Unit Interval.
Example: Tx Random jitter=0.8ps (At 25Gbps, Rj(rms)=0.02UI, 1UI=40ps)
- Simulation method including Random jitter:
EDA tool adds jitter to Tx input waveform according to formula below.
 $Time(n) = n * bit_time + Tx_Rj * gaussian_rand() \rightarrow \text{from IBIS spec.}$
From above equation, random jitter has Gaussian distribution.

Distribution of Jitter by “Tx_Rj * gaussian_rand()”



Enlarged

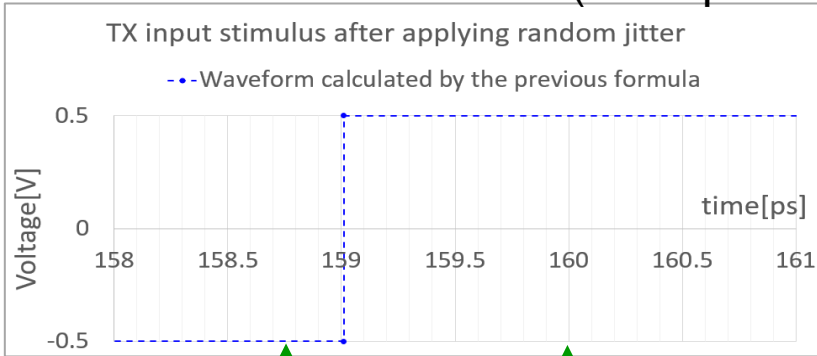


SAMPLES PER BIT setting in simulation including jitter

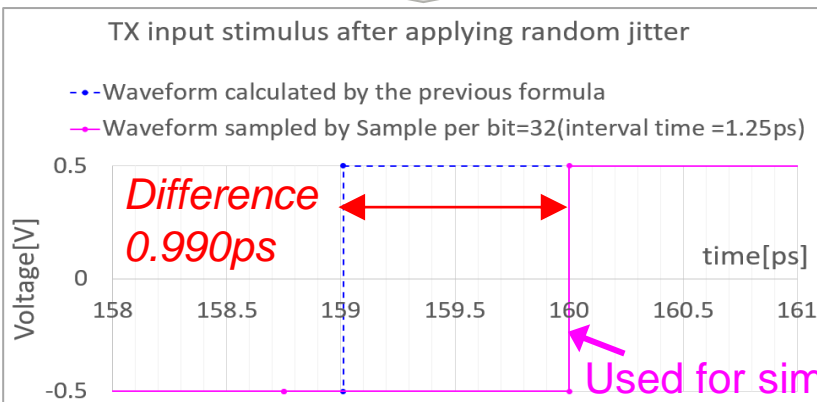


Jitter is not applied correctly to Tx input stimulus when SAMPLES PER BIT is small.

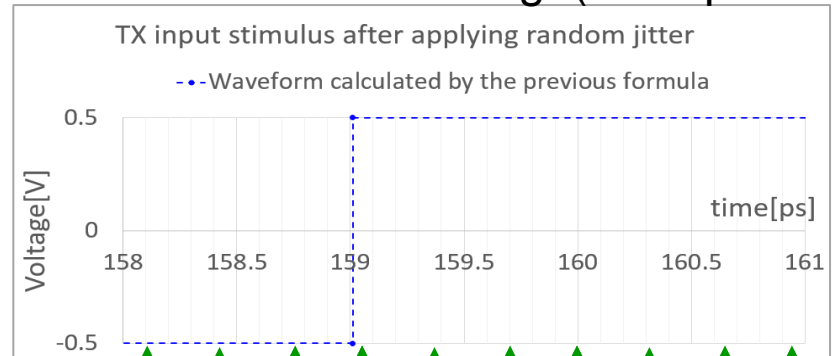
SAMPLES PER BIT: small(example 32)



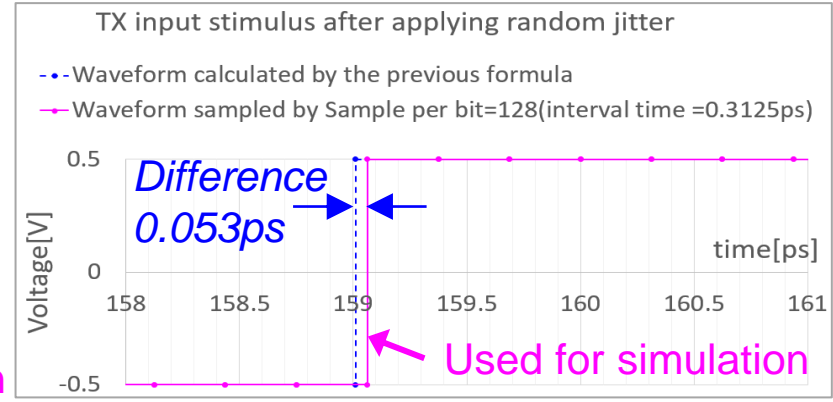
Sampling interval: $1.25\text{ps} (= 1/25\text{Gbps}/32)$



SAMPLES PER BIT: large(example 128)



Sampling interval: $0.3125\text{ps} (= 1/25\text{Gbps}/128)$



SAMPLES PER BIT setting in simulation including jitter

For example, when 25Gbps/Random jitter(rms)=0.005UI, verify appropriate SAMPLES PER BIT below.

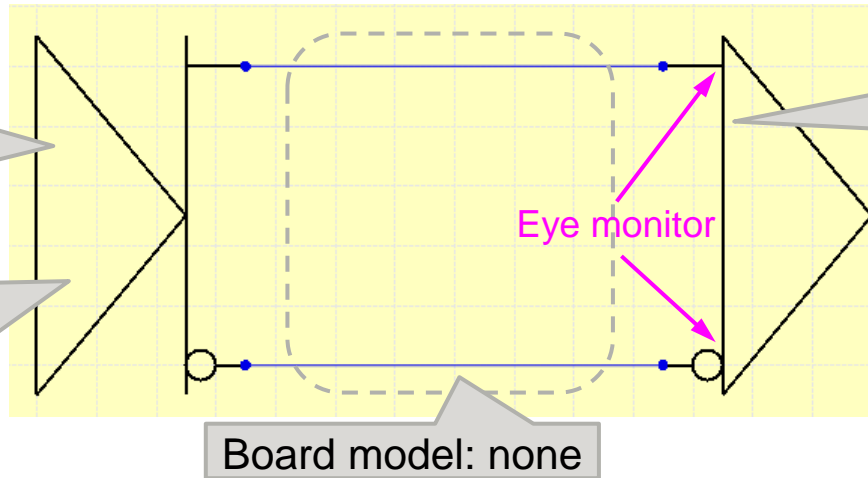
Method of verification

- Use topology below. Perform channel simulation with some SAMPLES PER BIT changes.
- Evaluate quality of SAMPLES PER BIT setting by Jitter Histogram of eye diagram.
- If SAMPLES PER BIT setting is appropriate, **Random jitter Histogram will be Gaussian distribution.**

■ Simple topology to include only Random jitter (avoid deterministic jitter due to reflection and loss)

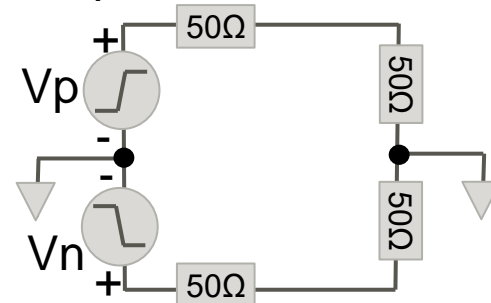
Analog model:
-Rout: 50ohm
-C_comp: none
-Package: none
-Equalizer: none

Tx input stimulus:
-25Gbps(40ps/UI)
-PRBS31
-100,000bit
-Rj(rms):0.005UI(0.2ps)



Analog model:
-Rterm: 50ohm
-C_comp: none
-Package: none
-Equalizer: none

Equivalent circuit

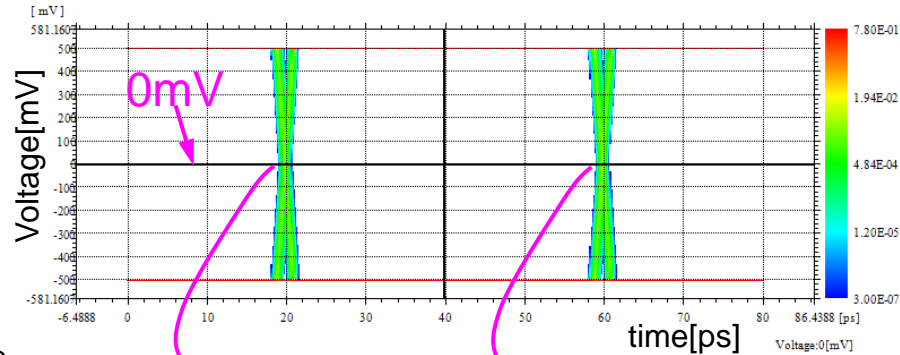


SAMPLES PER BIT to evaluate: 2048, 1028, 512, 256, 128, 64, 32

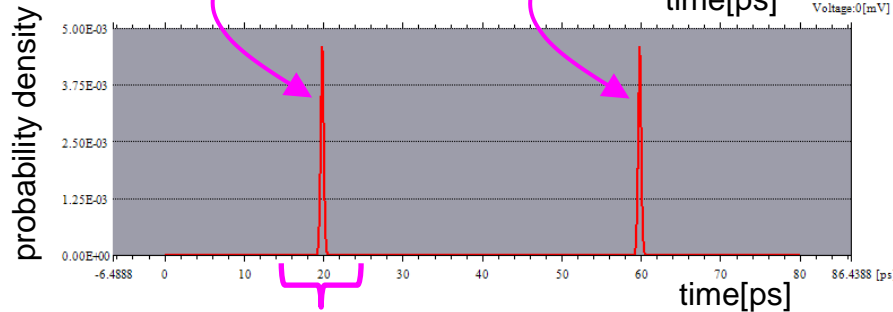
SAMPLES PER BIT setting in simulation including jitter

■ Evaluation of SAMPLES PER BIT settings by histogram

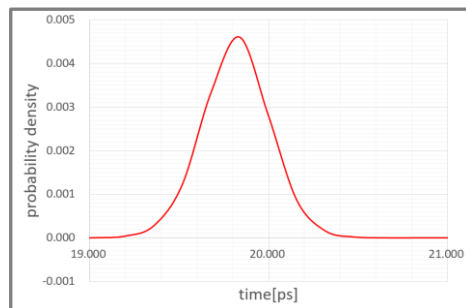
Eye diagram



Jitter histogram



enlarged

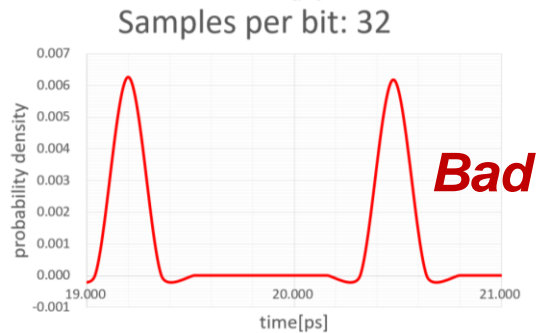
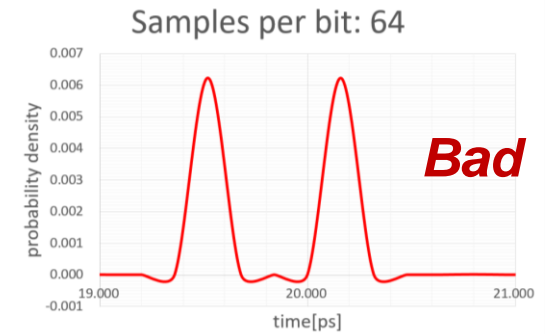
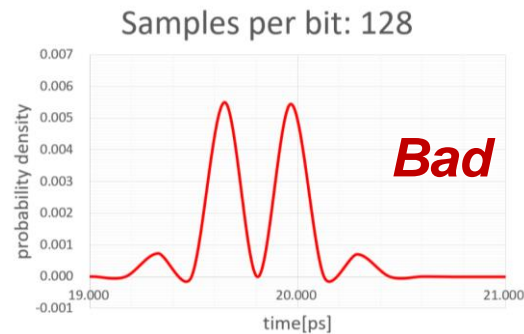
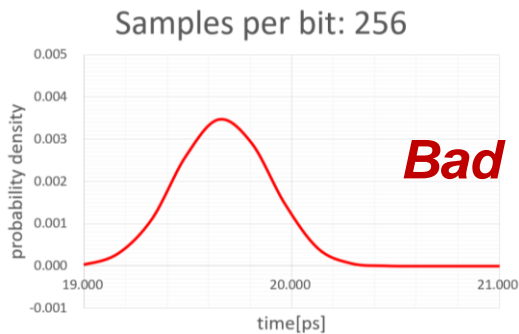
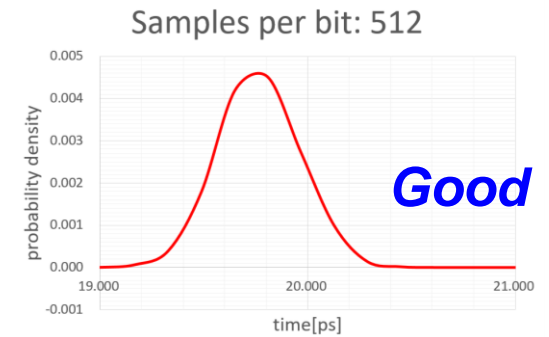
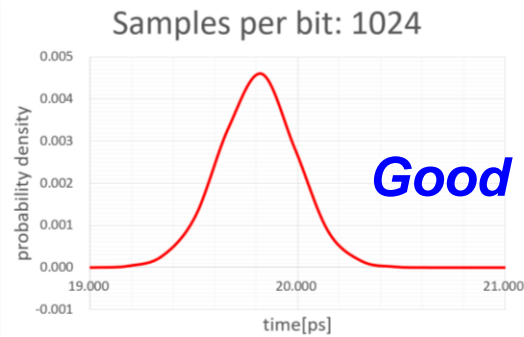
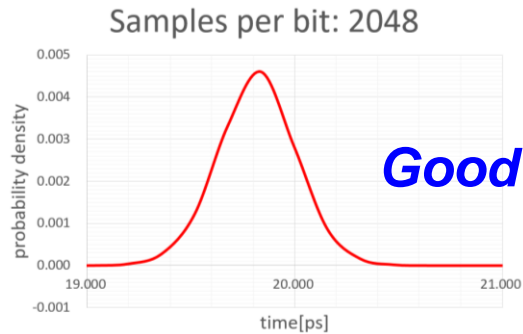


evaluation

If the histogram is Gaussian distribution, SAMPLES PER BIT is appropriate.

SAMPLES PER BIT setting in simulation including jitter

Verification Results **Histogram on left side of eye diagram**



SAMPLES PER BIT setting in simulation including jitter



Results Summary

Samples per bit	Sampling Interval(ps) [25Gbps, 40ps/UI]	Random Jitter(ps) [Rj(rms)=0.005UI]	Number of Samplings per Rj_rms	Simulation Accuracy Gaussian distribution?
2048	0.020	0.2	10.00	Good
1024	0.039	0.2	5.12	Good
512	0.078	0.2	2.56	Good
256	0.156	0.2	1.28	Bad
128	0.313	0.2	0.63	Bad
64	0.625	0.2	0.32	Bad
32	1.250	0.2	0.16	Bad

Summary

- SAMPLES PER BIT is important setting that determines simulation accuracy.
- Correct Tx input digital waveform will not be generated without proper SAMPLES PER BIT.
Therefore, subsequent simulation will also be inaccurate.
- In the channel simulation with $Rj_rms=0.005UI(0.2ps)$ at 25Gbps(40ps/UI), SAMPLES PER BIT for obtaining accurate results is 512 or more.
- That is, it is necessary to set SAMPLES PER BIT so that number of sample points is 2.5 or more per jitter time.

Acknowledgement



Special thanks for advice on how EDA tool work in IBIS-AMI channel simulation.


FUJITSU LIMITED

- Hirokazu Hidaka
- Kumiko Teramae
- Akira Ueda

References



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JEITA EDA Model Specialty Committee 2016
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