Virtual Asian IBIS Summit (China), November 20, 2020

Automated Analysis and Optimization for Multi-Board SerDes Channels with IBIS-AMI Model

Wei He and Jianfeng Xia
Xpeedic Co., Ltd.

XPEEDIC
ACCELERATE YOUR IC DESIGN

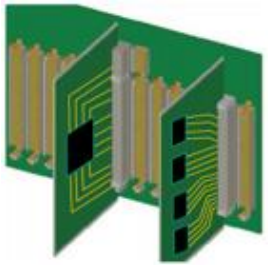
Outline

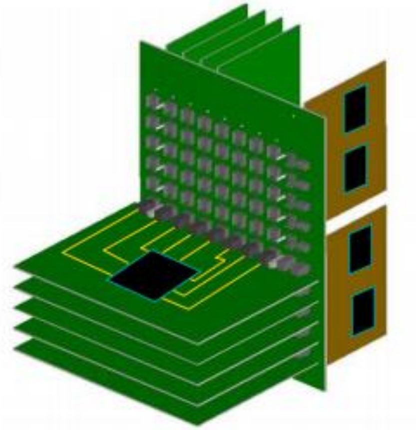
- Challenges on multi-board SerDes channel designs
- I: Accurate EM models for discontinuities along the channel
- II: Channel assembly for multi-board backplane system
- III: SerDes channel analysis with IBIS-AMI model
- IV: IBIS-AMI equalization optimization
- Summary

Challenge on multi-board channel modeling

- There are a variety of different configurations for backplane system.

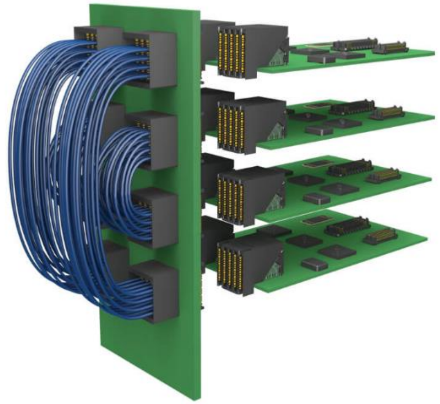
Traditional





Orthogonal

Orthogonal Direct

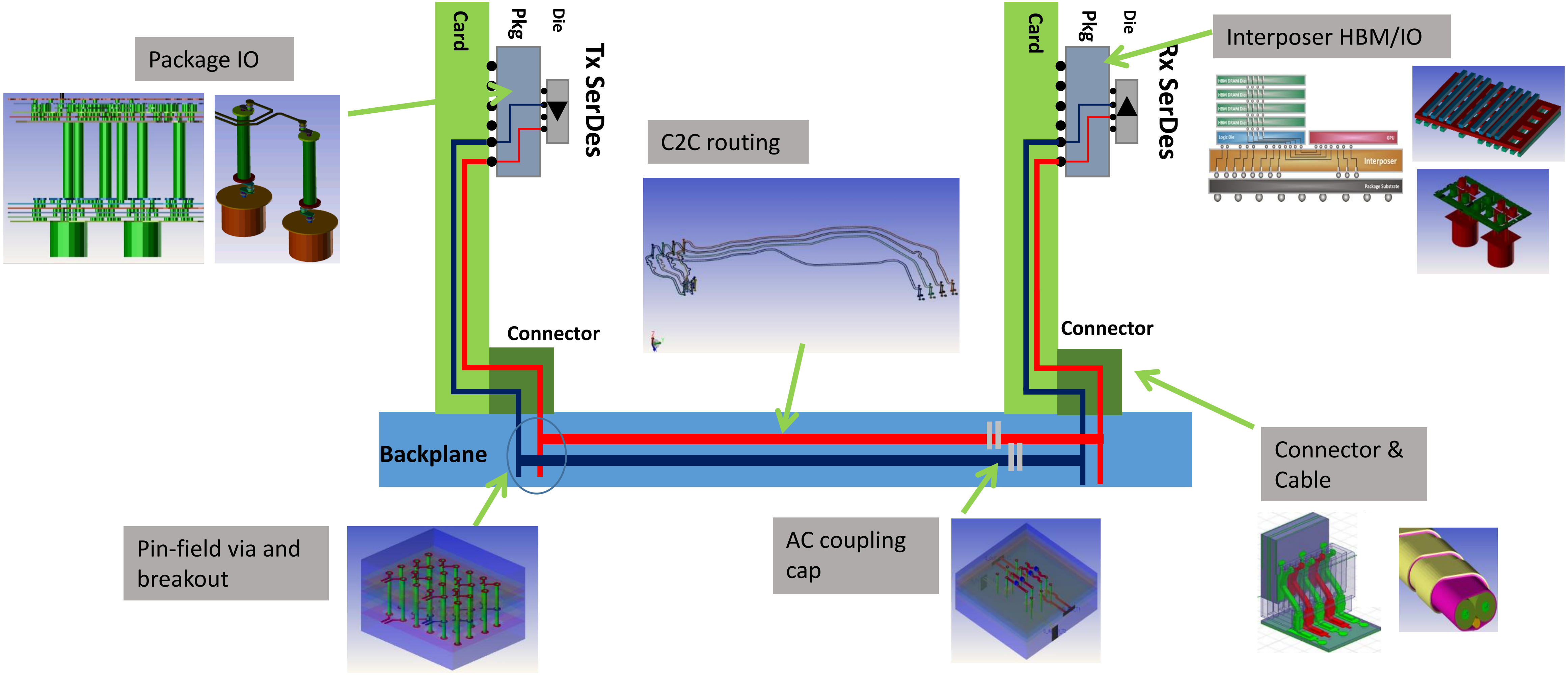


Cable

- SerDes channel simulation faces the following challenges
  - Automated flow to create channels with multi-board configurations
  - Accurate 3D models needed for the channel is overwhelming
  - Optimizing the channel performance with that many variables is prohibitively expensive

I: Accurate EM models for SerDes channels

- Discontinuities along the channel are ubiquitous which require accurate EM models

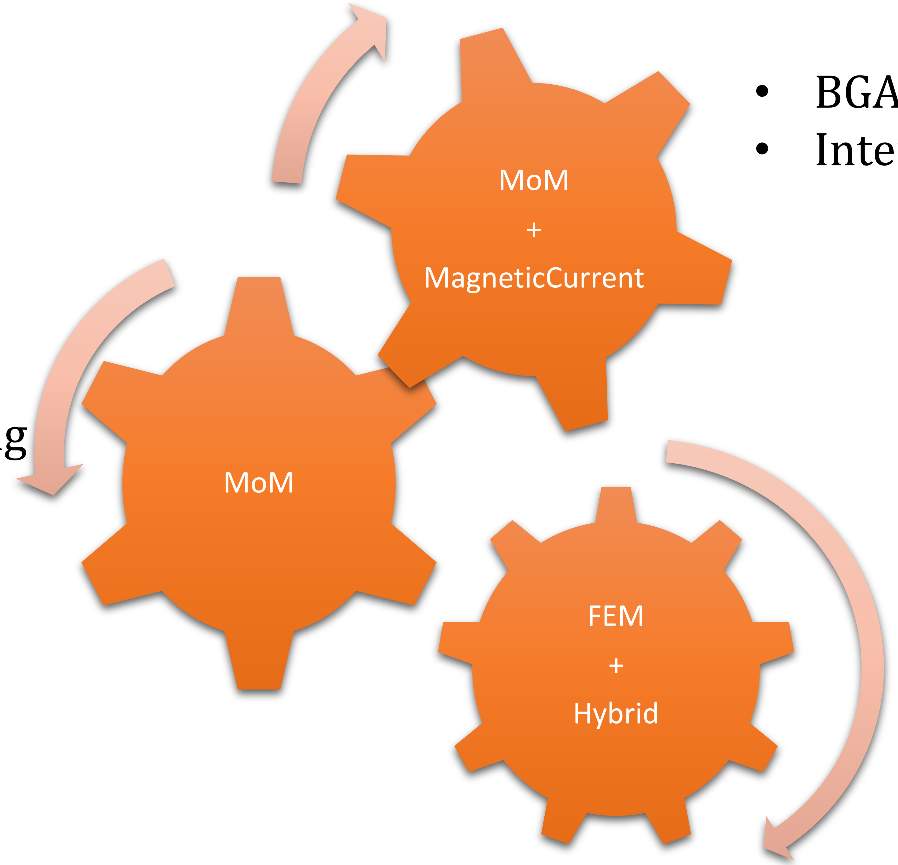


Need for fast EM solvers

- No single EM solver can solve all the problems with optimal accuracy and performance
- Method of Moments (MoM) solver, Finite Element Method (FEM), or hybrids solver can be the best solver for specific problems.

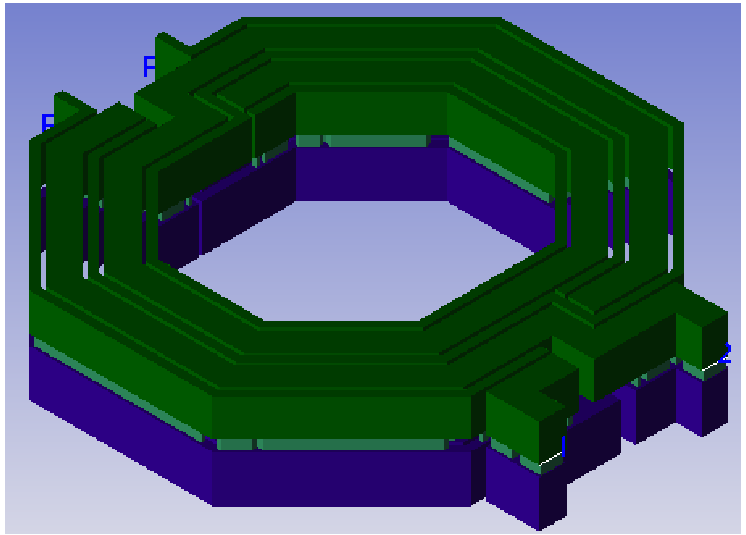
- BGA package simulation
- Interposer simulation

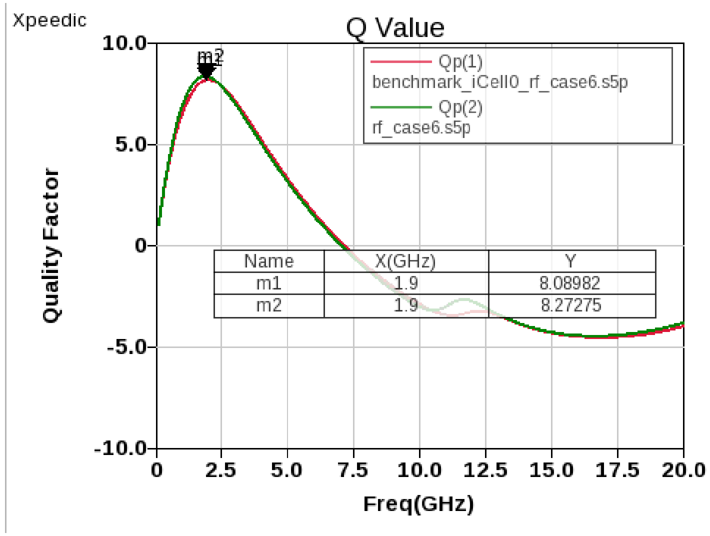
- On-chip passive modeling

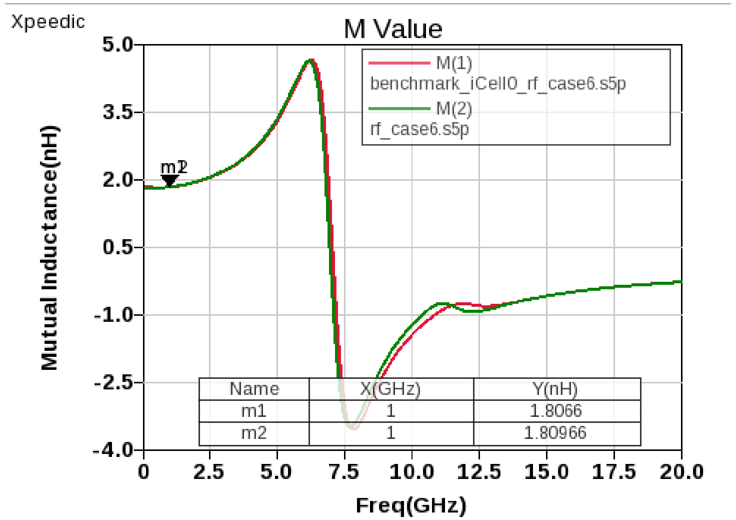


- 3D via modeling and simulation
- Full board crosstalk scan

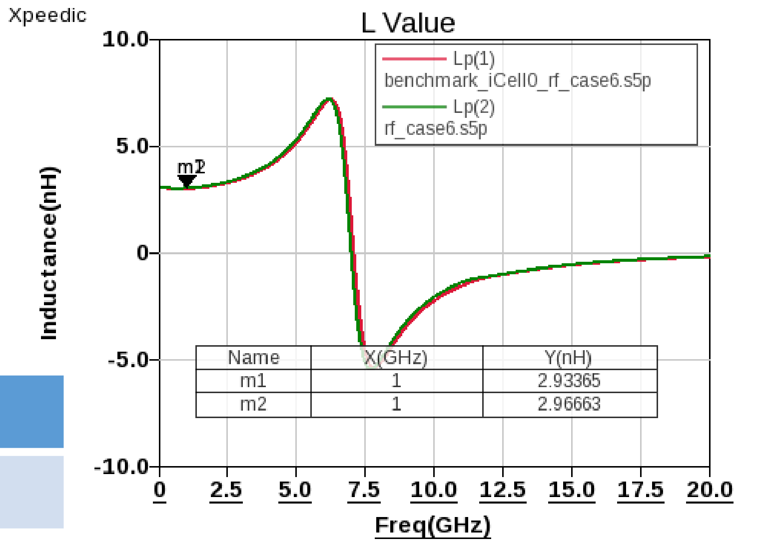
MoM for On-Chip Passive Modeling

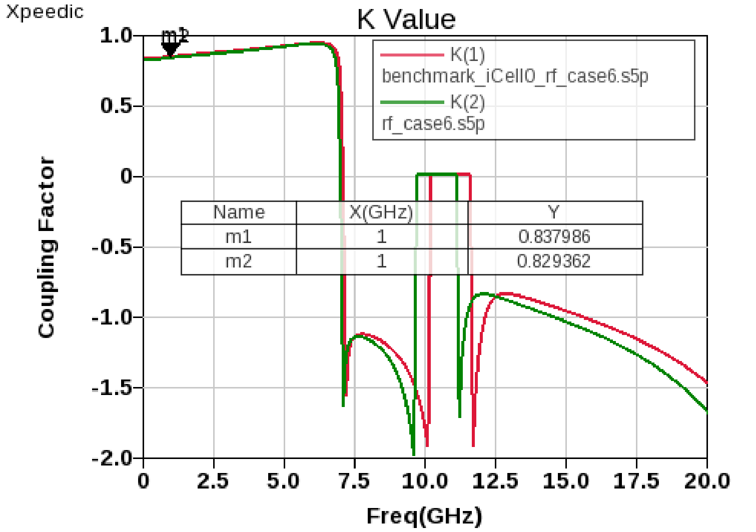






— **MoM Solver**
— **Ref1**

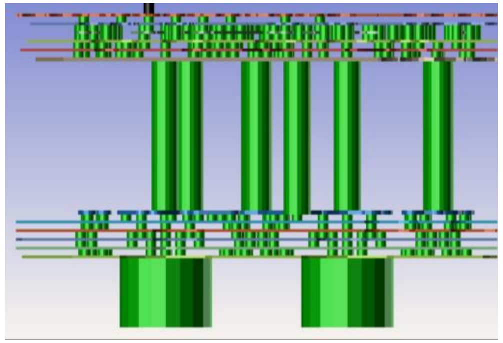




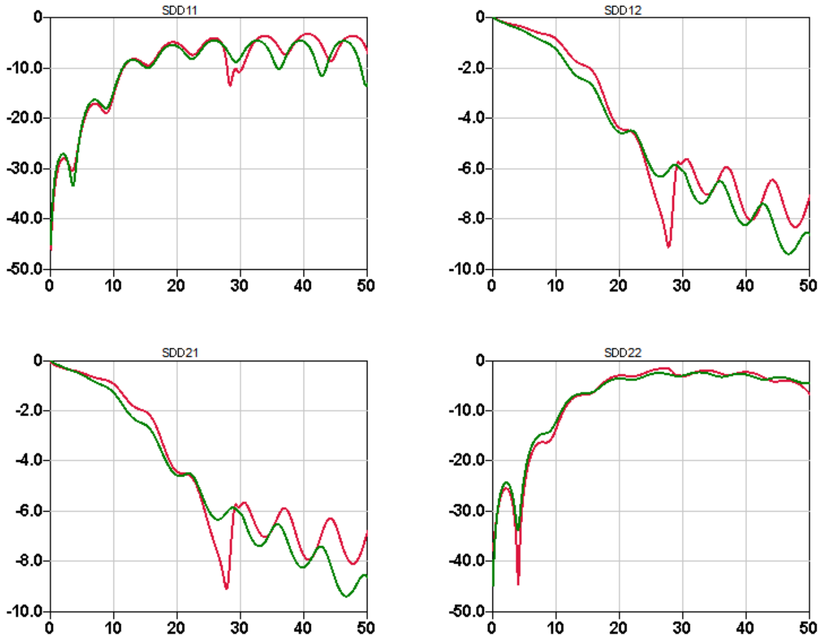
	Qpmax	Qsmax	Lp	Ls	M	K
Ref1	2.2%	5%	1.1%	1.3%	0.2%	1%

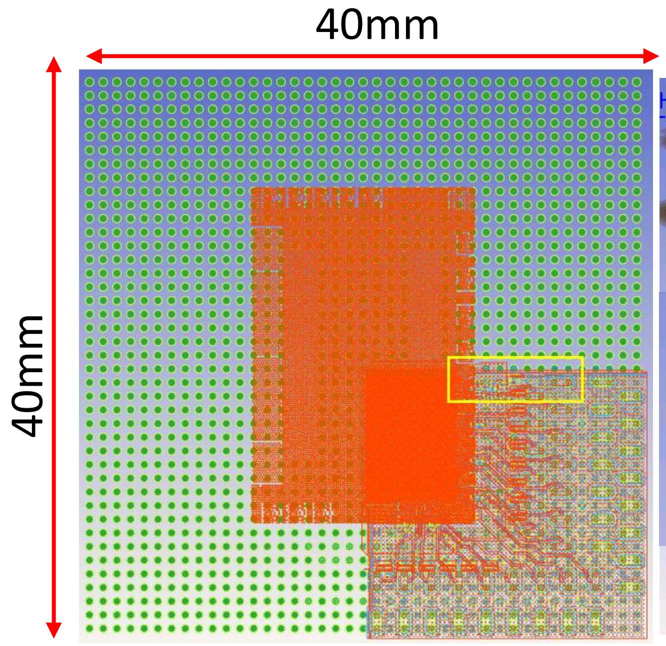
MoM for BGA Package Extraction

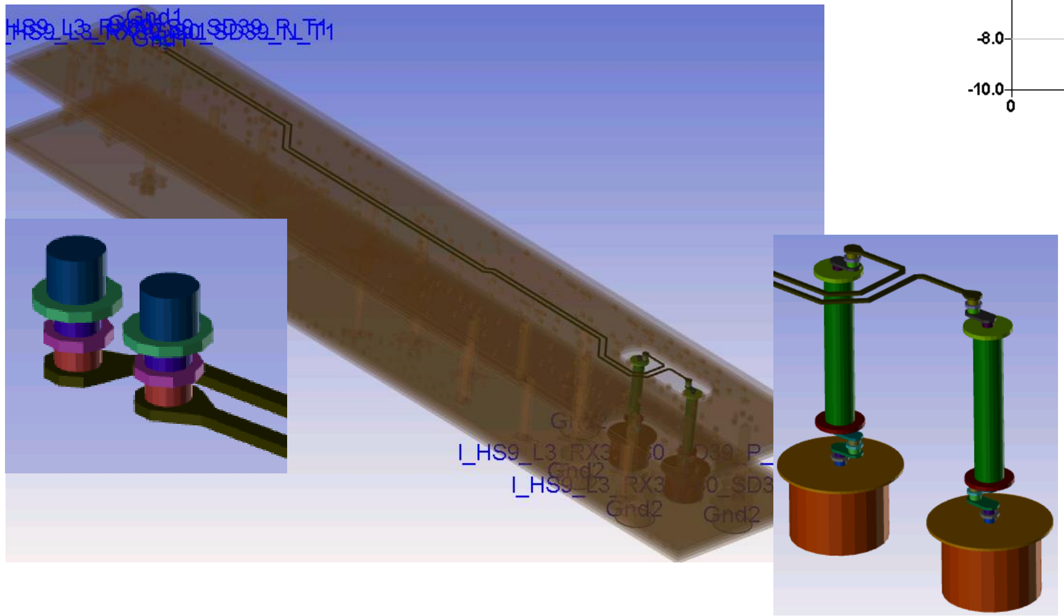
6-2-6 Stackup

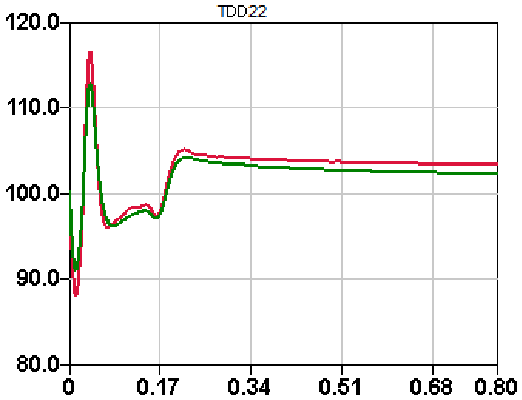


	unknowns	Number of Freq	Run Time
Pkg./IC Co-Sim.	89033	24	1h
Ref H	919w	25	5h

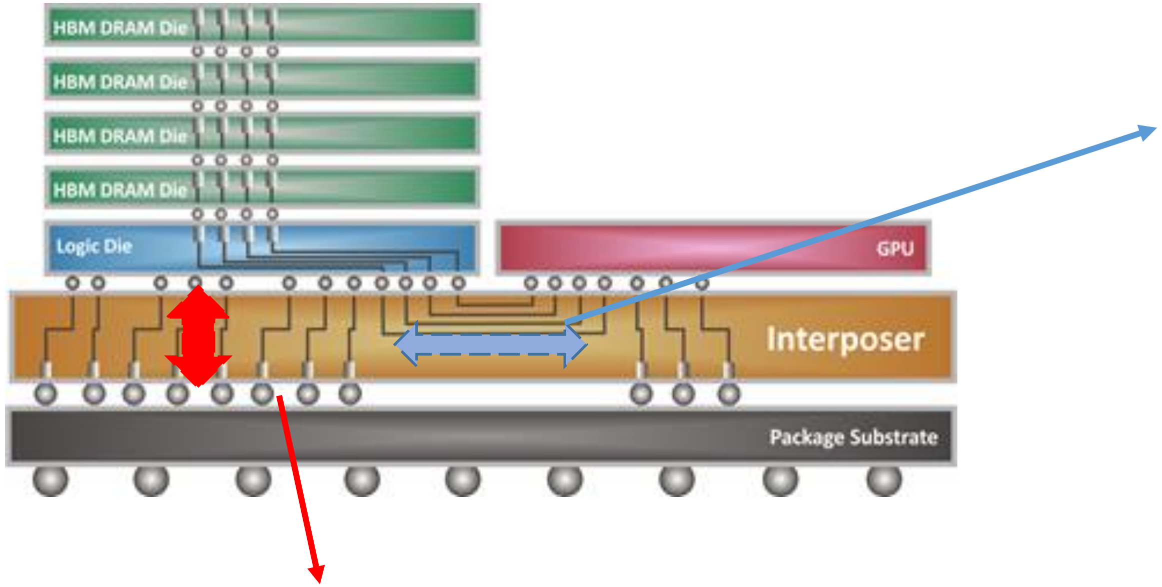




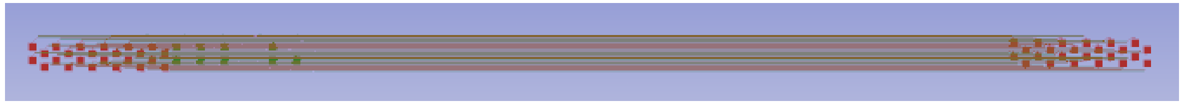


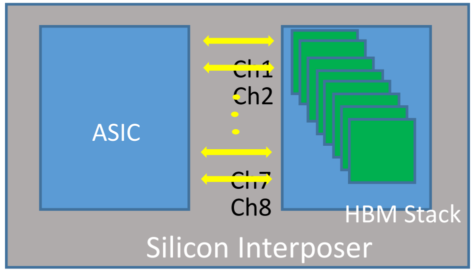


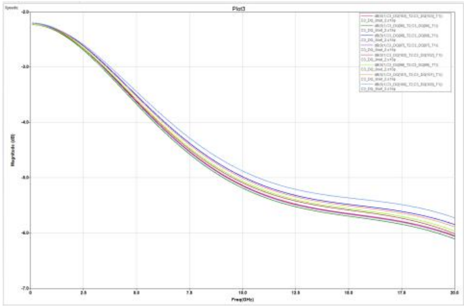
MoM for Interposer Analysis



High Speed Memory I/O Path
Large scale transmission line on mesh ground plane

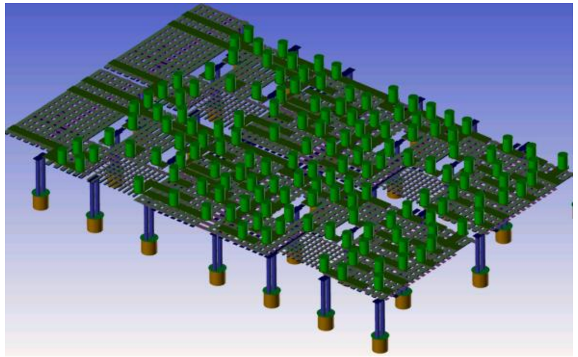


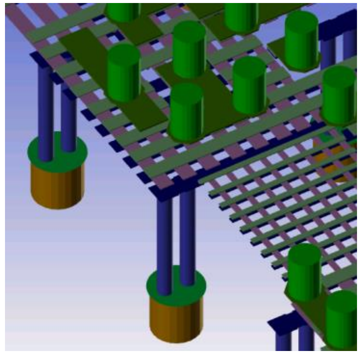




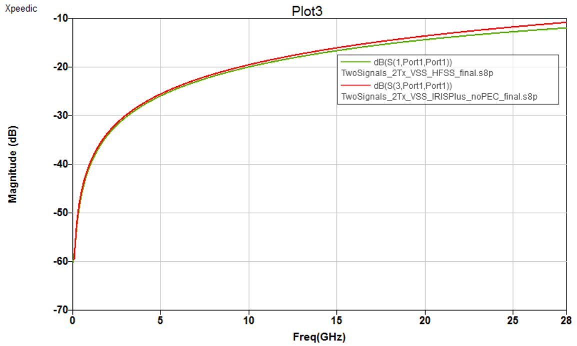
	Pkg./IC Co-Sim	Ref
Time	20min	3hr

High Speed Serial I/O Path (RDL->TSV)
Accurate TSV model is critical for SI





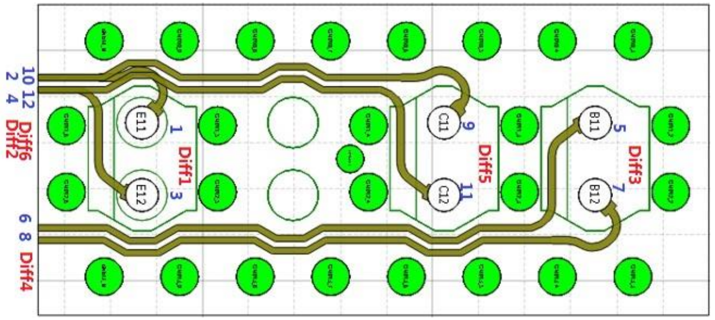
Return Loss

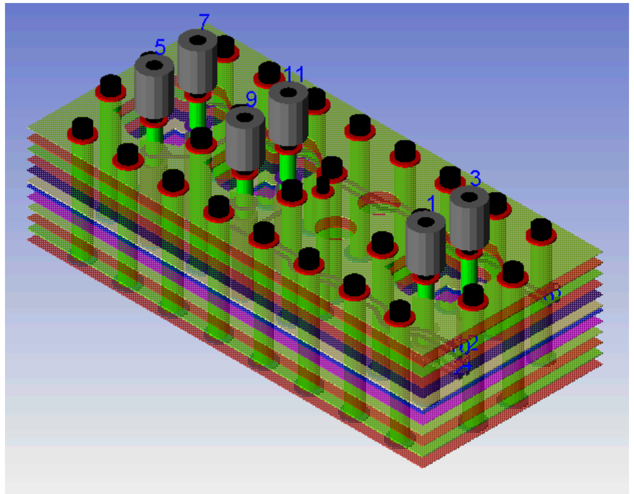


Faster

	MoM Solver	Ref
Time	56min	8hr

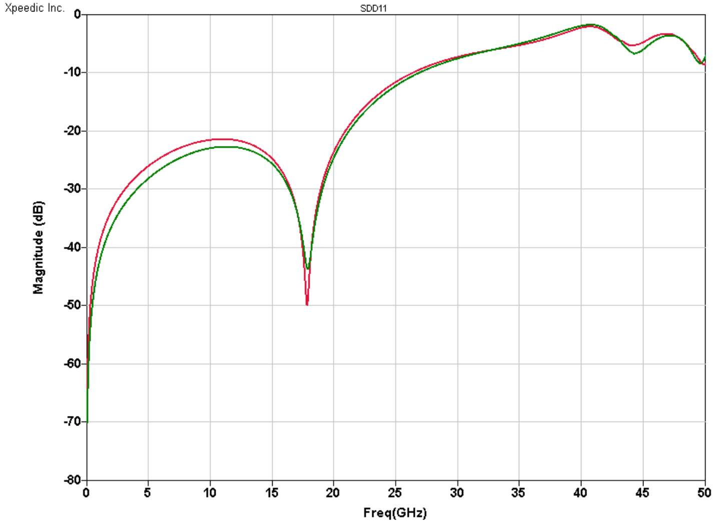
FEM Hybrid Solver for Board-level SI Analysis

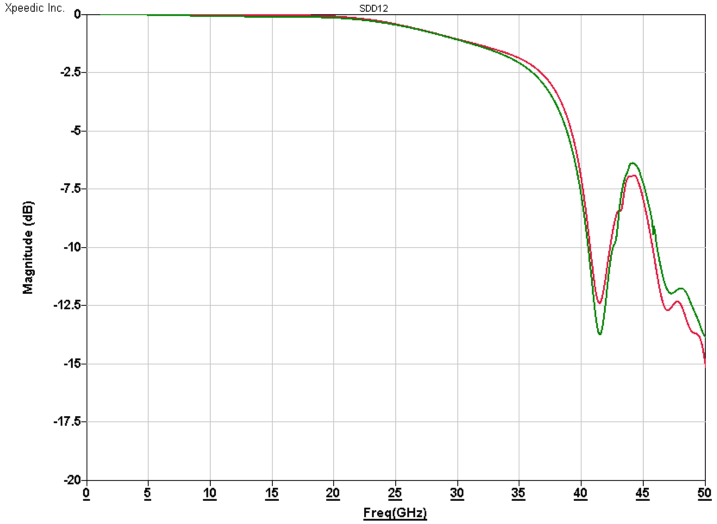




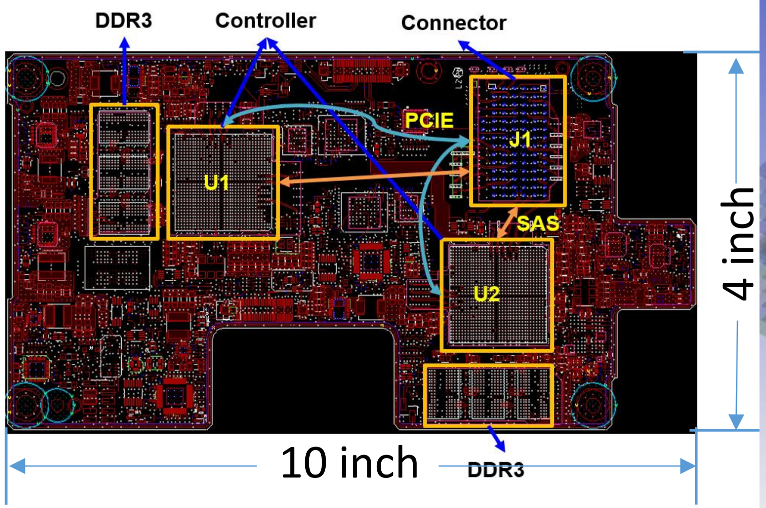
-- FEM Hybrid

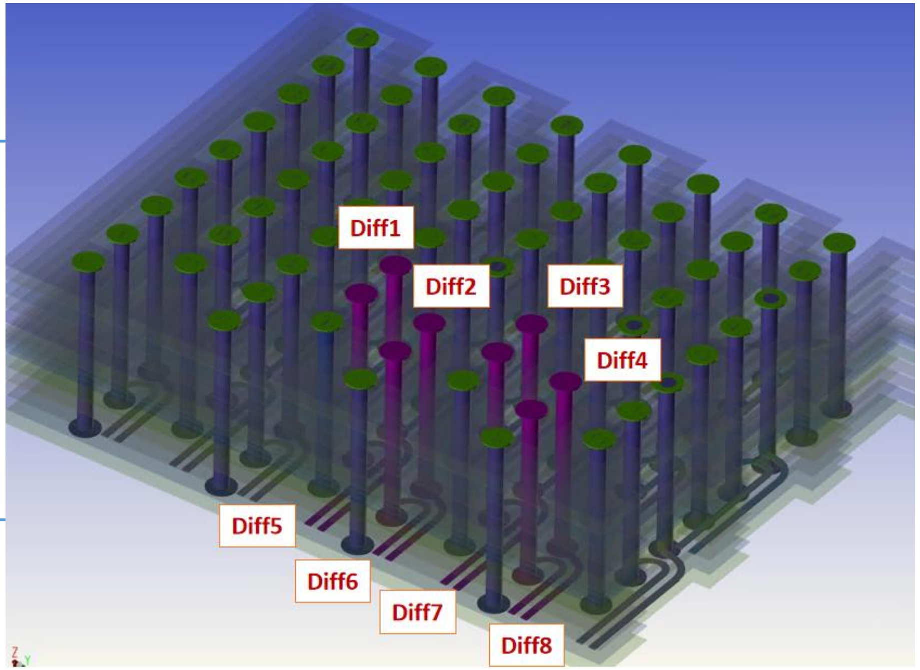
-- Ref H

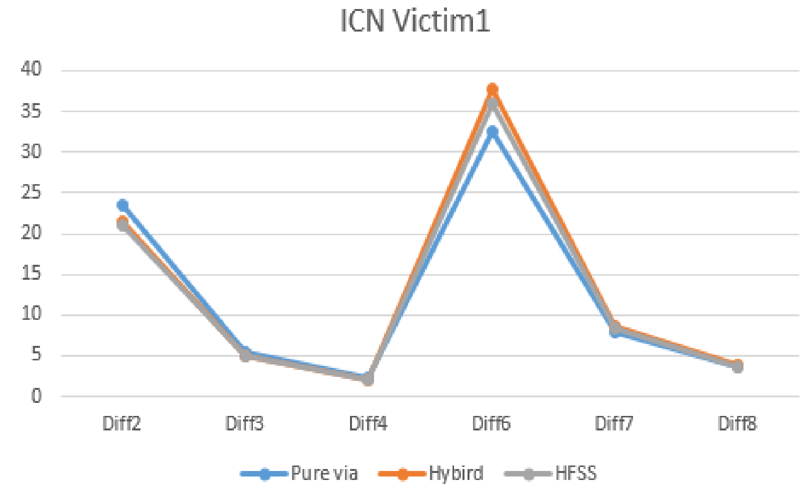


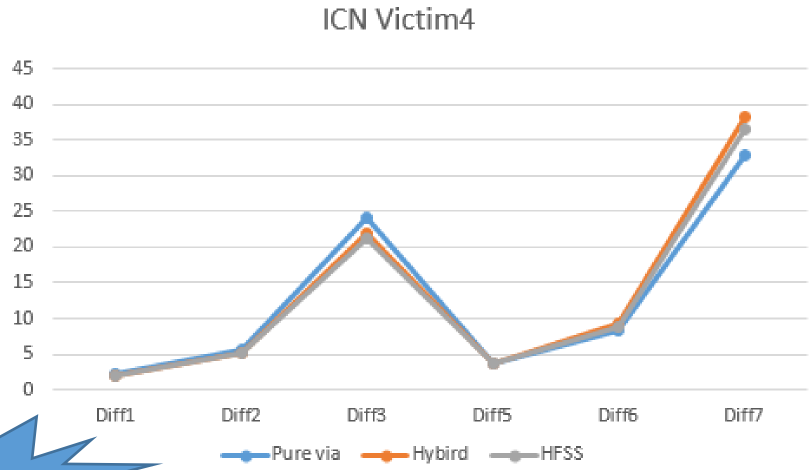


Via Solver for Board-level Crosstalk Analysis





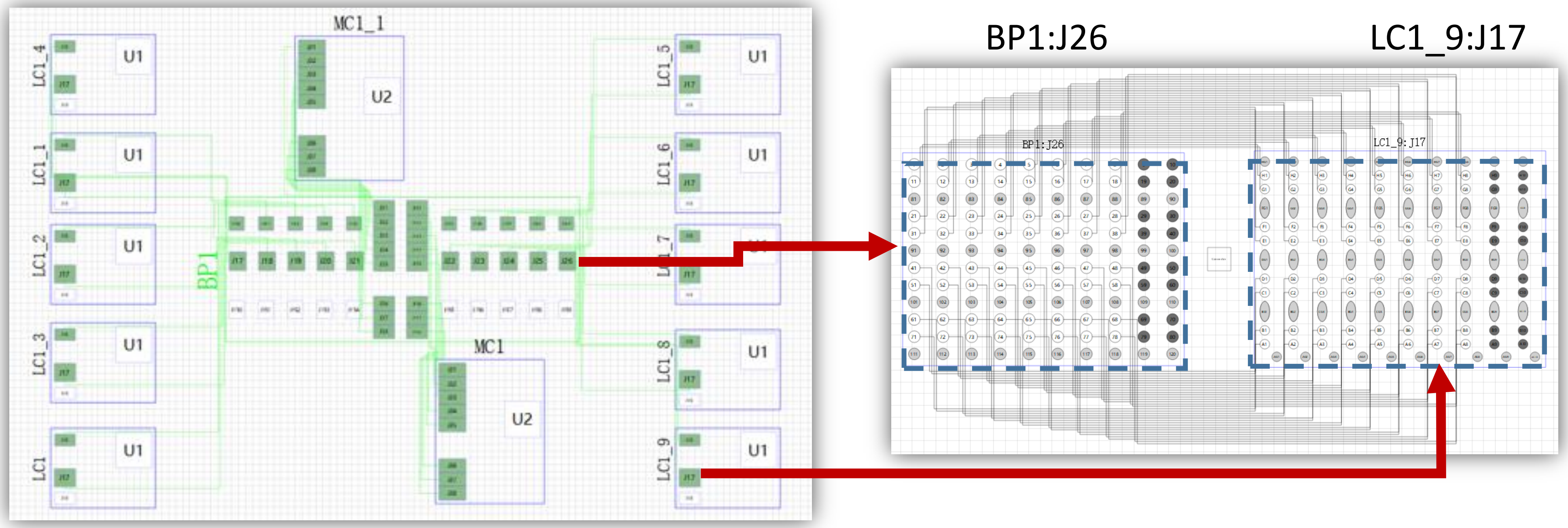


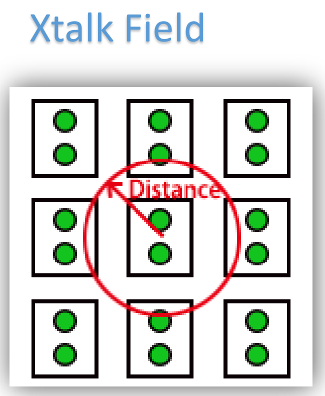


	Via Solver	Ref-H
Time	2min	60min

Faster

II: Quick assembly of multi-board channel

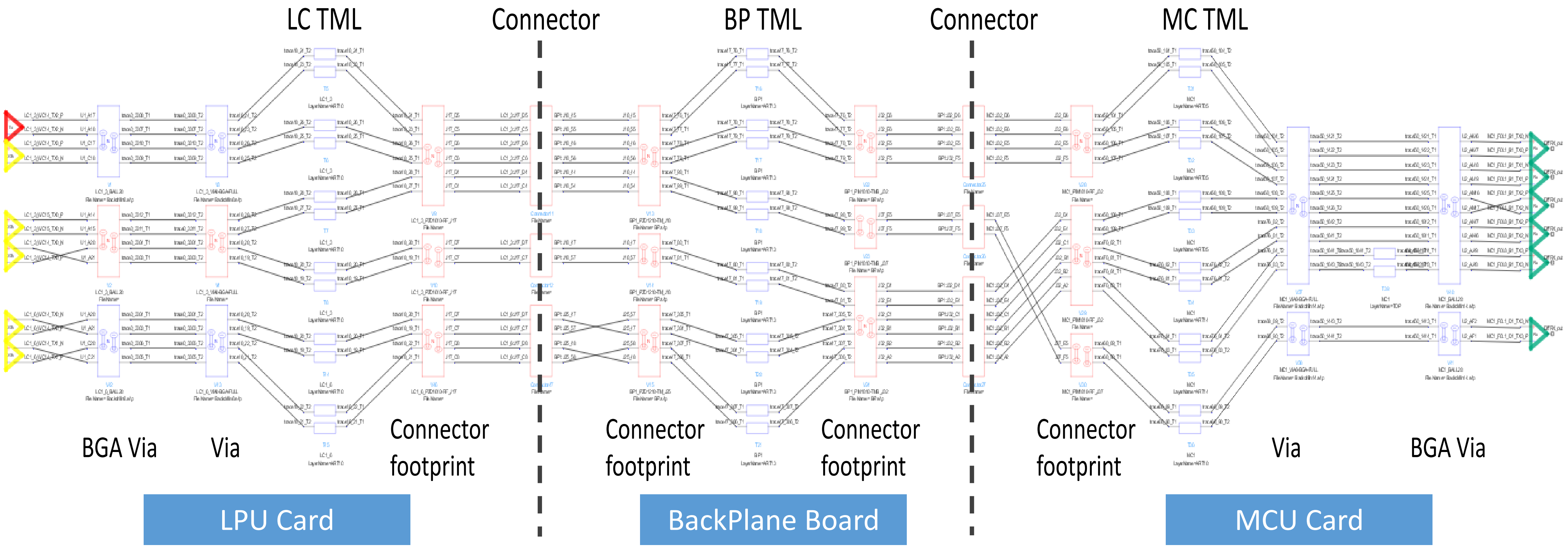




1. Multi-board system with connector RefDes
2. Board-to-board connectivity is established by connector pin-mapping
3. Neighboring nets for crosstalk can be defined.

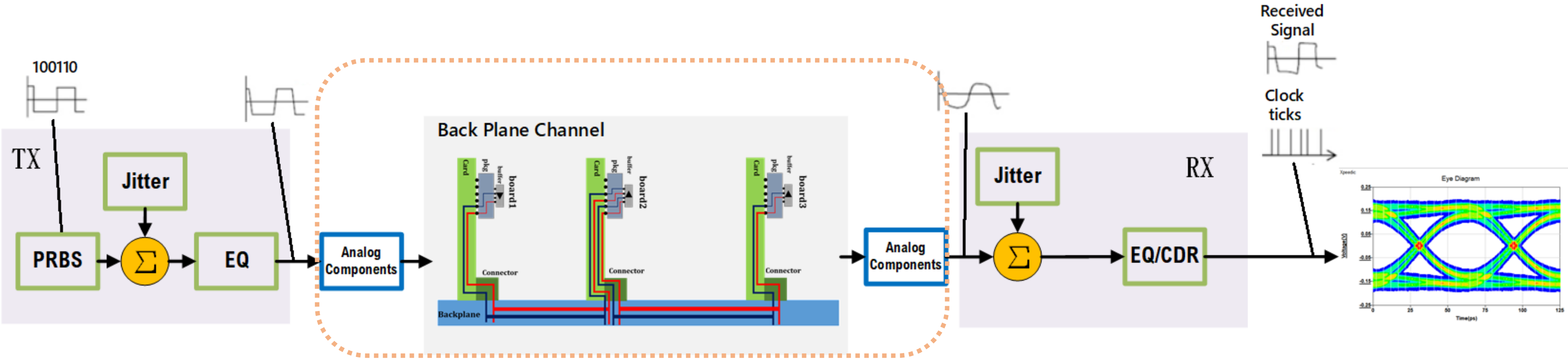
Building channels with or without crosstalk across multi-board backplane system can be automated

Auto EM model build to create the channel

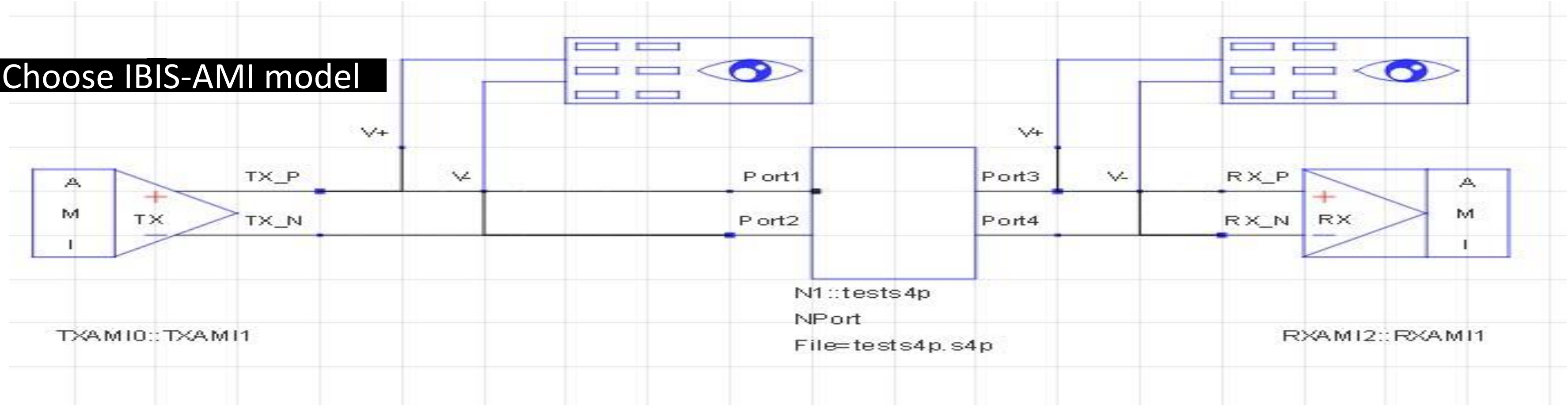


- S-parameter, SPICE, etc. models can be extracted.
- Transmission line is extracted by 2D solver.
- Via is extracted by FEM or Hybrid solver.

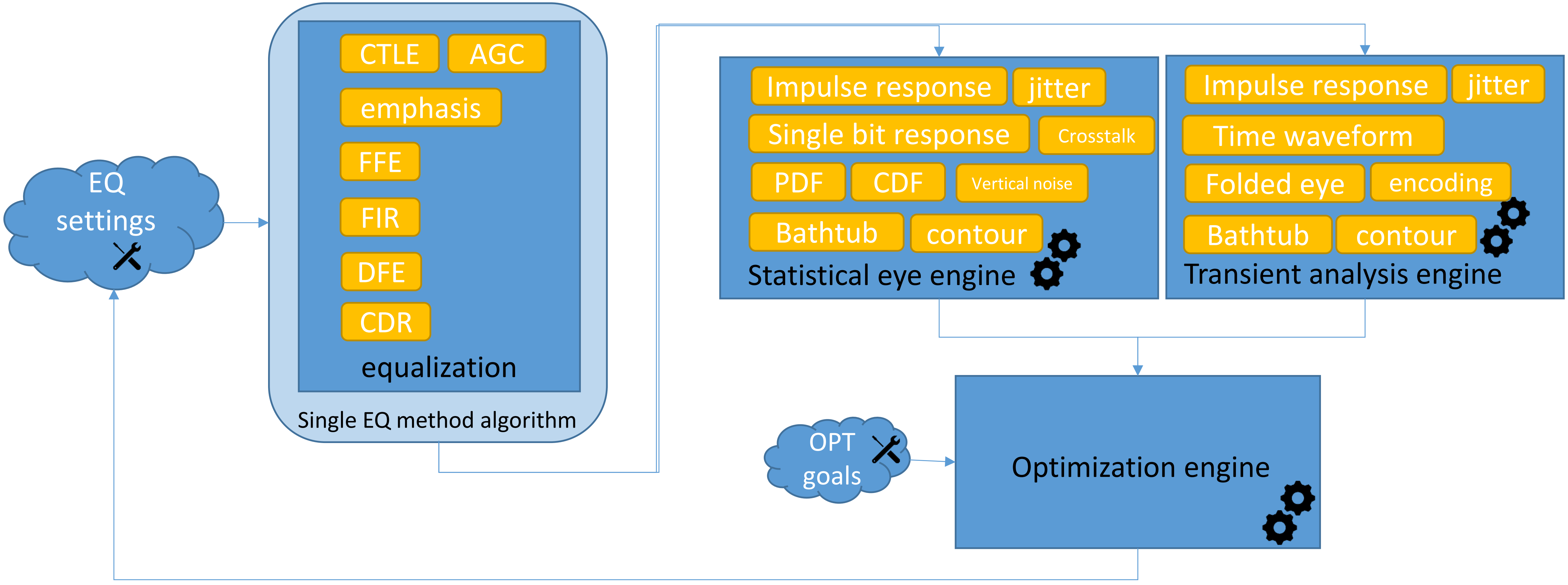
III: SerDes channel analysis with IBIS-AMI model



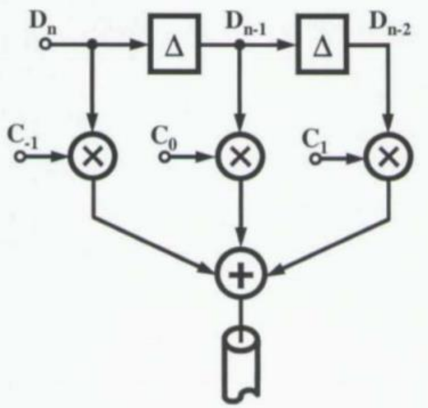
Choose IBIS-AMI model

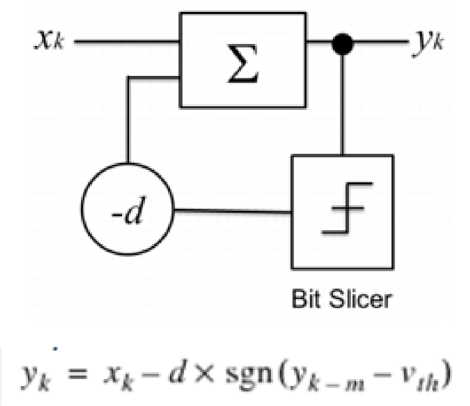


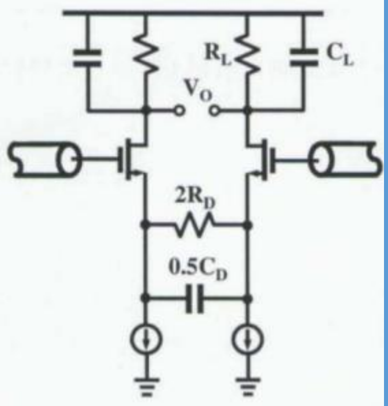
IV: IBIS-AMI Equalization Optimization



Comparison of Equalization Methods

<table>
<tr>
<th>CTLE


</th>
<th>FFE


</th>
<th>DFE


</th>
</tr>
<tr>
<td>

- More gain at main energy frequency
- Amplifying signal also amplifies noise + crosstalk(no better SNR)
- Trade-off: High Gain + Output Swing vs. Small size + Low power consumption

</td>
<td>

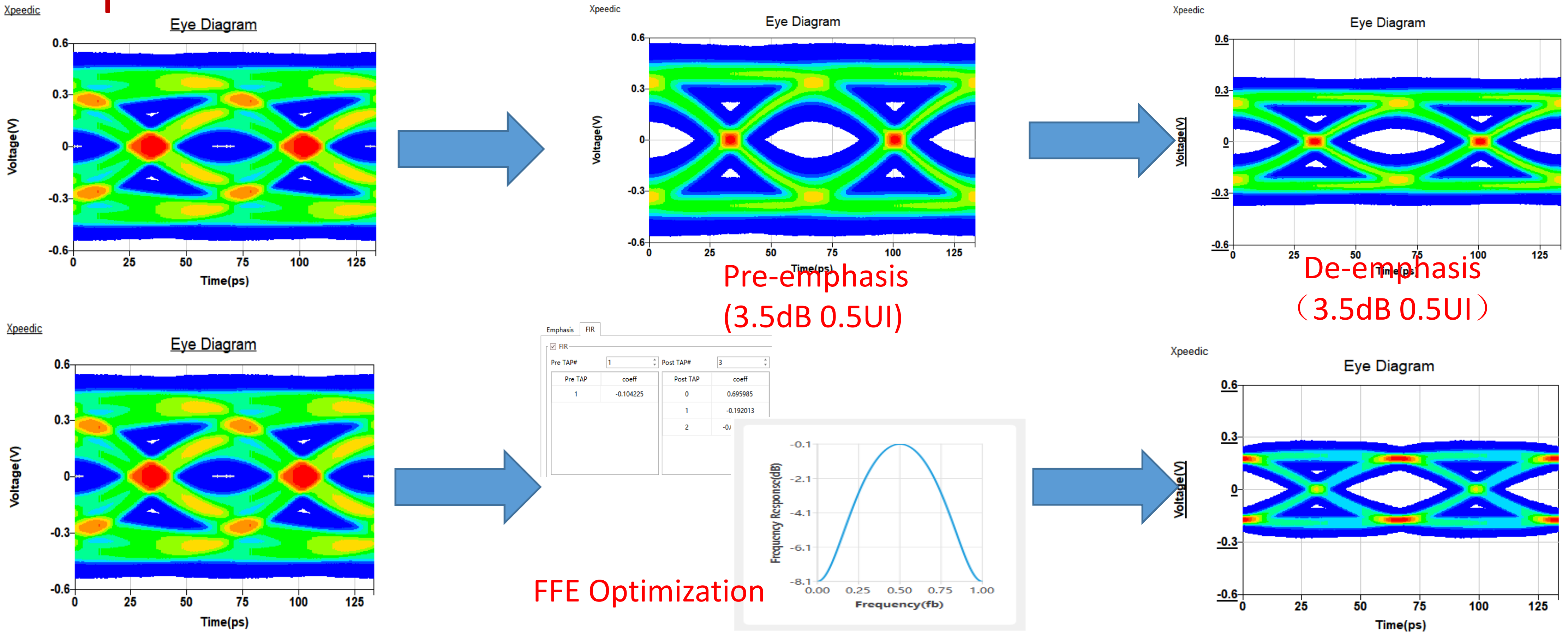
- Doesn’t amplify noise
- Easily cancels precursors
- Signal Attenuated due to peak-power limitation

</td>
<td>

- Non-linear equalizer
- Discrete-Time equalizer clocked by data transfer clock
- No amplification of noise + crosstalk
- Can only account for post-cursor(no pre-cursors)

</td>
</tr>
<tr>
<td>Only works well with linear loss channels</td>
<td>Can mitigate the pre-cursor channel response in low-BW channels.
Can compensate ISI arising from transient TL loss over wide time-spans.</td>
<td>Cannot equalize ISI arising from pre-cursor channel response.
Can only compensate ISI from a fixed time-spans.</td>
</tr>
</table>

Equalization Benchmark



- Equalization play a key role as we switch from baseband, two-level NRZ (non-return to zero) to PAM4 (four-level pulse-amplitude modulation) at lane rates in excess of 50 Gbits/s

Simulation Setup

Compliance
- IEEE 802.3
- OIF CEI
- PCIe
- ….

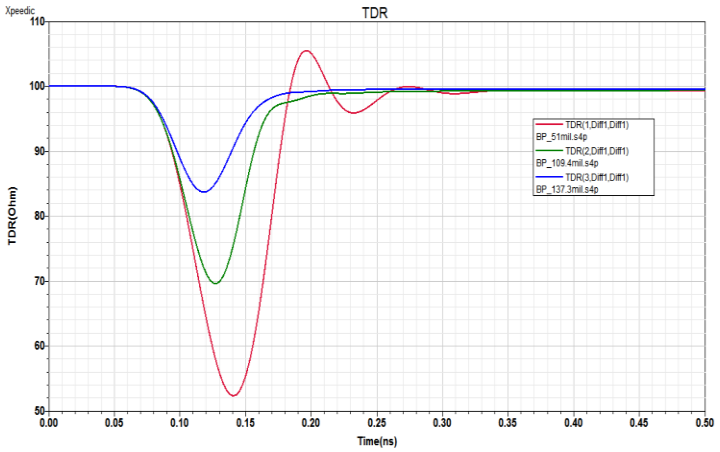
Freq domain simulation
- S-parameter
- Insertion loss
- Return loss
- Crosstalk
- TDR
- ….

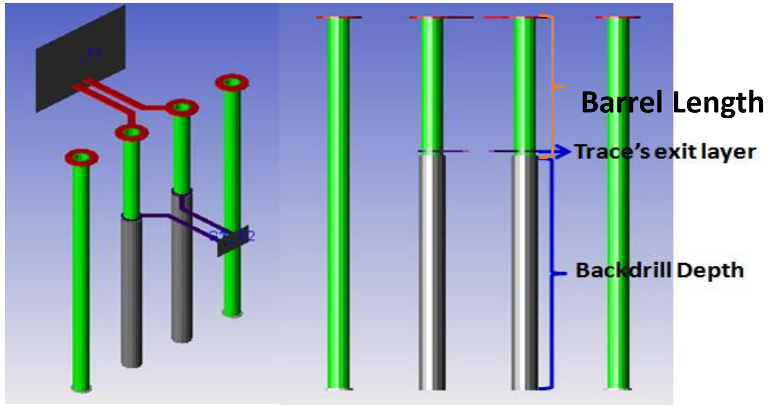
Eye simulation
- Eye diagram
- Bathtub curve
- Eye BER contour
- ….

COM simulation
- FOM margin
- ….

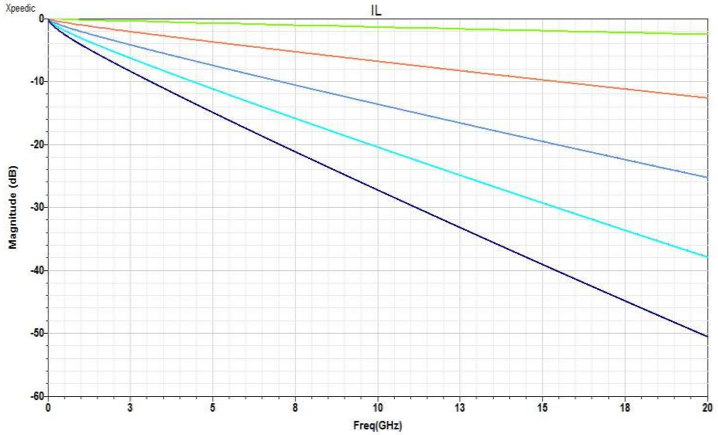
Support various parametric simulation

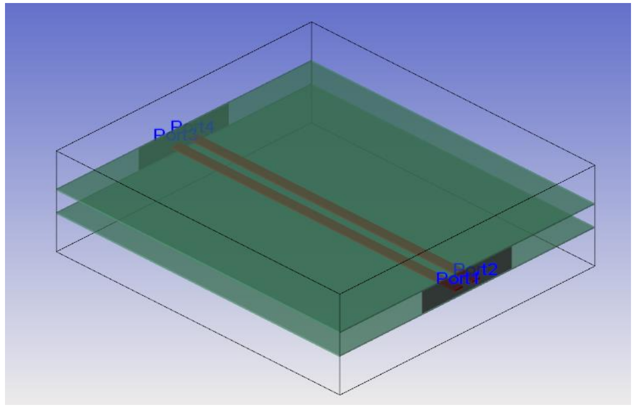
S parameter parametric



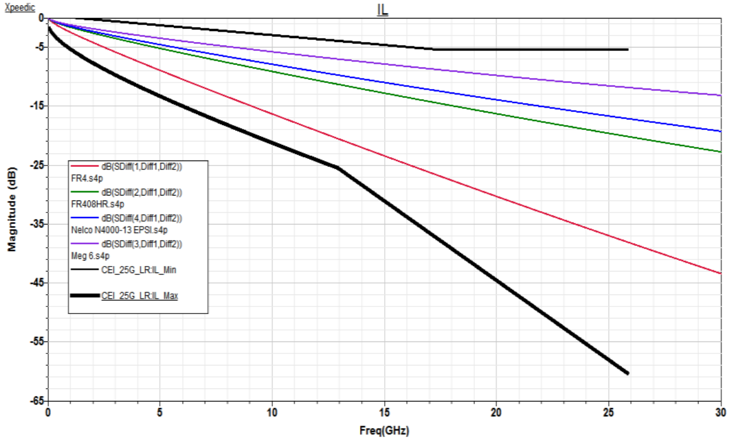


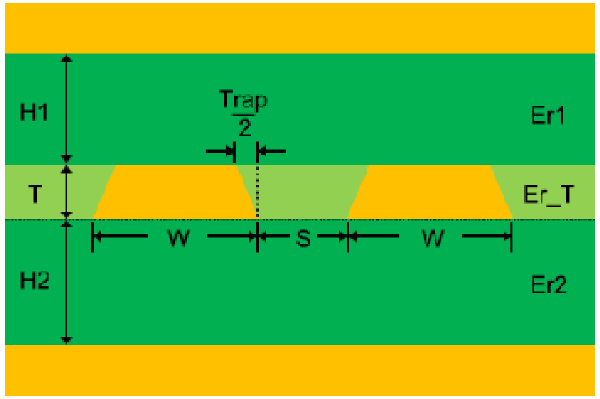
Support on TML Length



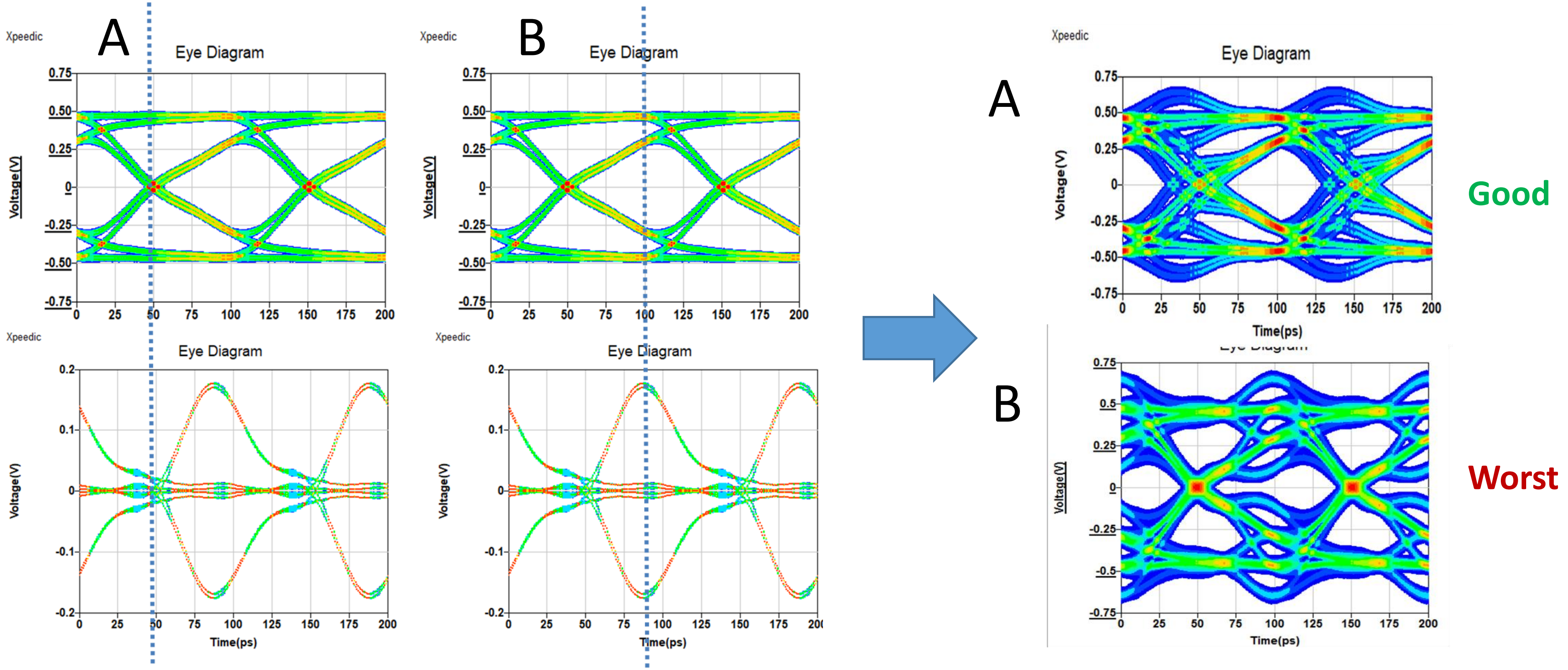


Support on TML Substrate



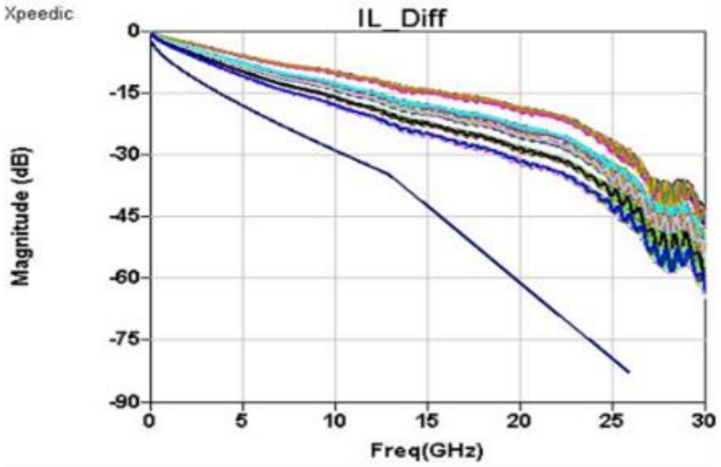


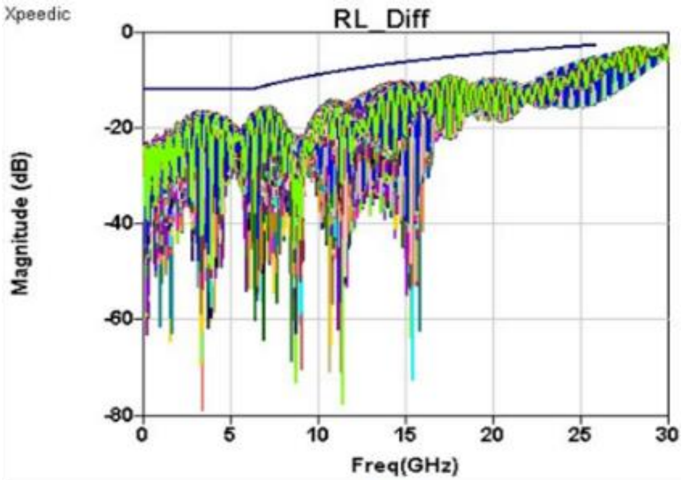
How to get a worst case of multi-channel crosstalk?

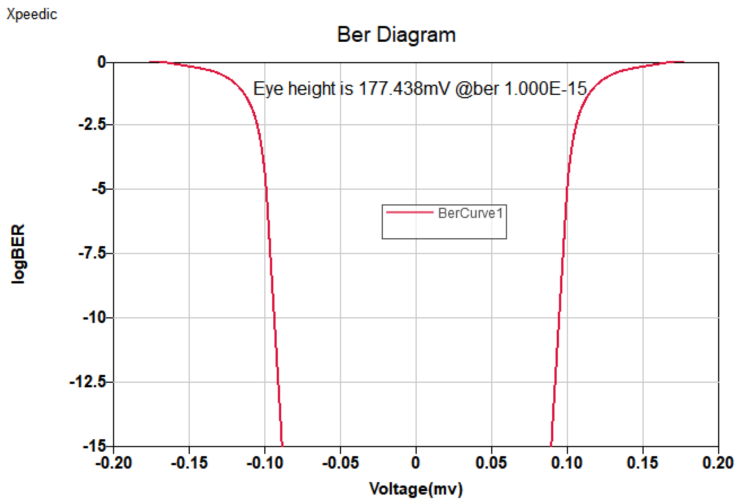


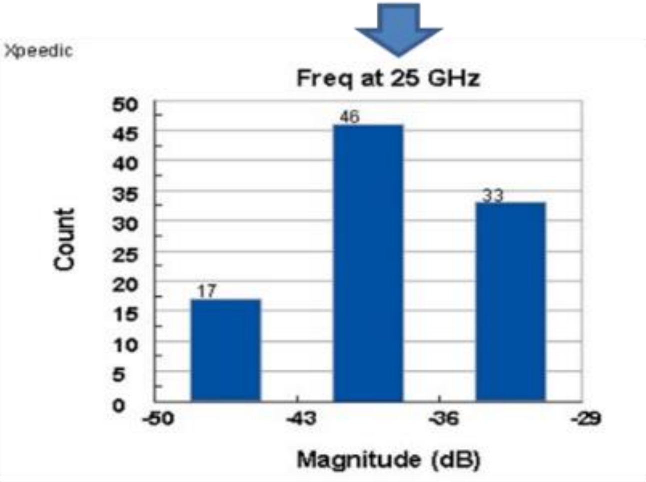
- Different aggressor channel delay will make eye diagram different.
- Adaptive adjustment of phase delay between aggressors and victim.
- The maximum crosstalk noise is added to achieve worst case analysis and increase design margin.

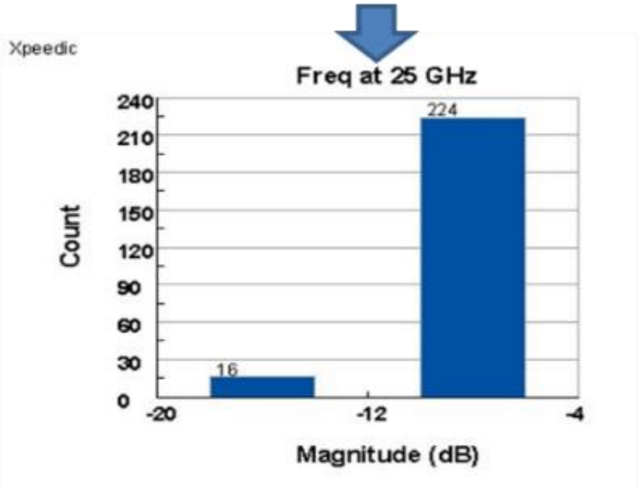
Result: Eye Diagram

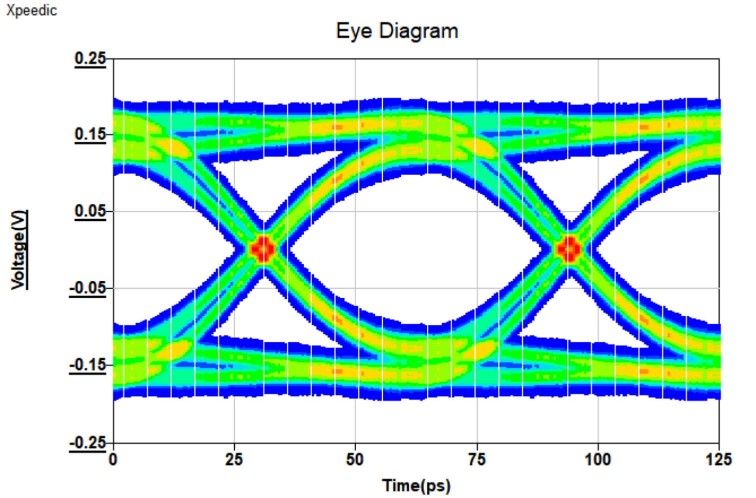




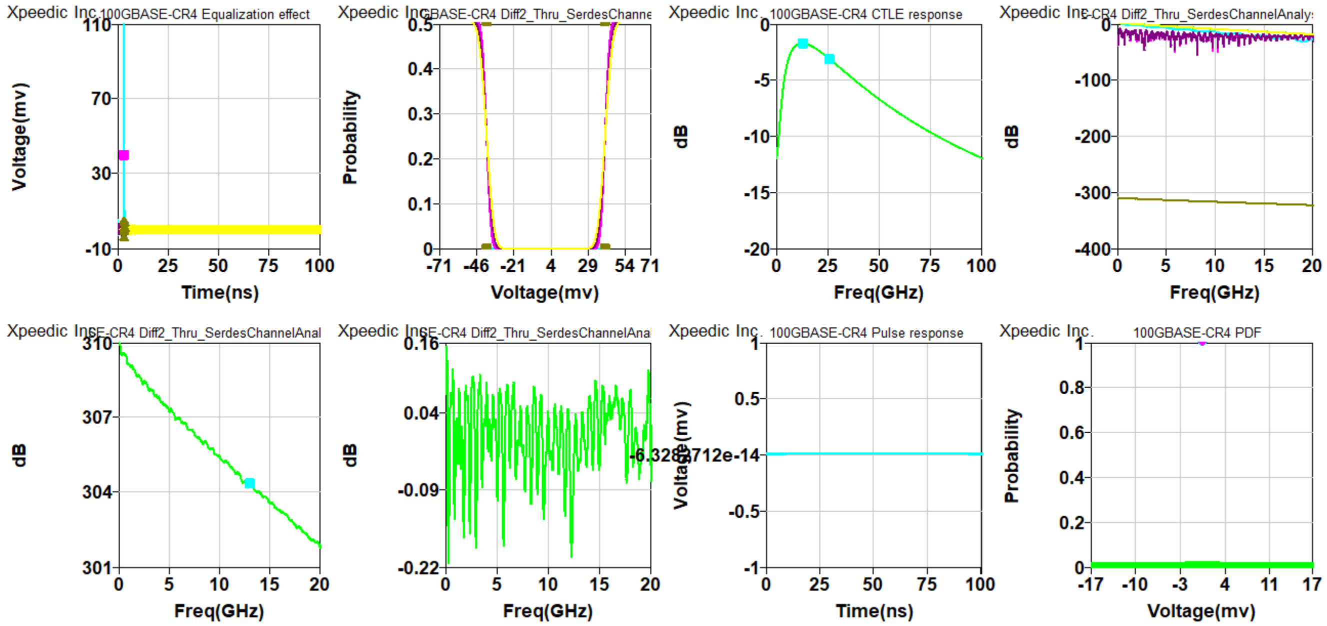








Result: COM (Channel Operating Margin)



Name	100GBASE-CR4 Case1_Value
FOM	21.0051 dB
TXFFE coefficients	-0.12 0.82 -0.06
CTLE DC gain	-12 dB
CTLE peaking gain	-1.86853 dB
Available signal	0.0539662 dB
levels	2
Pkg_len_TX	12
Pkg_len_NEXT	12
Pkg_len_FEXT	12
Pkg_len_RX	12
baud_rate_GHz	25.7813
f_Nyquist_GHz	12.8906
channel_operating_margin_dB	9.16853
peak_interference_mV	18.78
peak_channel_interference_mV	10.14
peak_ISI_mV	10.14

If COM value < 3dB, it will be shown in Red.

Summary

- Multi-board SerDes channel simulation becomes challenging;
- The presentation shows multiple ways to alleviate the challenges including
  - Multiple EM solver techniques to quickly build models for discontinuities along the channel
  - Quick channel assembly for multi-board backplane system with connector pin-mapping
  - SerDes channel analysis with IBIS-AMI model
  - IBIS-AMI equalization optimization to achieve the optimal channel performance

XPEEDIC

ACCELERATE YOUR IC DESIGN