DDR5 AMI Modeling and Simulation

Jiarui WU	***2020.11.20***
Application Engineer / Keysight Technologies	
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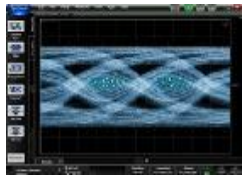
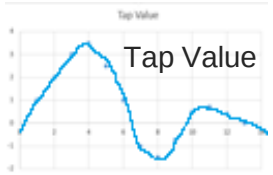
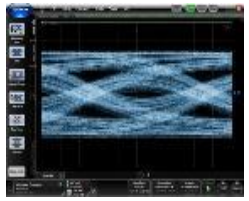
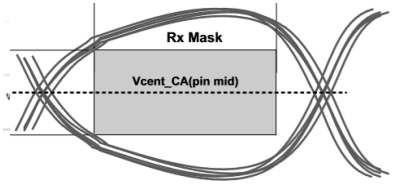
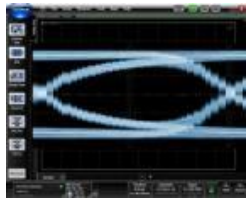
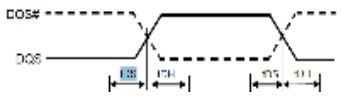
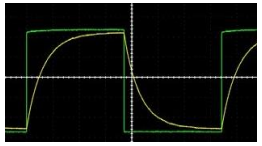
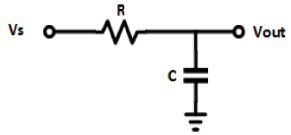
Agenda

- DDR5 Introduction
- DDR5 Main Challenges
- DDR5 Simulation and Modeling Solutions
  - Channel Simulation
  - Why IBIS AMI?
  - DDR5 AMI Challenges & Solutions

DDR5 Introduction

DDR5 Introduction

Signal	MT/s (Mega Transfers Per second)	Generation	Characteristics	Specification	Introduction
	3200 – 8400	DDR5	"Hyper Speed" • Eye collapses • Impulse response • BER Rj/Dj, Rn/Dn		2019
	1600 – 3200	DDR4	"Serial Speed" • Eye Diagrams • Rx Masks • Bit error rates		2014
	200 – 1600	DDR/2/3	"High Speed Digital" • Transmission lines • Ts / Th, Skew		2002
	33 – 133	SDRAM	"Low Speed" • Fanout • Capacitance		1961

DDR4 Vs. DDR5

Feature	DDR4	DDR5
Data rates	1600-3200 MT/s	3200-8400 MT/s
$V_{DD}/V_{DDQ}/V_{PP}$	1.2/1.2/2.5	1.1/1.1/1.8
Internal V_{REF}	V_{REFDQ}	V_{REFDQ}, V_{REFCA}, V_{REFCS}
DQ receiver equalization	CTLE	DFE
Write leveling training modes	Yes	Improved
Loopback mode	None	Yes

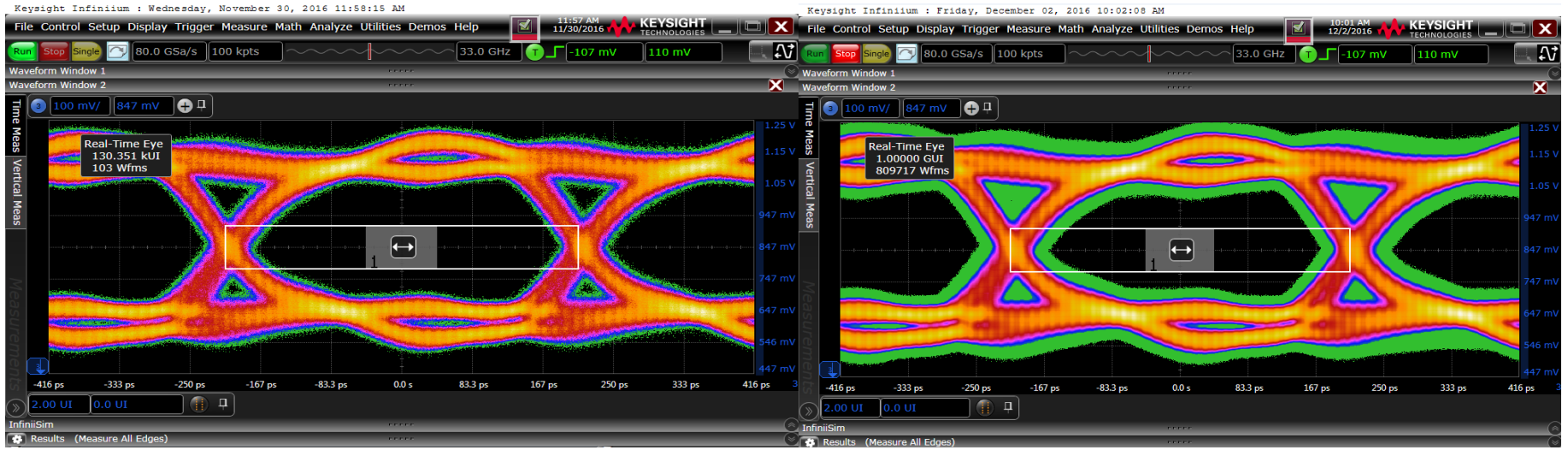
DDR5 Main Challenges

DDR5 Challenges - Jitter

BER Contour at 1e-16 tells us the Real Margin

Number of UI	BER	Eye Width	Eye Height
1.3e5	7.69e-6	352.72 ps	310.9 mv
2.80e6	3.57e-7	347.52 ps	288.3 mv
6.31e7	1.58e-8	339.70 ps	275.8 mv
1.10e8	9.13e-9	339.06 ps	271.1 mv
1e9	1e-9	336.45 ps	265.6 mv

- Higher Data Rate → Higher ISI
- ISI & RJ will decrease timing margin.
- Rx Eye Diagram/BER Contour need to be simulated/measured under low BER (1E-16)



DDR5 Challenges - Jitter

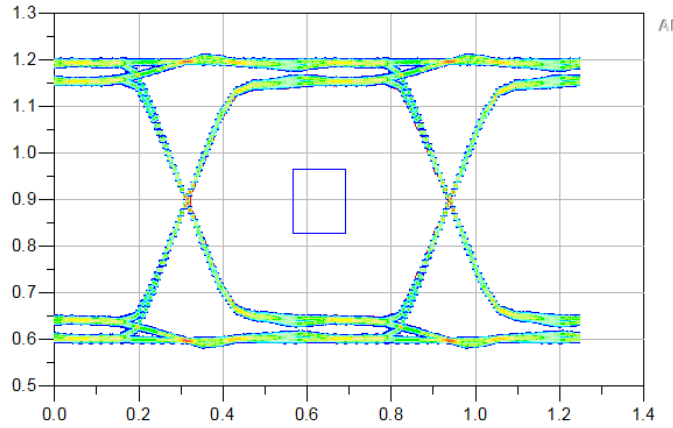
Jitter injected at Tx, and eye measured at the DRAM Solder-Ball (Rx Input)

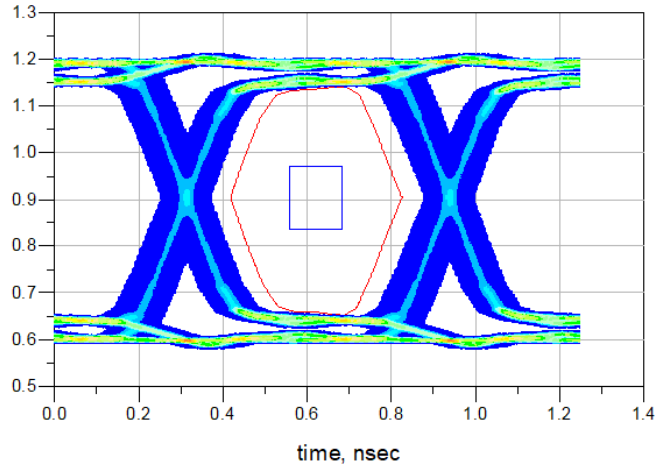
BER Contour at 1e-16 tells us the Real Margin

No Jitter – Just ISI from Channel

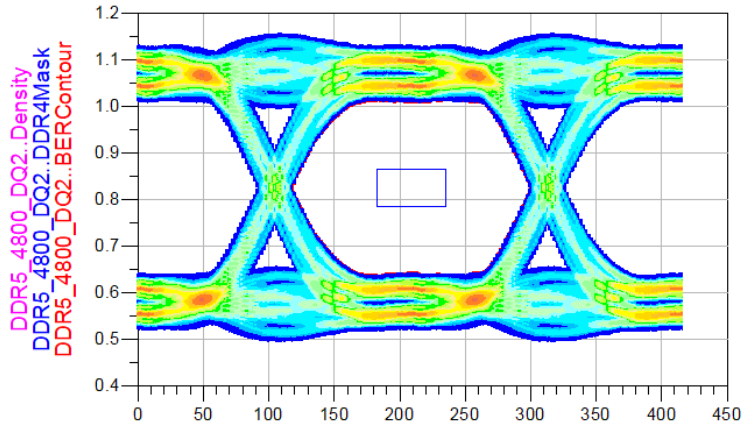
Random Jitter = 0.02 UI Applied at Tx (2%)

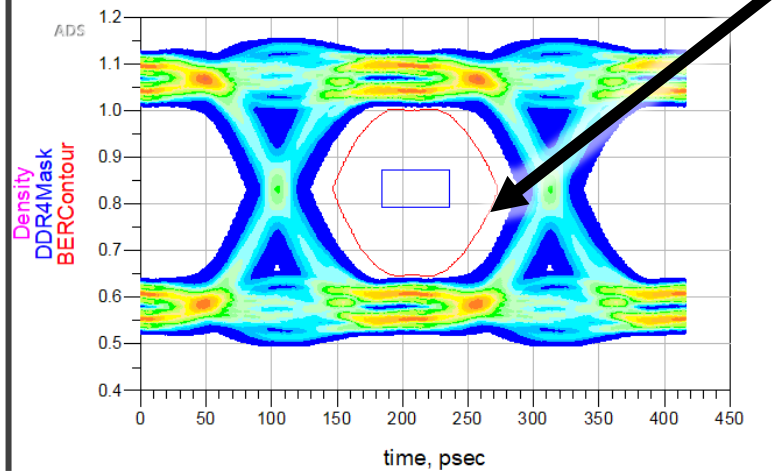
DDR4-1600





DDR5-4800





No Jitter – More ISI from Channel due to higher speed

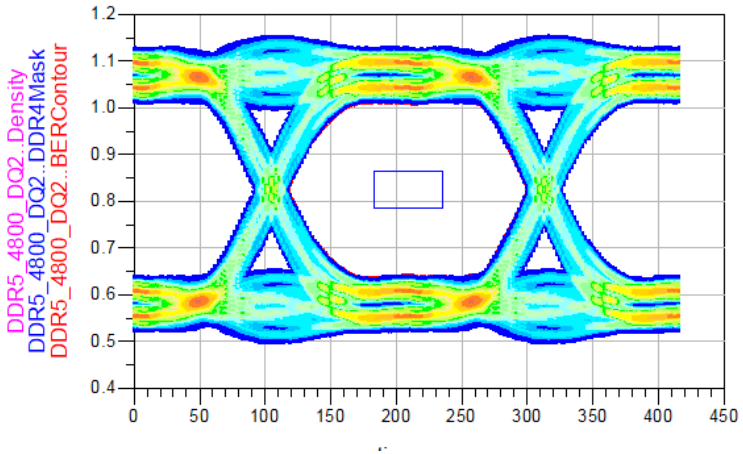
47% Reduction in Timing Margin

(27ps less margin to mask)

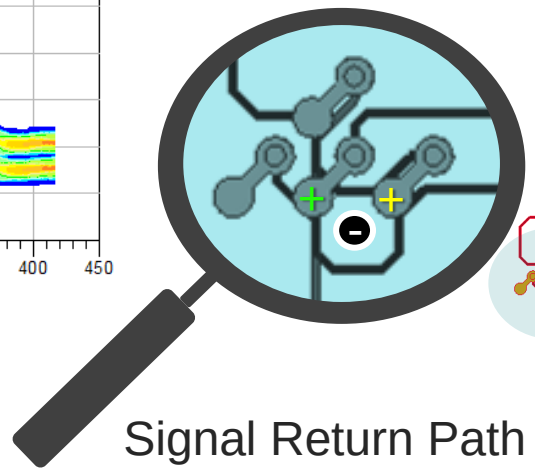
DDR5 Challenges - Crosstalk

The Importance of the Signal RETURN PATH

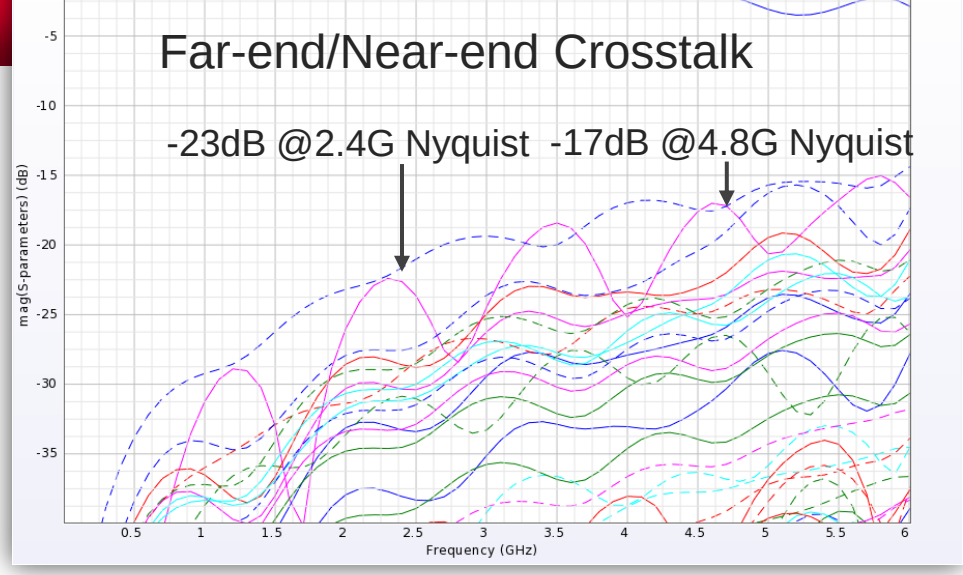
DDR5-4800

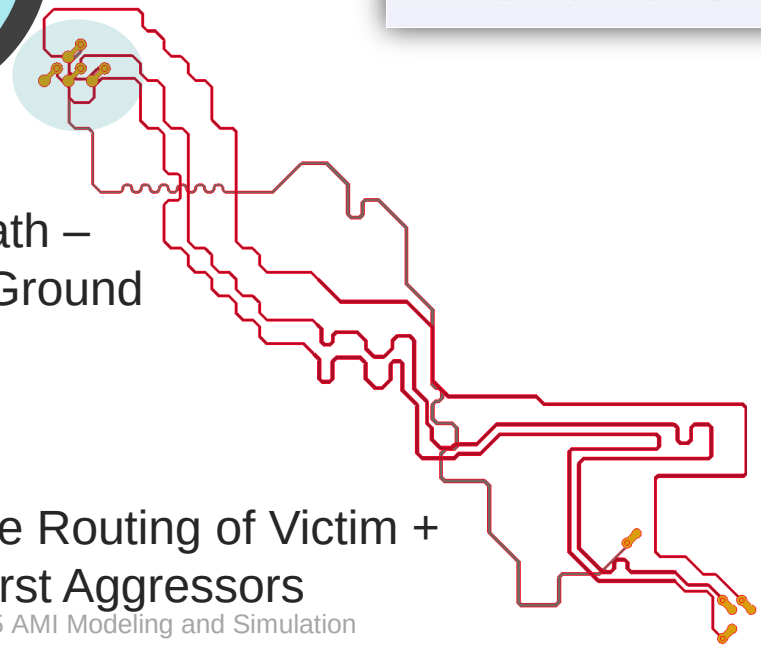


No Crosstalk, No Jitter – Just ISI from Channel

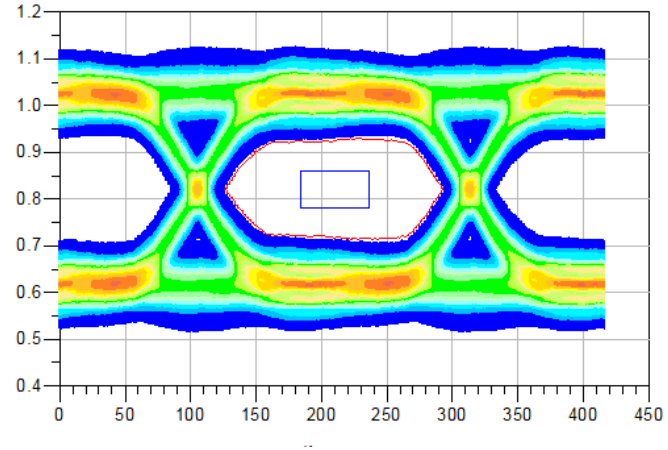


Signal Return Path – through shared Ground Pin





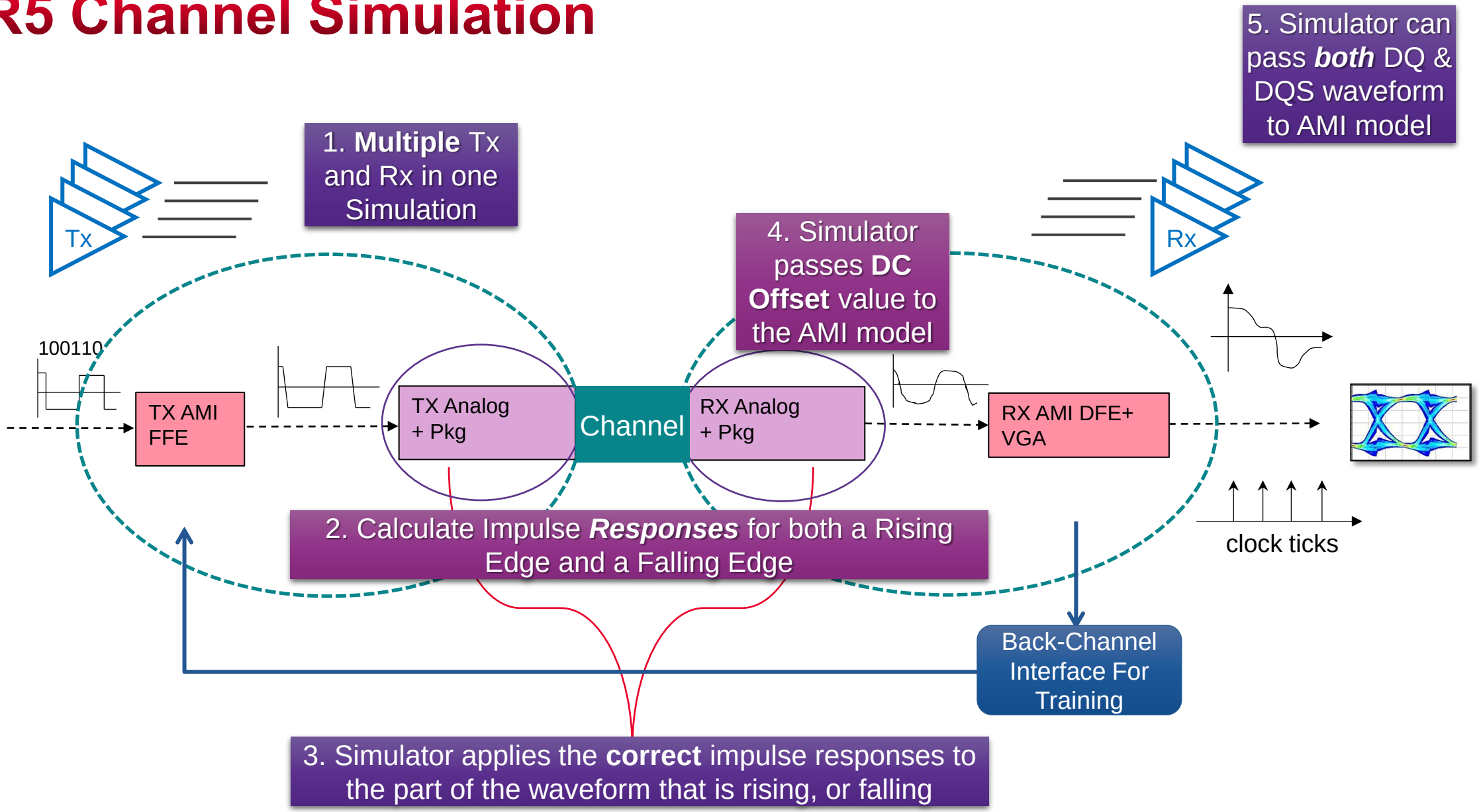
PCB Trace Routing of Victim + Worst Aggressors



With Crosstalk

DDR5 Simulation and Modeling Solutions

DDR5 Channel Simulation



Introducing IBIS AMI for DDR Signals

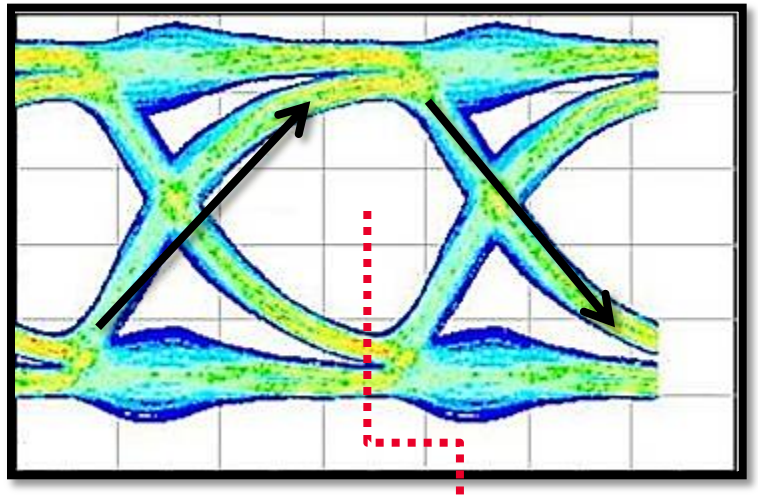
- EQ Necessary for TX: 3 Tap Pre-Emphasis (Feed Forward Equalization)
- EQ Necessary for RX: CTLE/VGA/DFE
- IBIS-AMI offers
  - Portability – One IBIS-AMI mode can run on many EDA tools
  - IP Protection – Digital signal processing behavior is concealed in model DLL/shared object
  - Interoperability - IC Vendor A🡐🡒IC Vendor B (AMI defines a common interface between the vendor model and the EDA channel simulator)
  - Non-linearity – As complex as the model vendor wishes the model to be
  - Performance – Ultra low BER simulations in seconds not days over the traditional SPICE simulation
- AMI has been widely adopted by IC, system and EDA companies for SerDes signals but this is the first application to DDR single-ended signals.

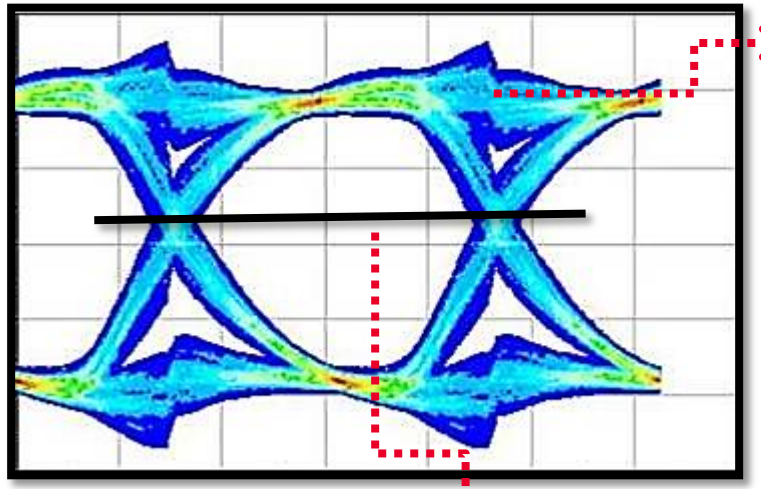
What Do We Need for DDR5 AMI To Work?

Supporting Parallel, single-ended signals with external clocks

Input to DRAM

After Gain & 4 Tap DFE





DFE Clocked by DQS:

- Correlated Jitter on DQ & DQS cancels out
- Uncorrelated Jitter on DQS is transferred to DQ

Single-Ended Signal

Asymmetric Eye:
Rise Time ≠ Fall Time

Asymmetric Eye:
Crossing Points are shifted in the Equalized Eye

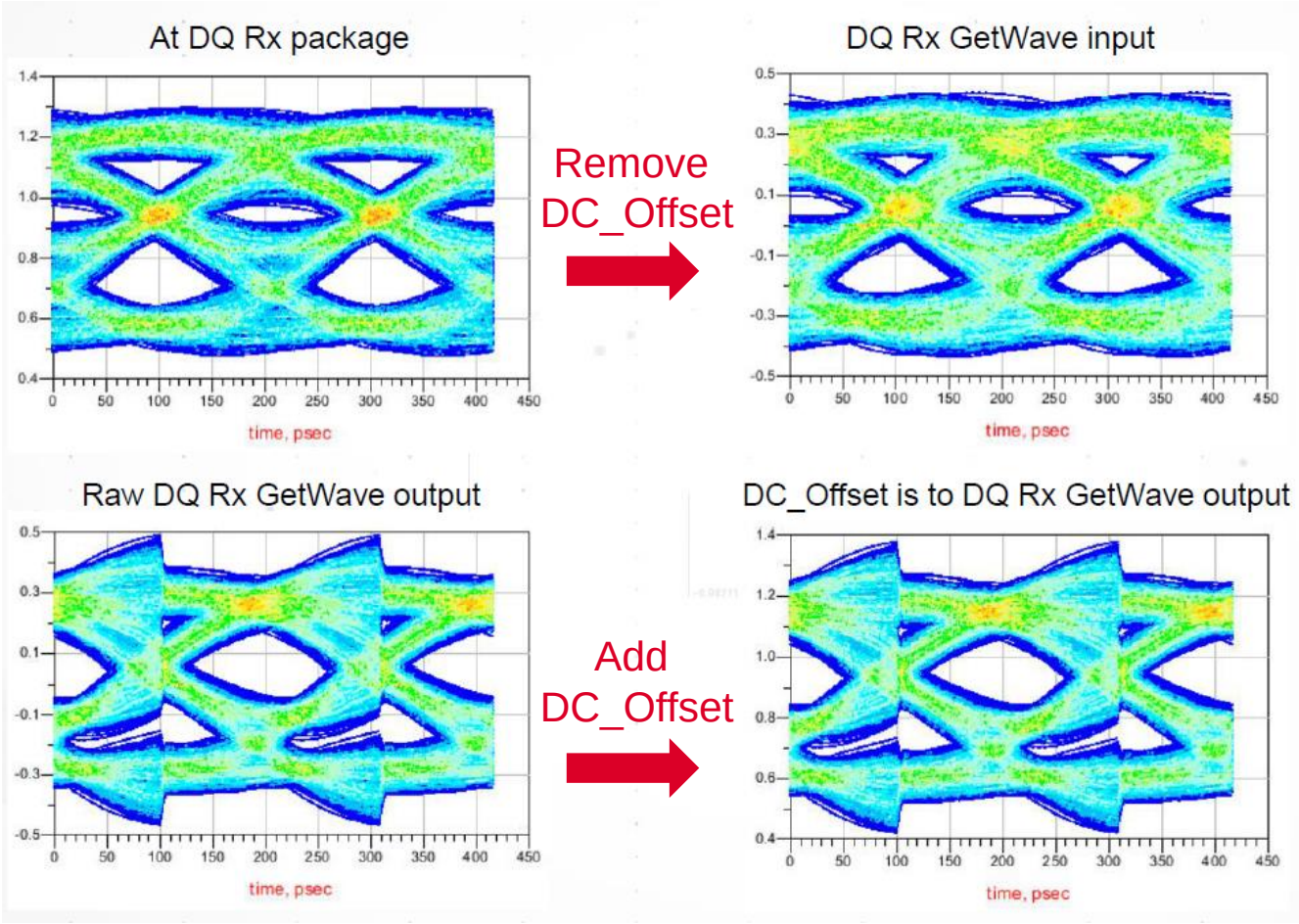
DDR5 AMI Challenges & Solutions

Common Mode in Single-Ended Signal

- Single-Ended (SE) signals
  - Both differential and **common** modes

→ A new reserved parameter **DC_Offset** in BIRD197.7

- SE waveform at Rx DLL Input node = Rx GetWave input + DC_Offset
- DC_Offset value is a constant that is characterized and passed into Rx Init by EDA tool
- Rx GetWave input & output waveforms both center around 0V



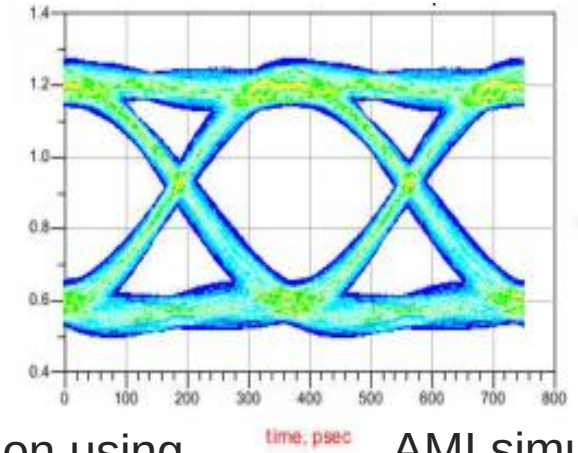
DDR5 AMI Challenges & Solutions

Asymmetric Rise and Fall Edges in Single-Ended Signal

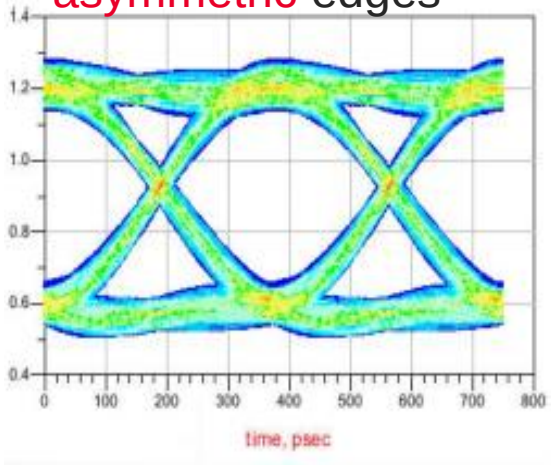
- Single-Ended (SE) signals
  - **Asymmetric** rise and fall edges
  - Simulation using symmetrical edges yields unrealistically symmetrical eye, resulting in inaccurate Vref determination and timing and voltage margin measurements.

→ EDA tool will capture asymmetrical rise and fall edges in waveform calculations.

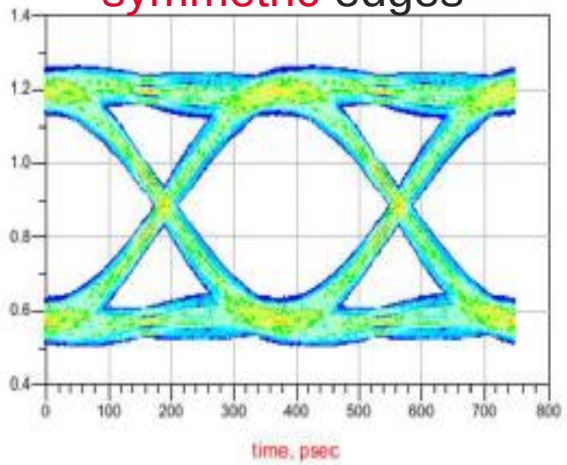
SPICE simulation



AMI simulation using asymmetric edges



AMI simulation using symmetric edges



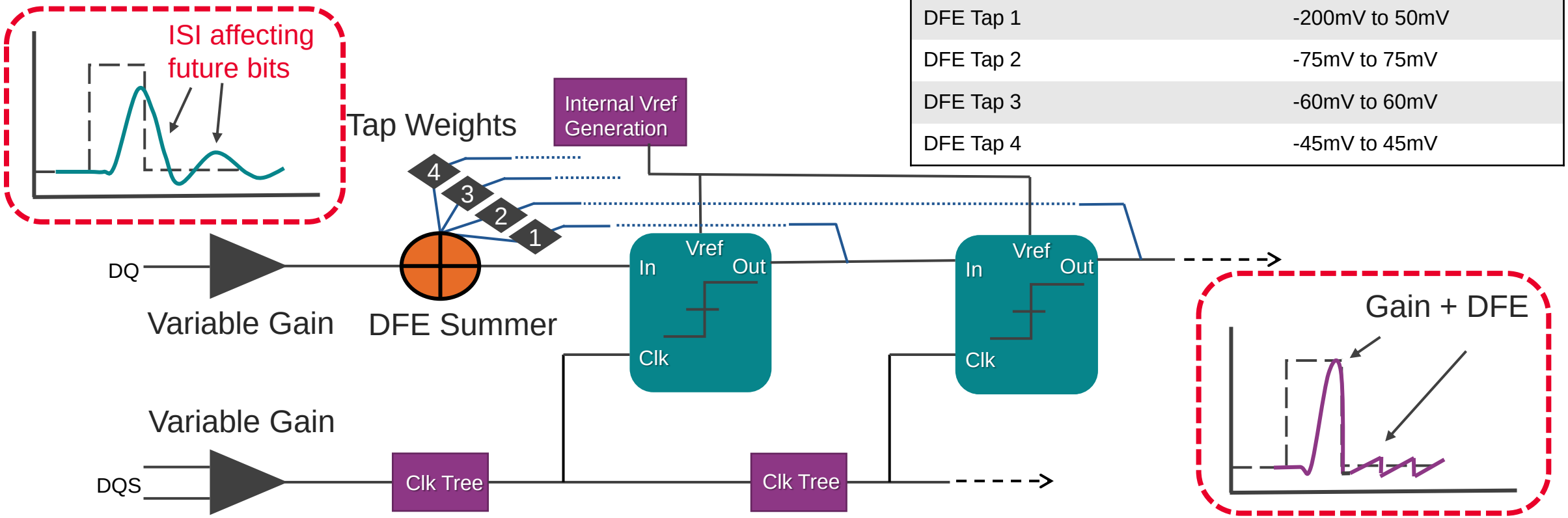
DDR5 AMI Challenges & Solutions

High ISI & Clocking

- Higher data rate results higher ISI

→ 4-Tap **DFE** (Decision Feedback Equalizer)

Mode Register Settings (per DQ)	*All values subject to change*
Variable Gain	-6dB to 6dB
VrefDQ	-3 to +3 Offset steps
DFE Tap 1	-200mV to 50mV
DFE Tap 2	-75mV to 75mV
DFE Tap 3	-60mV to 60mV
DFE Tap 4	-45mV to 45mV



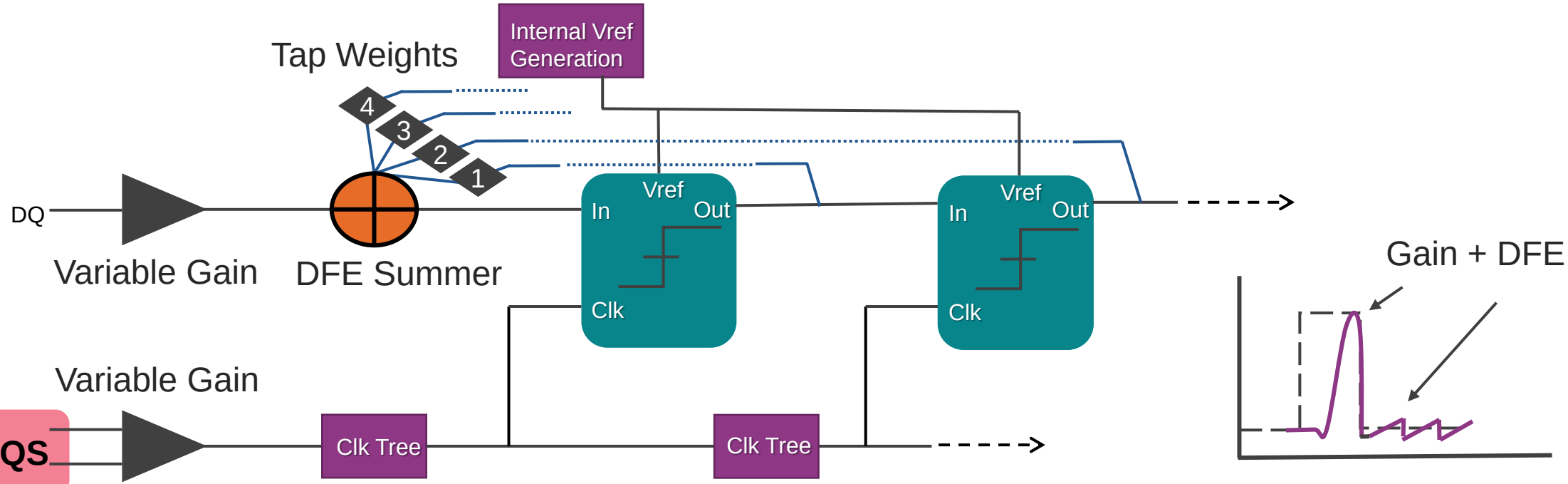
DDR5 AMI Challenges & Solutions

High ISI & Clocking

- No embedded CDR for DFE in DDR DQ Rx.

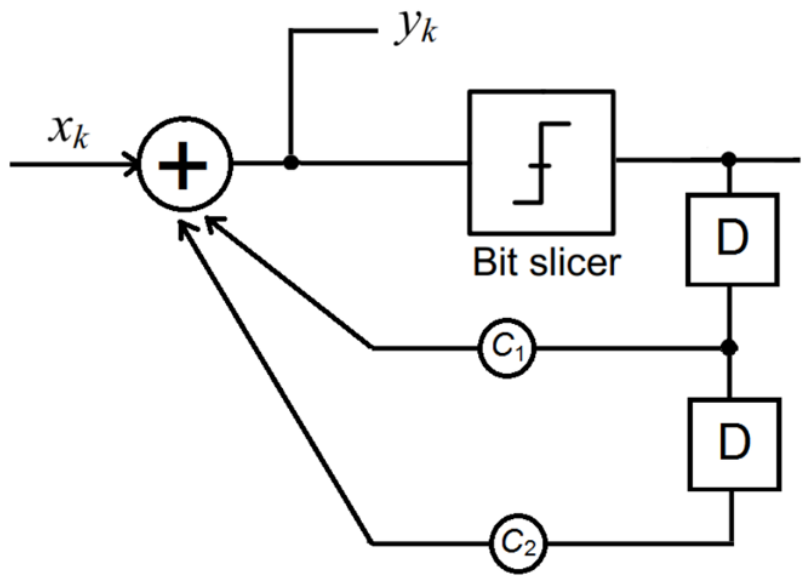
→New parameter **Rx_Use_Clock_Input** in BIRD204

- Output of DQS (DQS Rx AMI_GetWave)



Appendix: Adaptive DFE

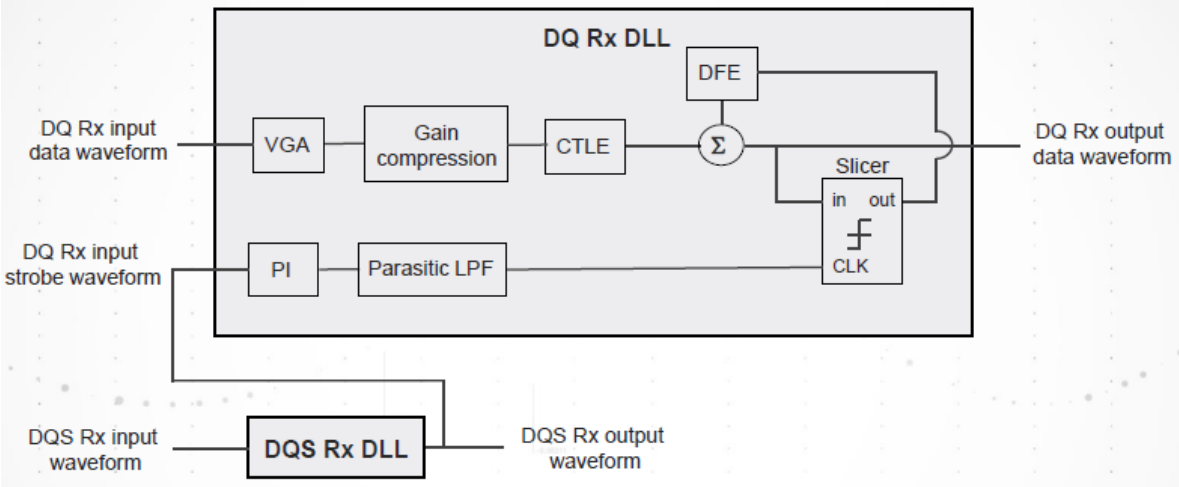
- The action of the DFE is to feed back a weighted sum of past decision to cancel the ISI they cause in the present signaling interval.
  - $y_k = x_k + \sum_{i=1}^{N_{taps}} c_i * slice(y_{k-i})$
- Feedback taps c_i is adapted with adaptive formula:
  - $e = G * y_k - slice(y_k)$
  - $c_i = c_{i-1} - \alpha * e * slice(y_{k-i})$
  - Where
    - y_k is the DFE differential output voltage
    - x_k is the DFE differential input voltage
    - c_i is the DFE feedback coefficient
    - e is the error value between EQ output at clock and output of decision
    - $slice(y_{k-i})$ is the decision function output voltage, it may be BitVoltageAtChannelInput (e.g. ±0.5)
    - k is the sample index in UI
    - G is scaling factor



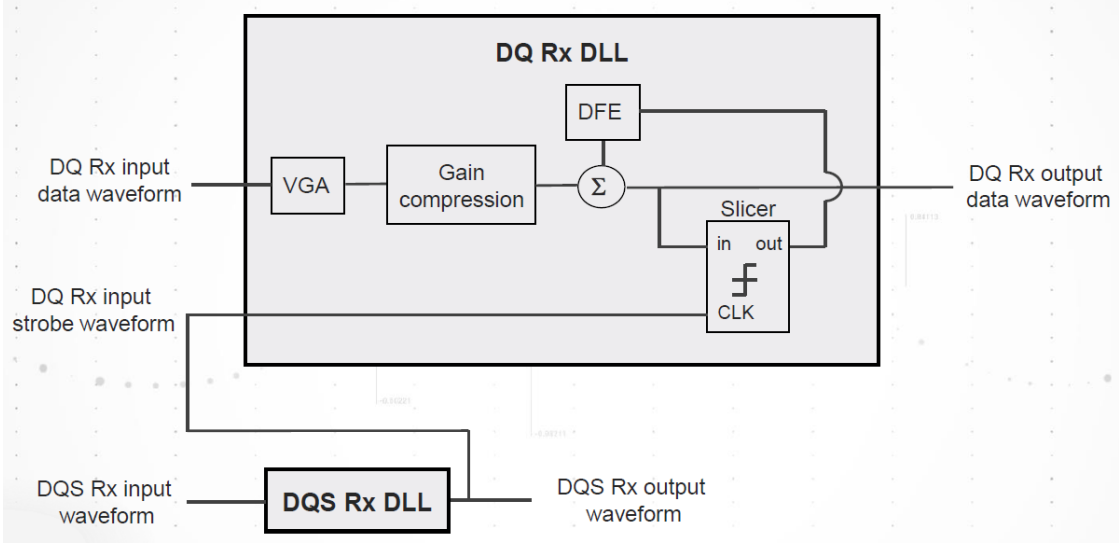
DDR5 AMI Challenges & Solution

High ISI & Clocking

- Controller DQ Rx Model Example
  - VGA, Gain compression, CTLE, adaptive DFE
  - DQS as clock with PI (Phase Interpolator)



- DRAM DQ Rx Model Example
  - VGA, Gain Compression, (CTLE), adaptive DFE
  - DQS as clock

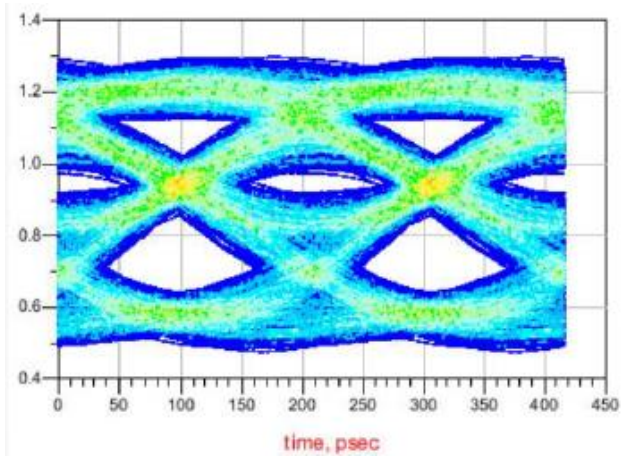


DDR5 AMI Challenges & Solution

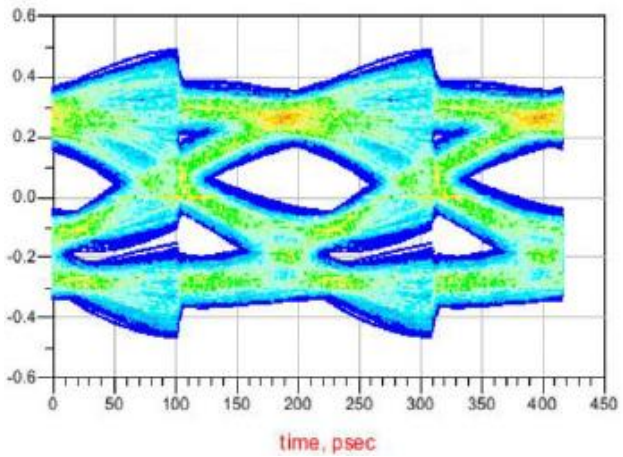
DFE with PI followed DQS

- Controller DQ Rx model can internally train the phase interpolator to adjust data-strobe skew for optimal DFE clocking

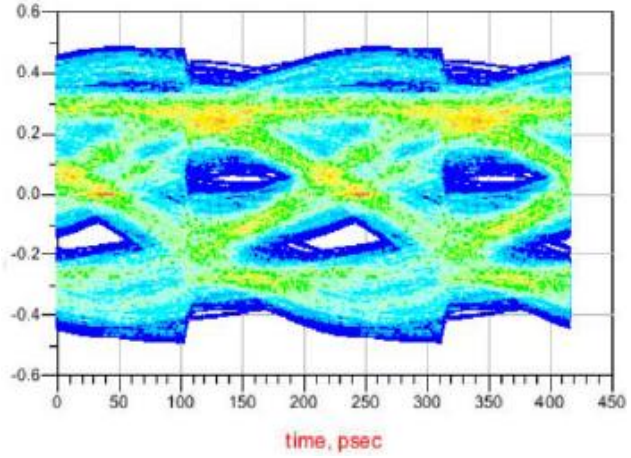
Before Equalization



After Equalization
(with phase interpolator training)



After Equalization
(without phase interpolator training)

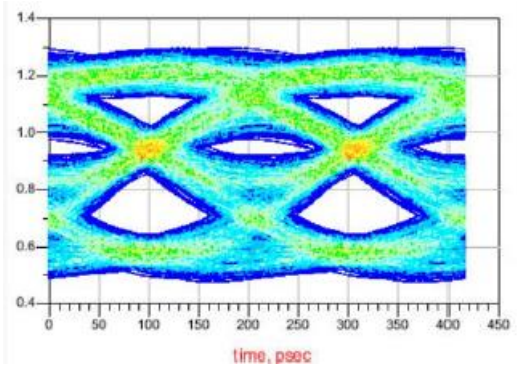


DDR5 AMI Challenges & Solution

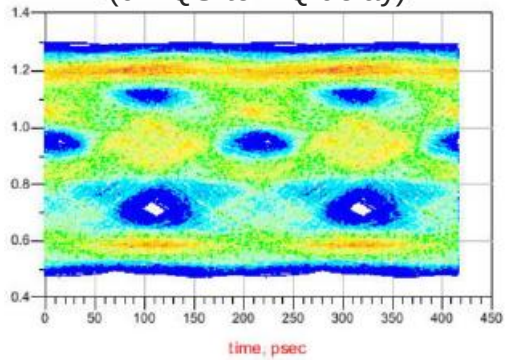
Jitter Tracking and Unmatched IO Rx

- Correlated jitters in DQ & DQS can be tracked in DQ Rx by clock forwading
- Unmatched DQ & DQS Rx are allowed

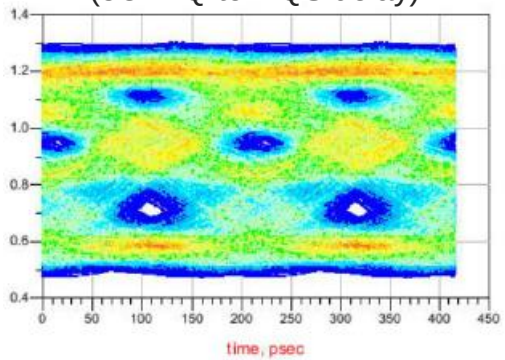
DQ Rx package wo. DQ & DQS Tx SJ



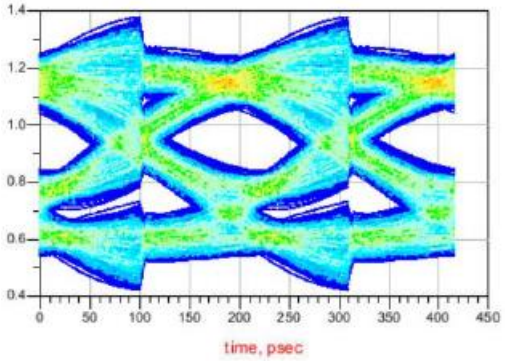
DQ Rx package with DQ & DQS Tx SJ (0 DQS-to-DQ delay)



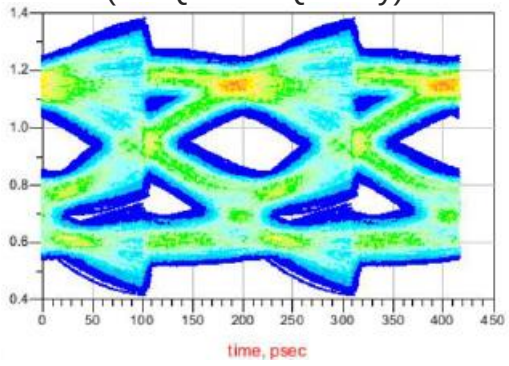
DQ Rx package with. DQ & DQS Tx SJ (5UI DQ-to-DQS delay)



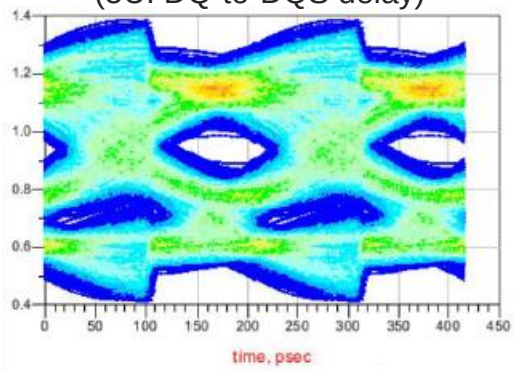
DQ Rx output wo. DQ & DQS Tx SJ



DQ Rx output with DQ & DQS Tx SJ (0 DQS-to-DQ delay)



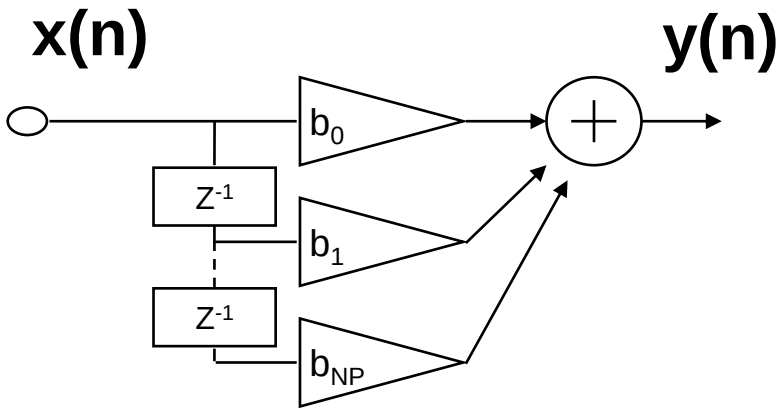
DQ Rx output with. DQ & DQS Tx SJ (5UI DQ-to-DQS delay)



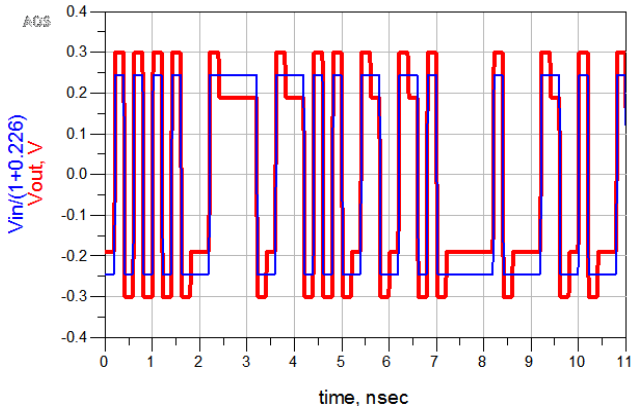
Appendix: Others: TX Equalizer

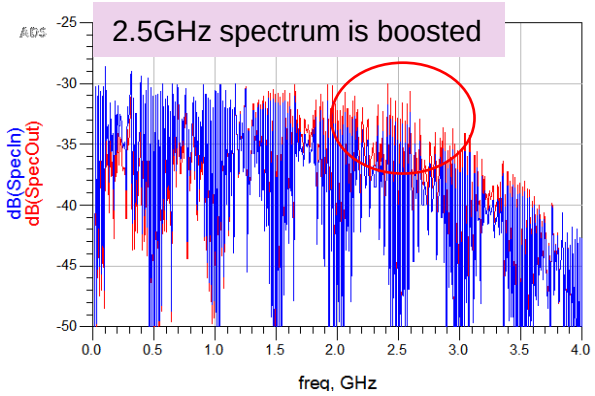
Pre-shoot or De-emphasis

- Boost signal strength around high frequency range
- Can be constructed by a N-tap FIR filter



$$y(n) = \sum_{k=0}^{N_P} b_k x(n-k)$$



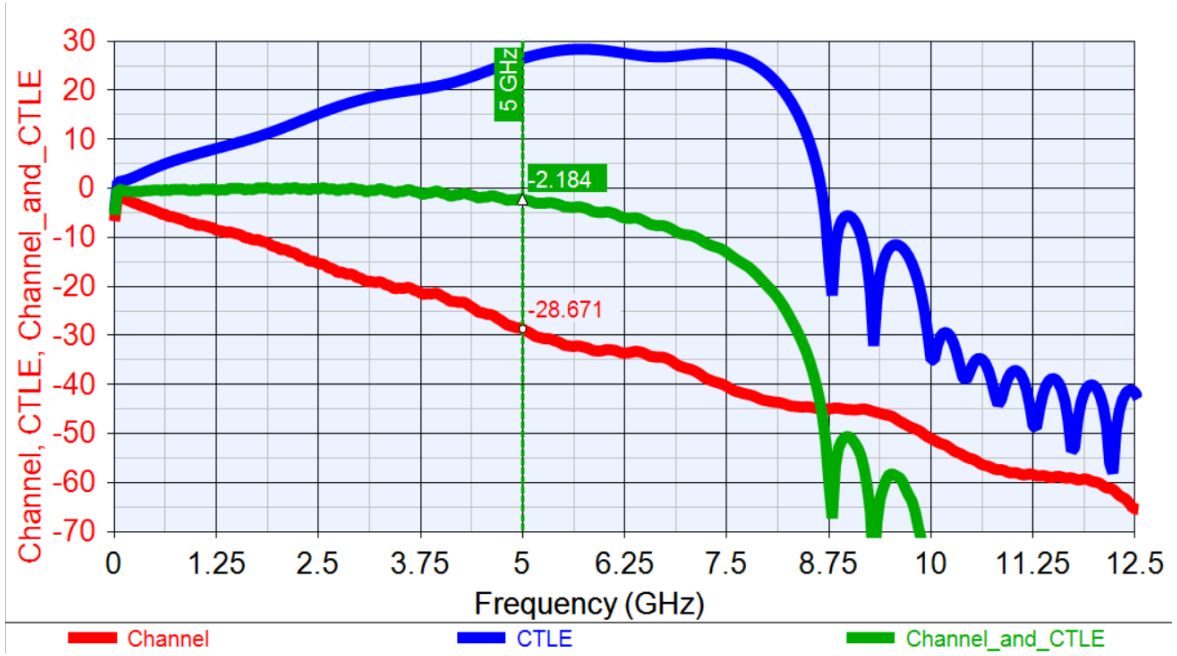


With De-Emphasis
Without De-Emphasis

Appendix: Rx Equalizer – CTLE

CTLE(Continuous Time Linear Equalizer)

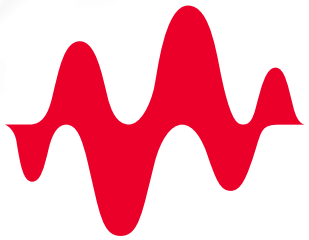
- CTLE is an amplifier with Analog Filter
- CTLE can be modeled by transfer function (Poles/Zeros)



Channel S21
CTLE Frequency Response
Channel + S21

$$H(s) = Apre\frac{(s-\omega_{z1})(s-\omega_{z2})\ldots}{(s-\omega_{p1})(s-\omega_{p2})(s-\omega_{p3})\ldots}$$

Zeros in rad/s = $[\omega_{z1}, \omega_{z1}, \ldots]$
Poles in rad/s = $[\omega_{p1}, \omega_{p2}, \omega_{p3} \ldots]$
Pre-Factor: A_{pre}



KEYSIGHT
TECHNOLOGIES