AMD

Inside an IBIS provider

Virtual Asian IBIS Summit (Japan)
November 12, 2021

Tadashi Arai / SMTS, Systems Design Engineer, AMD Japan

A Long Time Ago…

An IBIS user from early 90's

- SPICE simulation using I-V characteristics (before IBIS)
- IBIS from a promoting company – only

Extended IBIS capability

- IBIS from multiple IC vendors
- IBIS for complex buffer model
- PCB CAD extraction

Frustration against IBIS provider = IC vendor companies

- IBIS availability
- Accuracy / Quality – too many warnings, errors, unexpected behaviors, etc.
- Simple model for complex buffer – differential buffer, multi-stage, equalizer, package parasitic
- Power models

Case Study: A Semi-Custom Program

Customer-branded IC product

Mixture of AMD IPs, 3rd party IPs and customer IPs

AMD owns back-end design: floorplan, layout, package and MFG data to Fab

The customer owns schematic design, etc., also PCB design support

The customer requested IBIS as a part of provided materials

- Requested IBIS by tape-out – 6 month from project kick-off

My response to request: "*OK, no problem*"

- AMD has all required information – SPICE models at least
- AMD has capability of IBIS provider – designers might have knowledge and experience
- AMD already provided IBIS for the roadmap products – in the past. Only limited IBIS models are provided recently

Conclusion: My prediction was too optimistic…

I/O Buffer 1: Industry Standard High-Speed Serial I/O

Industry standard high-speed serial I/O interfaces

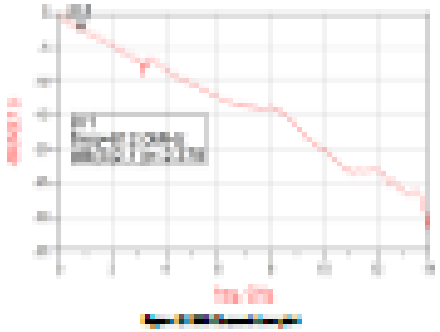
IP from a major 3rd party IP vendor

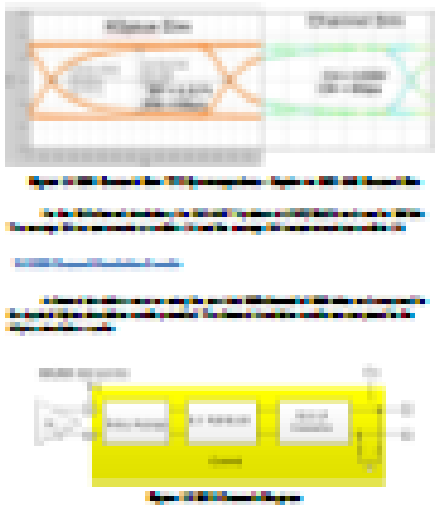
No request: IBIS-AMI model already included in customer IP Package

Test: Sanity check only (enough)

- Detailed report was attached with the package

Result: Good





I/O Buffer 2: Legacy Video-Out Interface

Legacy interface for video output interface

IP from a specialized 3rd party IP vendor

Response to request: "*IBIS is not ready. No experience to provide IBIS.*"

1st Attempt: Provided a SPICE macro model

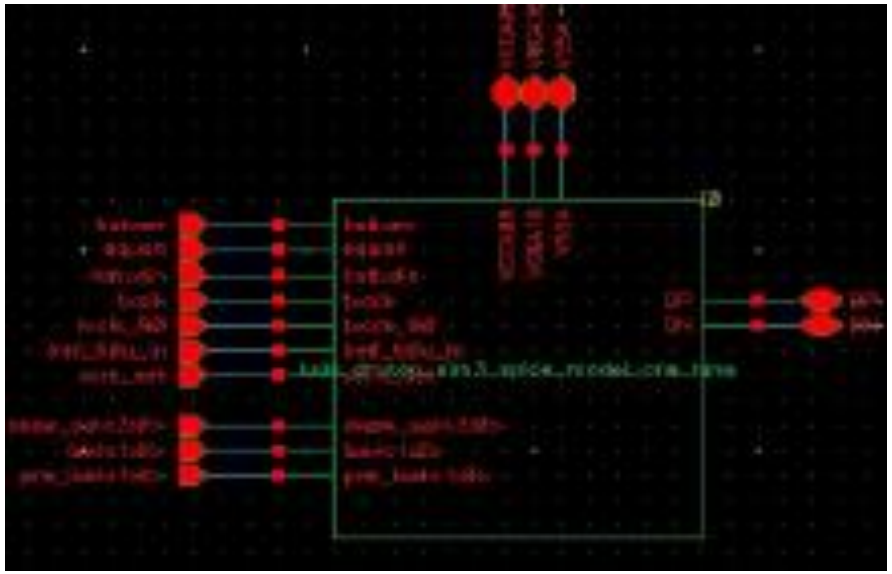
- ➔ Request for model usage; signal functions, conditions, etc. – No response
- ➔ Unable to generate IBIS from this SPICE model

2nd Attempt: Provided an IBIS

- ➔ Differential buffer – Single-ended model

Test: No sink device model – termination only

Result: Quality not validated



I/O Buffer 3: Memory Interface

High bandwidth JEDEC standard DRAM I/O interface

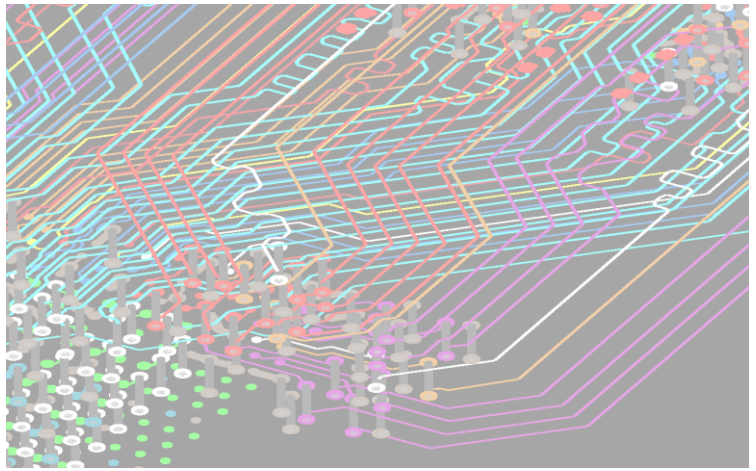
In-house IP

Response to request: "*IBIS was ready, will provide.*"

➔ Complex high-speed buffer (variable drive strength, DFE, CTLE, etc.) - Simple IBIS

Test: Functionality check (loop back – memory device IBIS unavailable)

Result: Questionable quality – Difficult to validate, but no problem (AMD owned PCB layout design)



I/O Buffer 4: Clock Input

Input pad for the reference clock

In-house IP

Response to request: "*OK, will provide SPICE model.*"

1st Attempt: provided a "SPICE model" (356MB text file)

- ➔ DSPF (Detailed Standard Parasitic Format) – Unable to understand the structure
- ➔ No clamp characteristics found

2nd Attempt: provided clamp I-V curves

Work: Formatted I-V curves into IBIS

Test: Sanity check (ibischk) only – no driver model

Result: Never validated

```
*|DIVIDER /
*|DELIMITER :
**FORMAT SPF
*


** COMMENTS

** GLOBAL_TEMPERATURE 25
** TCAD_GRD_FILE /proj/dk/technolog
**   TCAD_TIME_STAMP Sun Feb 14 03:
**   TCADGRD_VERSION 79
** COMMENTS_FILE /proj/socckt_clk_g
**   *STARRC_RECOMMENDED_VERSION
**   *Rapid3D_RECOMMENDED_VERSION
**   *StarRC template for 14LPP
**   ******************************
**   * Star-RCXT command file sampl
**   ******************************
**   EXTEND_VIA_CONNECTION: YES
**   *ICV_RUNSET_REPORT_FILE:
**   *ICV_ANNOTATION_FILE:
**   CALIBRE_RUNSET: /proj/socckt c
```

I/O Buffer 5: Slow Standard Serial I/O

Slow speed industry standard serial I/O interface

In-house IP

Response to request: "*OK, will provide IBIS*"

1st Attempt: the provided files were SPICE and SPF

➔ Tried to generate IBIS using s2ibis, but no success

2nd Attempt: provided V-T and I-V curves

Work: Formatted V-T and I-V curves into IBIS

Test: Functionality check (loop back)

Result: Good

I/O Buffer 6: General Purpose I/O

Slow speed general purpose I/O buffer

In-house IP

Response to request: "*OK, will provide information.*"

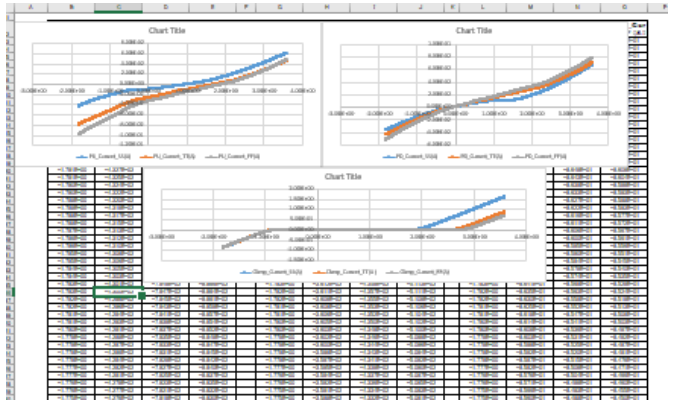
- ➔ I-V curves: 3 separate series V-I(typ), V-I(min), V-I(max) in different V ticks.
- ➔ V-t curves
- ➔ 2 types in drive strength

Work: Formatting into IBIS

- ➔ Consolidated I-V curves into "V, I(typ), I(min), I(max)" – very difficult
- ➔ Buffer type variation using **[Model Selector]**

Test: Functionality check (loop back)

Result: Good



Package Model

972 balls Organic FC-BGA package

In-house design – tight communication with team on various topics

Response to request: "*Yes, will provide a package model*"

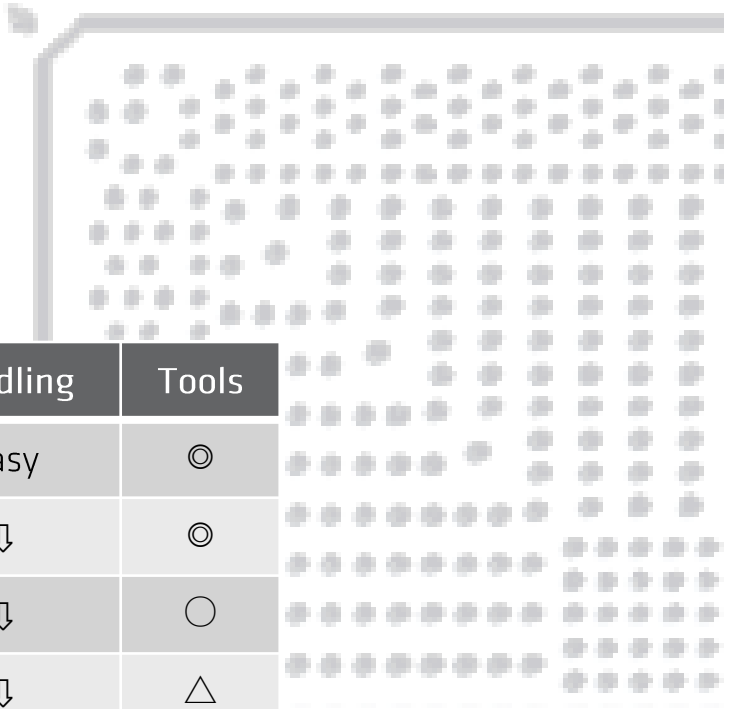
1st Attempt: S-parameter for each signal group

➔ Large, difficult to handle (max "s44p")

2nd Attempt: Discussed extracting RLC package models

➔ Package team won't do that for many reasons

➔ Asked if the customer can accept S-parameter – confirmed OK

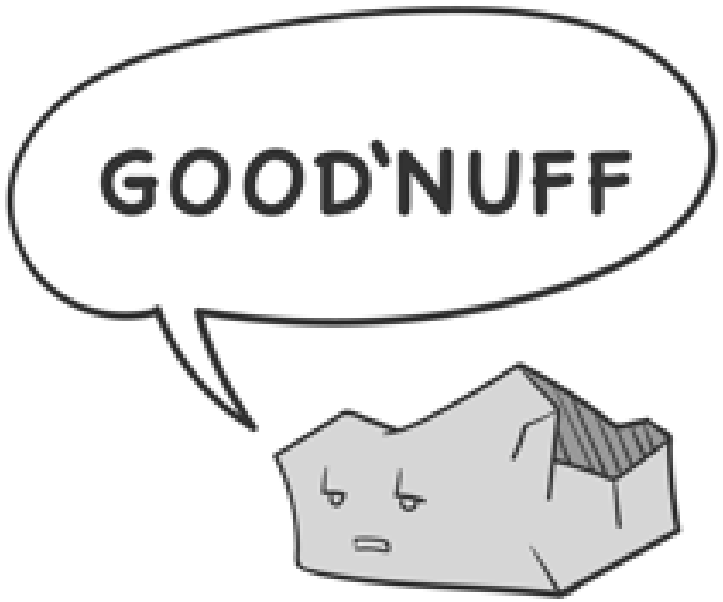


Build	Package Model	Accuracy	Handling	Tools
Difficult	Component **[Package]** RLC	Low	Easy	◎
⇧	**[Pin]** Package RLC	⇩	⇩	◎
⇧	Detailed package model: RLC ladder	⇩	⇩	○
⇧	Detailed package model: Matrix	⇩	⇩	△
Easy	S-parameter	High	Difficult	△

The Customer Response

- No additional question, request and discussion was made from the customer so far.

- Assumptions:
  - The customer was satisfied with the provided IBIS (?)
  - The customer can support questions from the customer's customer by themselves (?)
  - IBIS is not so much important…(?) ☹



Power-Aware Model

Power-aware IBIS was requested later – post Si phase, development already finished

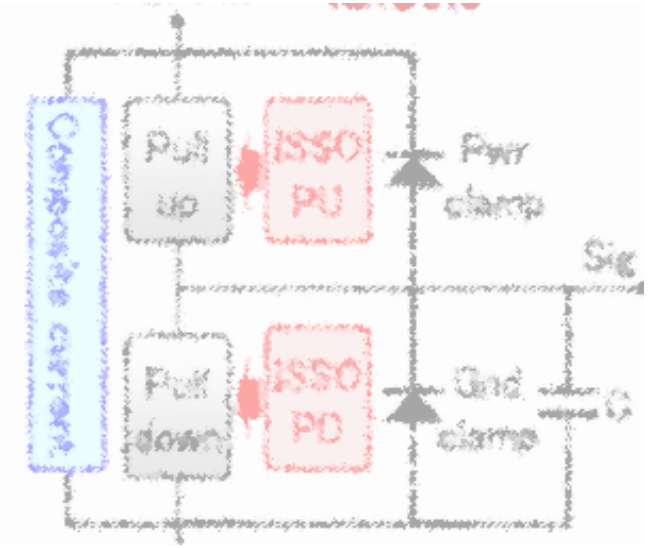
Response to request

- Feasibility unknown - No experience
- Additional cost – Non planned activity needs additional resources
- "*Will start assessment if customer will pay extra*" with a quote

Result: The customer gave up the request

Discussion (internal)

- Maybe possible to generate since we have power models
- Unknown who can generate it. Silicon designer? Power designer?



IBIS Provider Nice-to-Have

- Resource planning
  - Cost, workload, schedule, outsourcing, …
- Designer encouragement
  - “SPICE is enough”
  - “Don’t know how-to”
  - “Not my business”
  - Negotiation with external vendors
- Dedicated team
  - Wide understandings from silicon to board design
  - From planning to sustaining support

Team “IBIS” Workflow

Planning
- Target IBIS complexity / Resource workload for developers / Budget / Outsourcing

Data Collection
- SPICE models / Buffer characteristics
- Package characteristics
- Power models…

Building
- SPICE to IBIS
- Data formatting
- Compile
- Extracting parasitic…

Qualification

Publishing

Maintenance and Support

Qualification

Test Items

- Check if IBIS file loaded into EDA tool without error
- Check if each model shows ‘reasonable’ waveforms in operating range

Test bench

- Target devices
- Terminations
- Reference channels

Corner case

- Within / outside of operating range
- Out of design recommendations

SPICE model correlation

- Pre-Si

Silicon correlation

- Post-Si, test coupon / evaluation kit

Package correlation

Conclusion

IBIS users, please

Understand IBIS is not easily, automatically generated in provider companies

Push harder on provider companies to create better IBIS models

IBIS providers, please

Establish IBIS provider workflow in the company / organization

IBIS committee, please

Promote a standard workflow for providers to help establish a dedicated team in the company


AMD