Virtual Asian IBIS Summit (Tokyo)

DDR memory system simulation method

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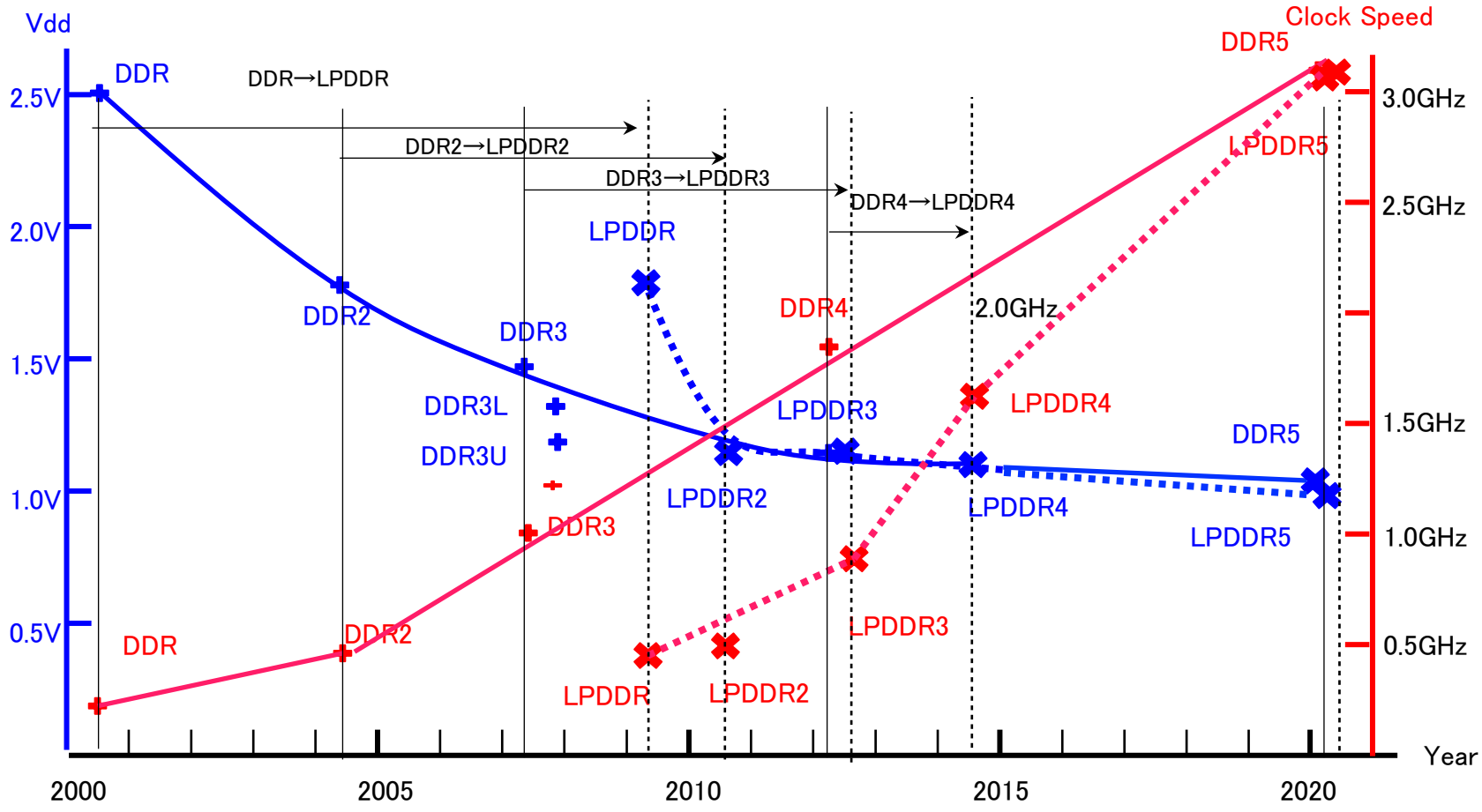
OVERVIEW

- (LP)DDR Memory has 5 generations
- Every generation is x2 speed and lower Vdd from previous
- Higher speed makes it difficult to design PCB system
- New generation DDR implements new features to make PCB design easier
- New features require changes to simulation methods

(LP)DDR Speed/Vdd

- JEDEC



(LP)DDR Features on Generation

- JEDEC

Item		DDR	LPDDR	DDR2	LPDDR2	DDR3	LPDDR3	DDR4	LPDDR4	DDR5	LPDDR5
Rerease		2000/06	2008	2004	2010	2007	2012/5	2012/9	2014/8	2020/7	2019/7
Transfer Speed(gBPS)		200～400M	200～400M	400～800	400～1066	800～2066	800～1600	1600～3200	1600～3200	3200～6400	3200～6400
Clock(Hz)		100～200M	100～200M	200～400M	200～533M	400～1033	400～800	800～1600	800～1600	1600～3200	1600～3200
Vdd/Vddq		2.5	1.8	1.8	1.2	1.5	1.2	1.2	1.1/0.6	1.1	1.05/0.5
Output Impedance		Full/Half	Full/Half	Full/Reduce	34/48/60/80/120	30/40	34/48	34/40	34/40	*	*
ODT	Value	—	—	50/75/150/OFF	—	20/30/40/60/120/OFF	34.3/40/60/80/120/OFF	34/40/48/60/80/120/240/OFF	40/48/60/80/120/240/OFF	*	*
	Pull	—	—	Vdd/2	—	Vdd/2		Vdd	Vdd	Vdd	Vdd
Training		—	—	—	—	—	—	○	○	○	○
Equalizer/Emphasys		—	—	—	—	—	—	—	—	○	○
Strage		16Mb～256Mb	64Mb～2Gb	128Mb～4Gb	64Mb～32Gb	512Mb～8Gb	1Gb～32Gb	2Gb～16Gb	4Gb ～32Gb	8Gb～64Gb	4Gb ～32Gb

DDR vs. LPDDR

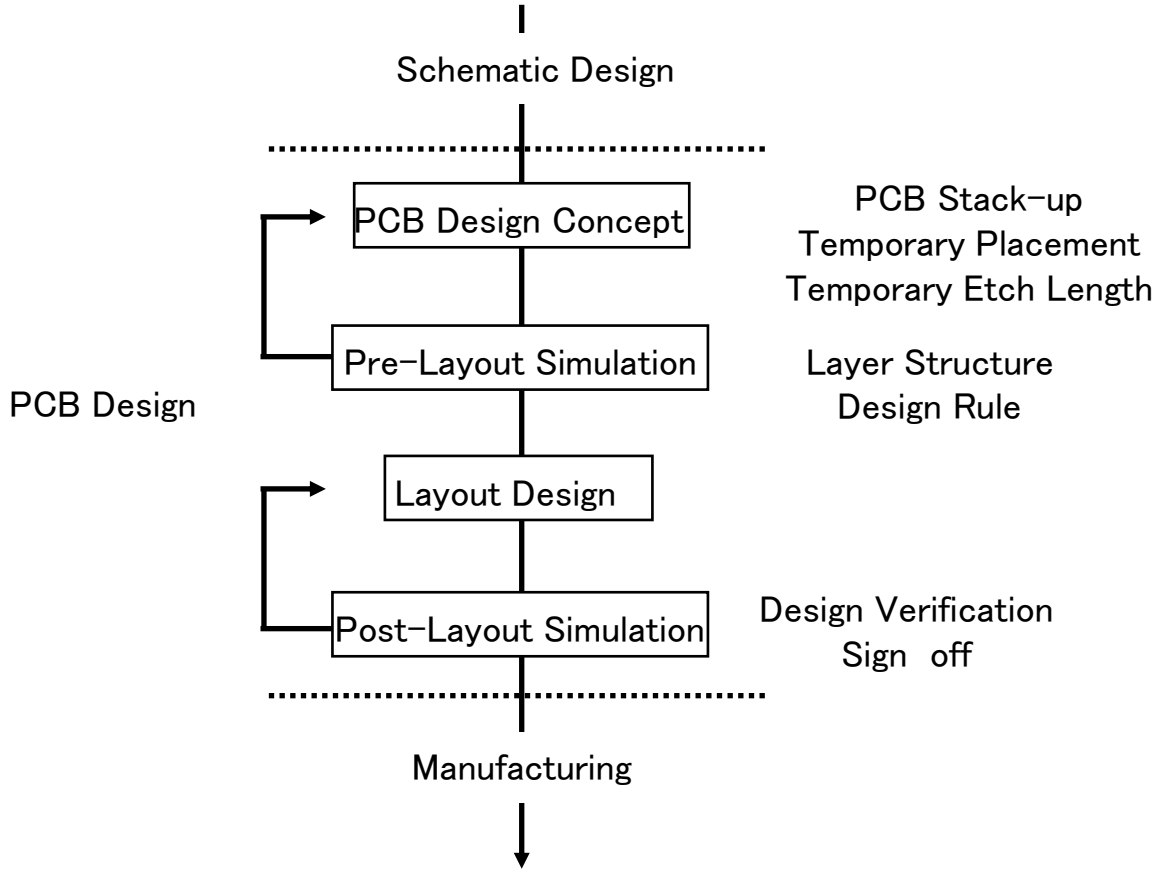
- DDR
  - Application: HPC, PC, Built-in System
  - High-end Performance: Speed, Memory Size
  - Connect multiple memories
  - BGA
    - DIMM/SIMM Module
- LPDDR
  - Application: Mobile device
  - Low Power First, next size then speed, memory size
  - Connect one or a few memories
    - POP (Package-on-Package), Flip Chip, BGA

DDR Technologies

- DDR
  - Lower Power
    - Green Energy
      - Data Center, Super Computer
- LPDDR
  - Higher Speed, More Memory Size
    - High Performance Mobile Device
      - Smart Phone, Mobile Game, 5G
- DDR4/LPDDR4
- DDR5/LPDDR5

DDR~DDR3 System Simulation

- Basic Simulation Flow



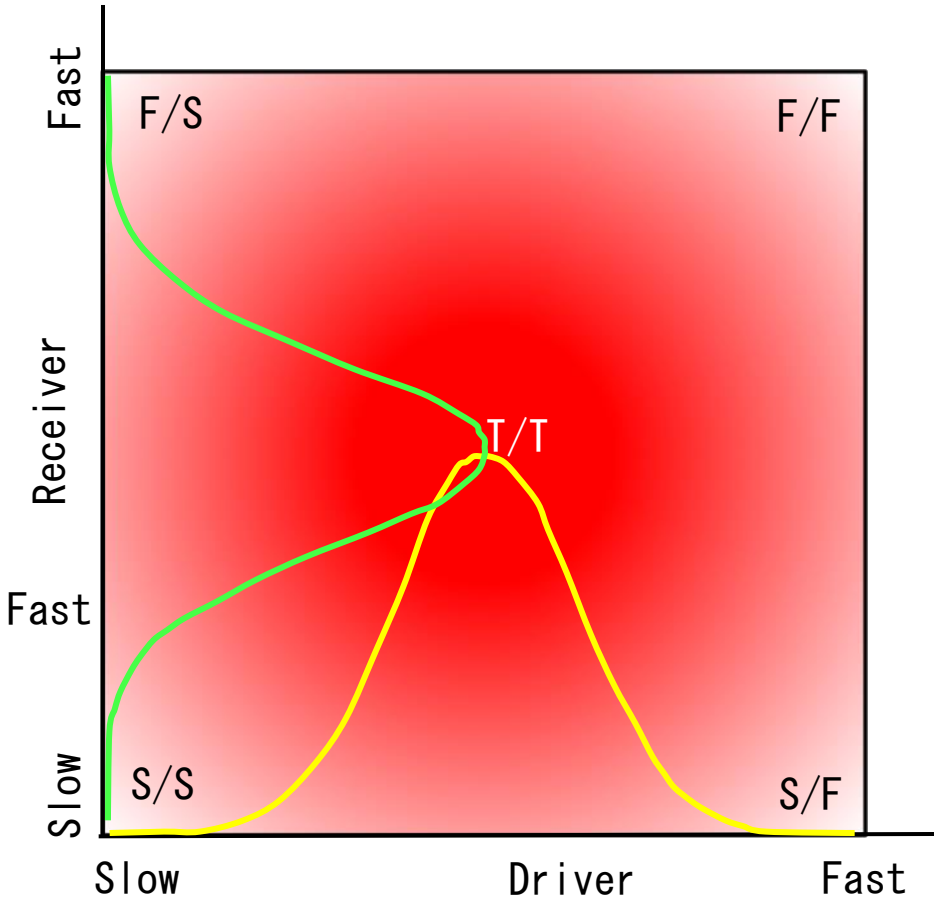
DDR～DDR3

- Features for PCB Design
  - Multi-Driver Strength
  - Multi-Value ODT (DDR2)
  - Fly-by (DDR3)
- Considerations
  - Typical/Worst
  - Derating

Tolerance of IC Characteristics

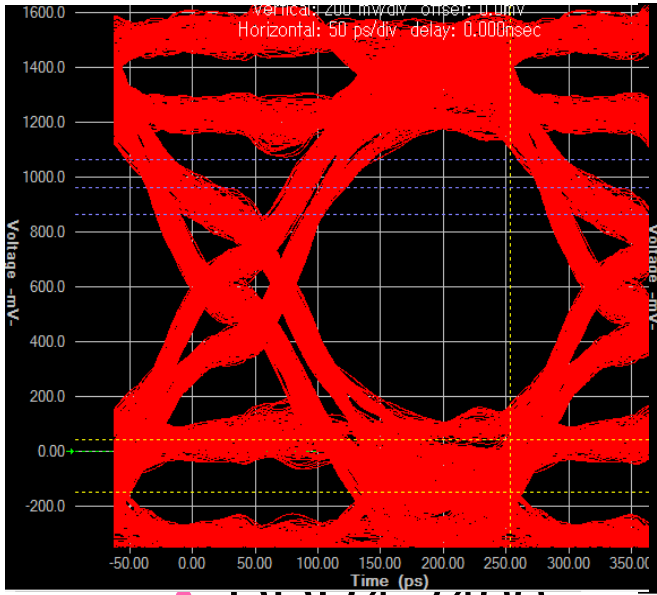
- Drive: Slow - Fast
- Receiver: Slow - Fast

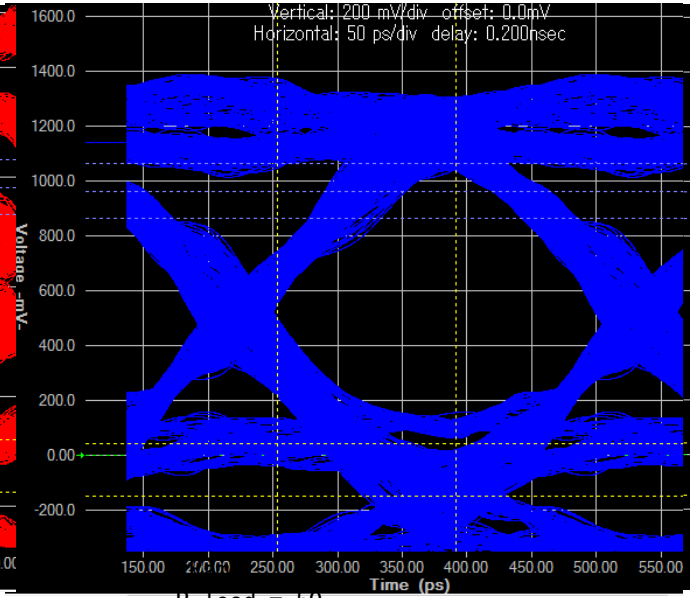
- IO Model
  - Fast/Typical/Slow
  - Driver: Output Impedance
    Ramp
  - Receiver: Threshold Voltage
- C Comp, Package L/C/R
- Vcc Voltage
  - Vtyp +/- 5~10%
- IC Temperature

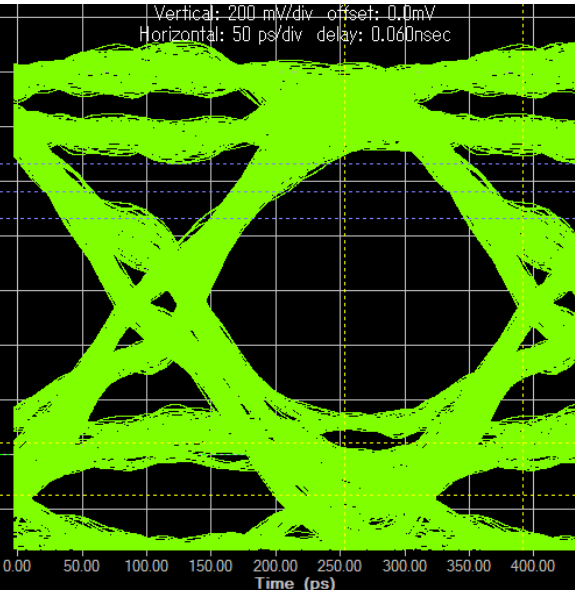


Typ vs. Corner

- Fast
- Typ
- Slow







- DDR4 2400
  - Driver: DQ
  - Receiver: DQ

```
R_load = 50
|        typ                    min                    max
dV/dt_r 4.1235E-01/6.4489E-11   3.8046E-01/8.4106E-11   4.4653E-01/5.2562E-11
dV/dt_f 4.5987E-01/6.2372E-11   4.3947E-01/7.9203E-11   4.6741E-01/4.9982E-11
|*************************************************************************
[Falling Waveform]
V_fixture = 1.2V
V_fixture_min = 1.14V
V_fixture_max = 1.26V
R_fixture = 500hm
C_fixture = 0F
|   Time              V(typ)              V(min)              V(max)
    0.00000000E+00    1.19999848E+00      1.13999700E+00      1.25999947E+00
    5.00000000E-12    1.19999849E+00      1.13999700E+00      1.25999948E+00
    1.00000000E-11    1.19999849E+00      1.13999700E+00      1.25999948E+00
```

Derating

- Timing Specification
  - Reference: Threshold Voltage
    - Timing differs based on Slew-Rate
  - Standard is the value of 1v/ns

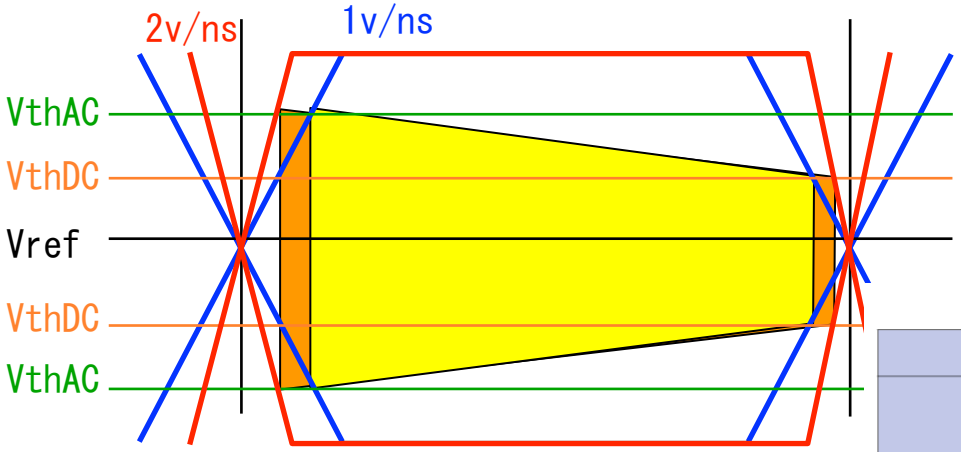
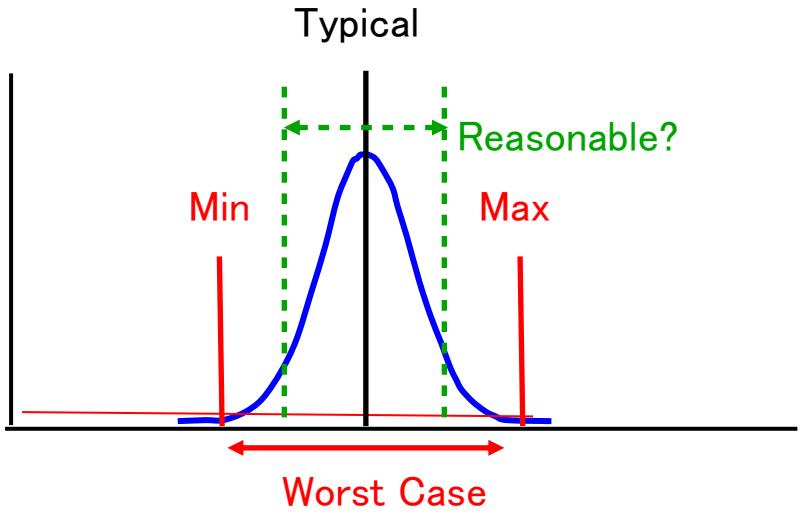


Table 69 — Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based

ΔtIS, ΔtIH derating in [ps] AC/DC based AC175 Threshold -> VIH(ac)=VREF(dc)+175mV, VIL(ac)=VREF(dc)-175mV																	
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

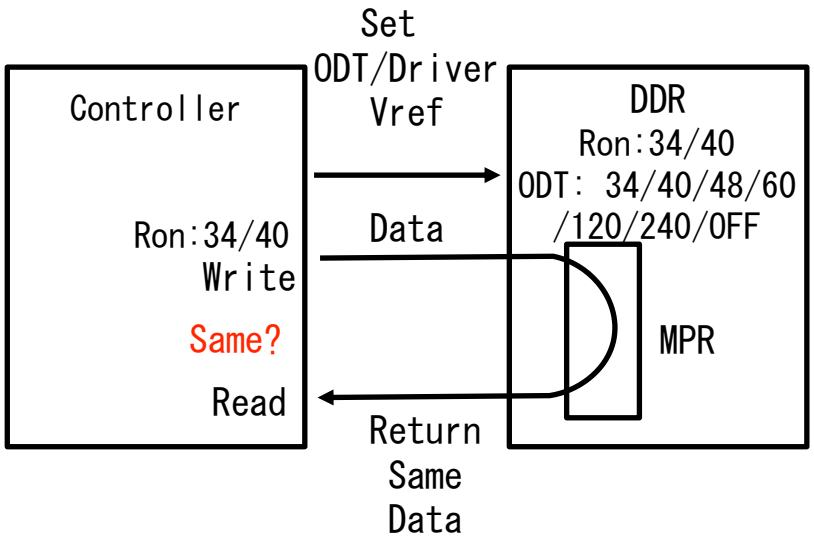
DDR3 System Simulation

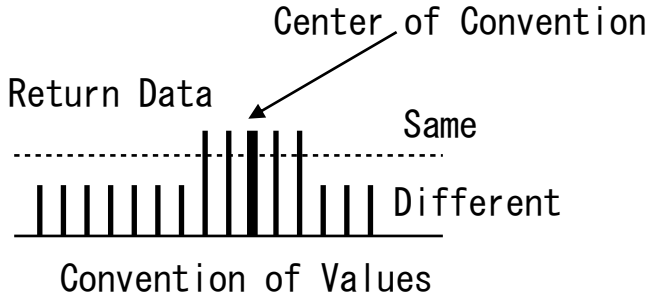
- IBIS Model
  - Timing Simulation
    - Bus Simulation (Crosstalk)
      - 8 Bit Parallel Signals
      - PRBS
    - Power Aware
    - Eye Pattern
      - Derating
  - Worst Case/Typical Case
    - Margin/Yield Rate



DDR4/LPDDR4

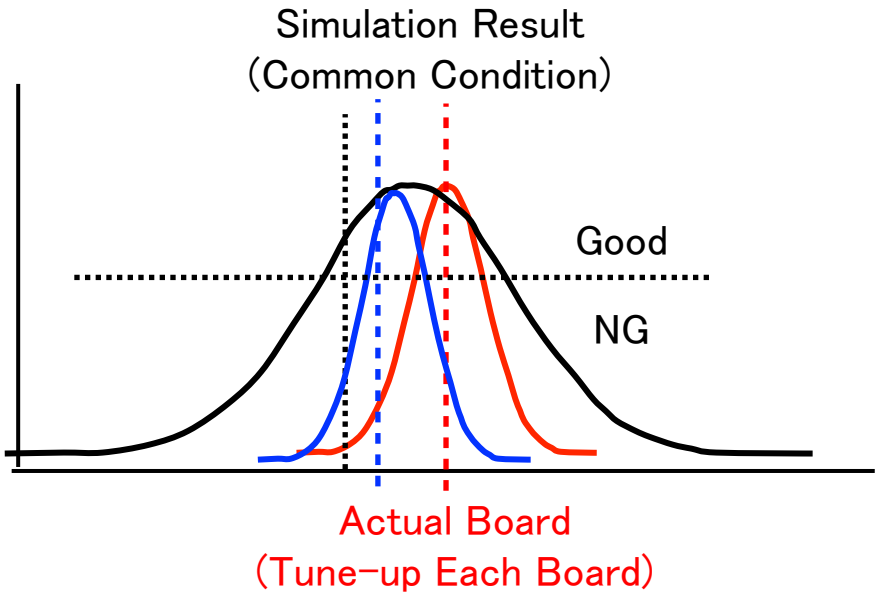
- New Features
  - DQ Vref Training/ZQ calibration
  - Support Eye Mask
    - No more Derating





DDR4/LPDDR4 System Simulation

- IBIS Model
  - Timing Simulation
    - Bus Simulation (Crosstalk)
      - 8 Bit Parallel Signals
      - PRBS
    - Power Aware
    - Eye Mask
      - No More Derating
  - Best Case Analysis
    - Any One Case is Good, Real Should be Better
- IBIS-AMI (Idea)
  - Auto Model Selector
  - Crosstalk Analysis, SSN Analysis



DDR5/LPDDR5

- New Features
  - Analog Driver/Receiver
    - Emphasis
    - Equalizer
      - Feature of PCI Express/High Speed Serial
  - Separate Clock/DQ Write/DQ Read
    - CMD/Address is Slower than DQ

DDR5 Simulation

- IBIS-AMI
  - Emphasis, Equalization: IBIS Model Supports Driver/Receiver
  - Crosstalk Analysis?
  - SSN Effect?

Reference

- “Is Typ. Analysis Enough? What Is Corner Condition?”
  S.Maeda, 2016 Asian IBIS Summit Tokyo