Expectations for IBIS 7.1

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(Previously presented August 17, 2021, by Michael Mirmak, with updates)

Agenda

- History of IBIS 7.1 Development
- Major and Minor Features
  - Complex C_comp Modeling
  - On-die Power Distribution Networks
  - EMD: Electrical Module Descriptions
  - Other Major Changes
- What Comes Next

IBIS 7.1 Development

- Editorial Task Group re-convened February 26, 2021, to assemble IBIS 7.1
  - Weekly meetings Wednesday, 8 AM US Pacific time
- Technical content closed with 13 BIRDs approved for inclusion on July 16
- Two additional BIRDs written by Editorial task group and approved by Open Forum votes on October 8 and 29, 2021
- Editorial work completed on October 27, 2021, and draft IBIS 7.1 document released for review
- Draft introduced at October 29, 2021, Open Forum meeting
- IBIS 7.1 draft available at https://ibis.org/ver7.1_wip

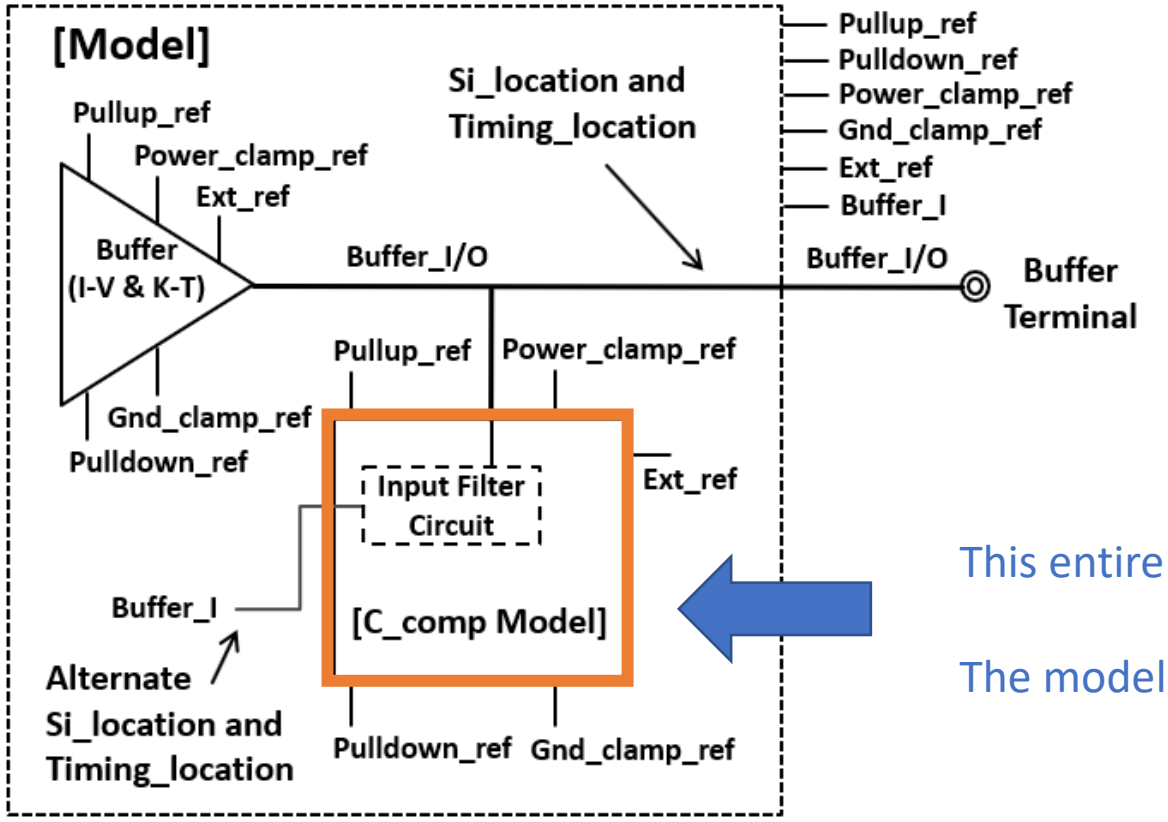
Major and Minor Features of 7.1

- BIRD195.1: Enabling [Rgnd] and [Rpower] Keywords for Input Models
- BIRD197.7: New AMI Reserved Parameter DC_Offset
- BIRD198.3: Keyword Additions for On-Die PDN (Power Distribution Network) Modeling
- BIRD199: Fix Rx_Receiver_Sensitivity Inconsistencies
- BIRD200: C_comp Model Using IBIS-ISS or Touchstone
- BIRD202.3: Electrical Descriptions of Modules
- BIRD203: Submodel Clarification
- BIRD205: New AMI Reserved Parameter for Sampling Position in AMI_Init Flow
- BIRD206: Clarification of text “transition time”
- BIRD207: New AMI Reserved Parameters Component_Name and Signal_Name
- BIRD208: Clock-Data Pin Relationship Keyword
- BIRD209: Make Clock Times Output Required for Clock Executable Models
- BIRD212: Clarification of PAM4_UpperThreshold, PAM4_CenterThreshold, PAM4_LowerThreshold
- BIRD214: Change “bit_time” to “symbol_time”
- BIRD215: Back-channel Statistical Optimization Editorial Update

Individual changes documented at https://ibis.org/birds/

Complex C_comp Modeling

- Modeling impedance using complex frequency- or time-dependent networks rather than single capacitors

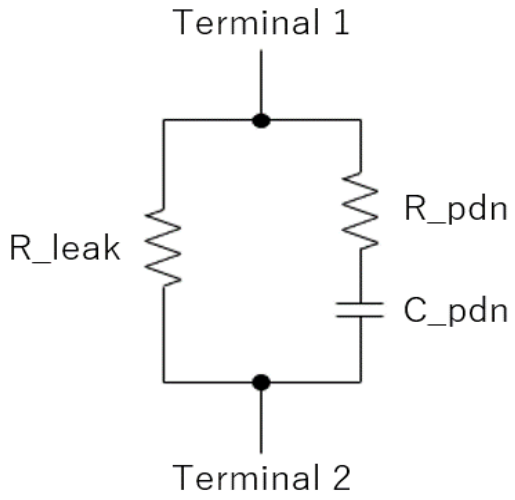


This entire block replaces C_comp and its variants

The model can be a SPICE model or an S-parameter network

On-Die Power Distribution Networks

- A new set of keywords has been added to describe decoupling networks on the device die and to capture power supply noise effects, “especially in the high-frequency range”



PDN networks are simply described, and connect between signal names or bus labels (terminals) described as PDN Domains

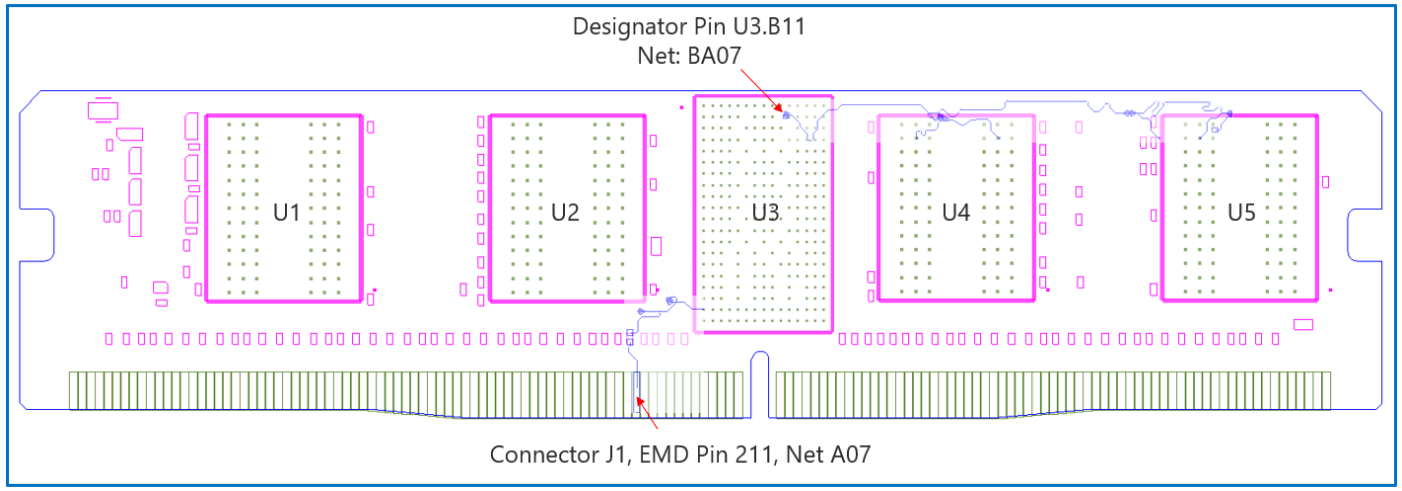
This connects rails, not just pins

Variations are independent of [Model] typ/min/max corners

This is an alternative to Series and Interconnect Model keyword representations and can coexist with them

EMD: Electrical Module Descriptions

- A way to describe complex networks of devices and/or interconnects that can in turn be used as modules in other networks
  - Imagine a DIMM electrical model: a PCB and DRAM device which, together, can be used in multiple instances in a PCB system model
- The successor to EBD, the Electrical Board Description (EBD) format
  - EBD had many limitations on connectivity and electrical modeling capabilities



Four devices here are instances of a single IBIS component

The devices are combined on a substrate with its own interconnect description

The substate is a DIMM, which would be simulated in a larger system

Summary of Other Major Changes

- DC Offset
  - Expands support for single-ended interfaces (e.g., DDR) by communicating channel DC level to IBIS-AMI receivers
- Back-channel Statistical Optimization
  - Expands model-to-model training of equalization beyond bitstream simulation
- Sampling Position in AMI_Init Flow
  - Enables more model-level control of signal sampling in statistical IBIS-AMI simulations
- Expanding Architectural Descriptions, Including Clocking and Clock-Forwarding Support
  - Adding Component_Name and Signal_Name enables buffer-specific information to be passed into IBIS-AMI models at the component level
  - DQ/DQS GetWave support enables clock ticks to be used in data latching across models
  - Explicit links between clock and data pins permits tools to monitor and impose component latching relationships

What's Next

- IBIS 7.1 Draft has been released for review
  - https://ibis.org/ver7.1_wip
  - Second official Open Forum review will take place at November 20, 2021 meeting
  - Possible vote on IBIS 7.1 at December 10, 2021 Open Forum meeting
  - Member companies: watch for vote solicitation email to participate in voting
- IBISCHK 7.1.0 syntax parser will be ready for release at the same time as IBIS 7.1 approval!

Please review the draft IBIS 7.1 document – your feedback is gratefully accepted!