



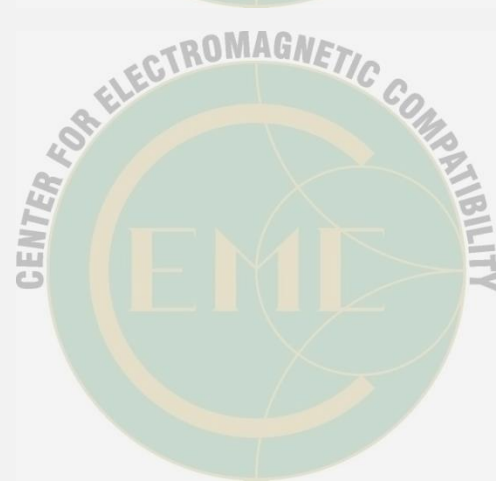
IBIS Model Simulation Accuracy Improvement by Including PSIJ Effect



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- Limitation of the Current Power-Aware IBIS Model

II. Jitter Sensitivity Based Modification

- Ku/Kd Modification Based on PSIJ Sensitivity

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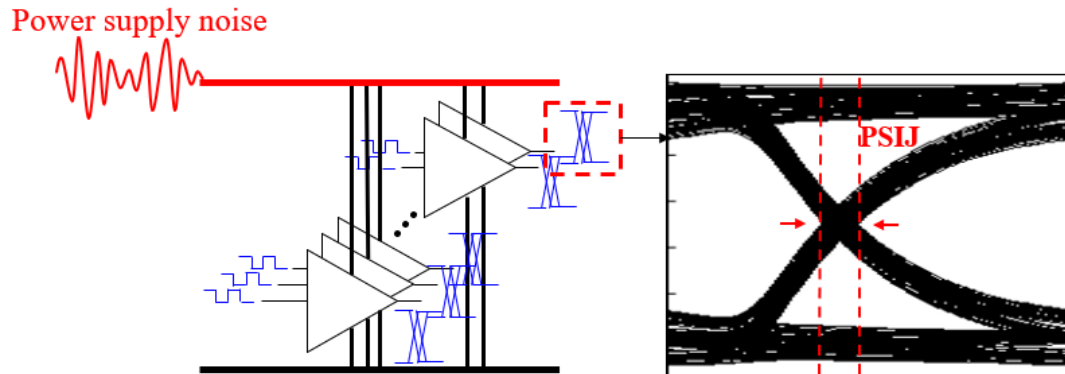
- 8 Stage Inverter Chain with Different Loads
- DDRx DQ Tx Buffer with Pre-driver with Different Terminals

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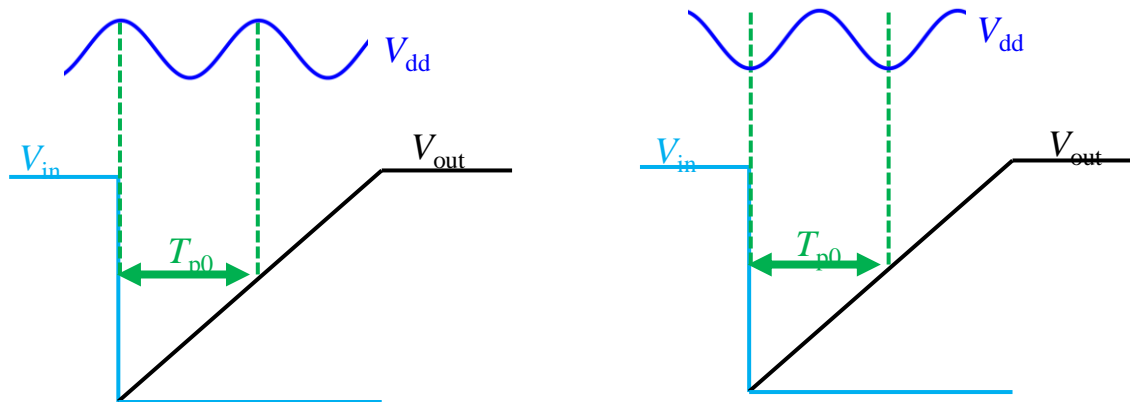
Power Supply Induced Jitter (PSIJ)

Power supply induced jitter (PSIJ):

- The time variation in the output transition edges from ideal positions due to the voltage fluctuations on power rail.



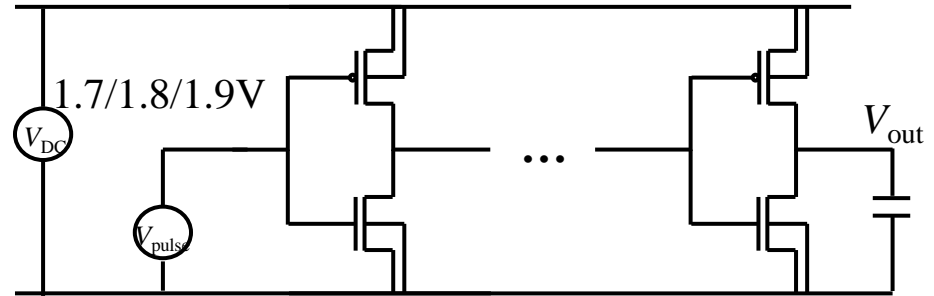
- The V_{cc} noise can take effect during the propagation delay time range;
- The influence is accumulated, just considering instantaneous voltage value is not accurate.



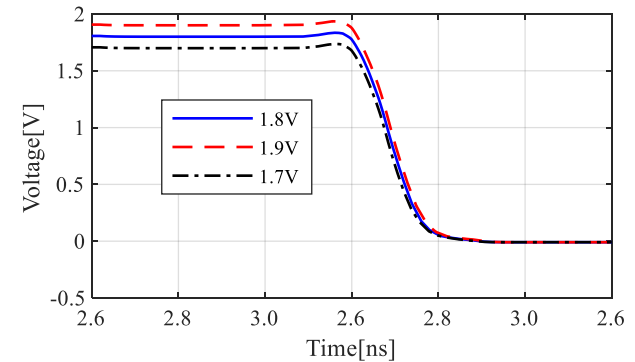
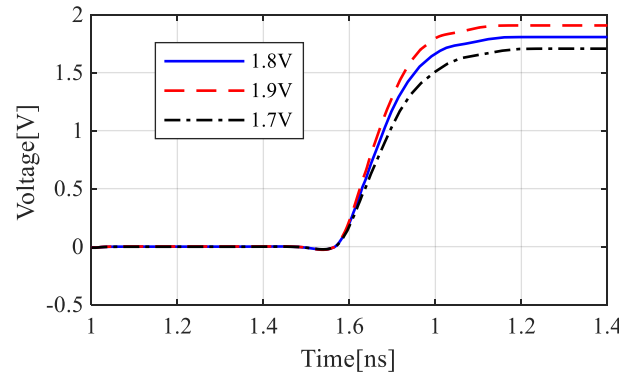
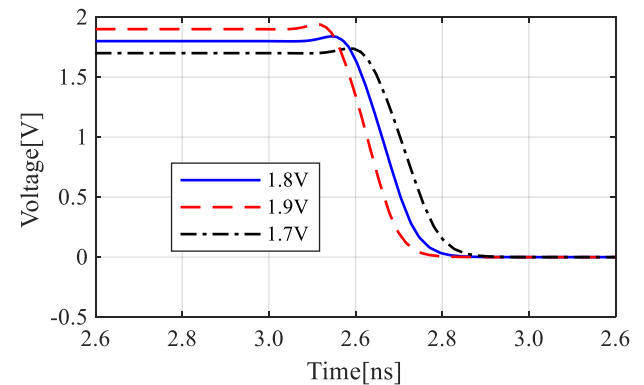
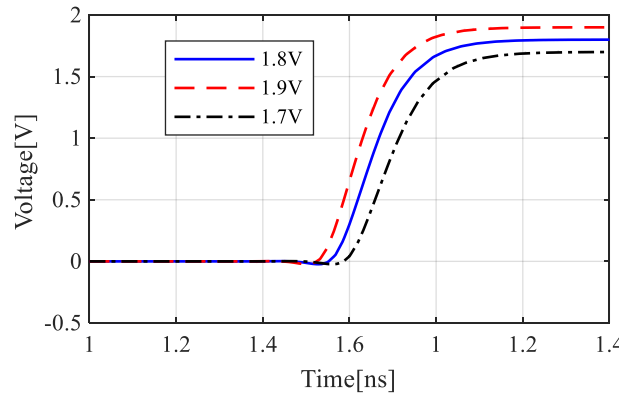
Limitations of the Current Power-Aware IBIS Model

- **Cannot** account for the delay change caused by power noise correctly.

➤ Example: an inverter chain output, change power voltage to 1.7/1.8/1.9V, respectively



SPICE Results



Power-aware IBIS model
Results
(ver5.1, generated with EDA tool)

Limitations of the Current Power-Aware IBIS Model

- Power-aware IBIS model considers gate modulation effect, ratio modification on K_u , K_d based on power rail voltage value

Gate Modulation Coefficients

The ST "Gate Modulation" solution is based on the introduction of two coefficients, one for the Pullup and one for the Pulldown stage, which modulate properly the IBIS standard current ($I_{IBIS-STD}$) when a bouncing noise occurs on the power and ground nodes

$$\underbrace{I(V_{gs}, V_{ds})}_{\text{Effective SPICE current}} = K_{ssn}(V_{gs}, V_{ds}) * \underbrace{I(V_{gs}=V_{DD}, V_{ds})}_{\text{IBIS standard current}}$$



$$I_{\text{effective}} = K_{ssn}(V_{gs}, V_{ds}) * I_{IBIS-STD}$$

$$K_d(t) I_{pd} \rightarrow K_{sspd}(V_{pd}) K_d(t) I_{pd}$$

$$K_u(t) I_{pu} \rightarrow K_{sspu}(V_{pu}) K_u(t) I_{pu}$$

$$K_{sspd}(V_{pd}) = \frac{V_{pd}}{I_{sspd}(0)}$$

$$K_{sspu}(V_{pu}) = \frac{V_{pu}}{I_{sspu}(0)}$$

Source: "BIRD 98 and ST 'Gate Modulation' Convergence", IBIS Open Forum Teleconference, Jan. 26th, 2007
http://www.ibis.org/docs/BIRD98&ST_Proposal_Convergence.ppt

- The ratio modification K_{sspd} , K_{sspu} on K_u , K_d is only a function of V_{pd} ($V_{cc}-V_{out}$) or V_{pu} ($V_{out}-V_{gnd}$), it cannot reflect the effect of power rail voltage noise on switching edge timing change

Previous method on modification of K_u , K_d does not consider the time averaged effect;
 Source: Behavioral modeling of jitter due to power supply noise for input/output buffers (US Patent 9842177B1)

Previous Proposed Behavior Model

- Modify $K_u(t)$, $K_d(t)$ as a function of **time averaged** power rail voltage $V_{cc}(t)$; introduce correction coefficient B and A as a function of **time**

$$K_u(t) = K_{u0}(t) + B_u(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau) d\tau}{t} - V_{cc0} \right] + A_u(t) \left[\frac{\int_0^t V_{cc}(\tau) d\tau}{t} - V_{cc0} \right]^2$$

$$K_d(t) = K_{d0}(t) + B_d(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau) d\tau}{t} - V_{cc0} \right] + A_d(t) \left[\frac{\int_0^t V_{cc}(\tau) d\tau}{t} - V_{cc0} \right]^2$$

K_u, K_d under nominal V_{cc}

Linear fitting coefficient

Quadratic fitting coefficient

Averaged $V_{cc}(t)$ after the switching event happens;

- 2 equations, 2 unknowns' algorithm to extract $K_u(t)$, $K_d(t)$ for typ/min/max

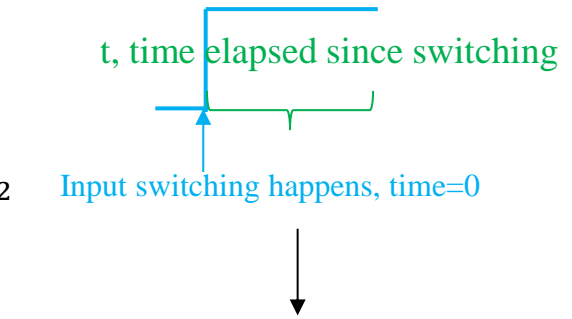
$$K_u(t) * I_u(V_1) + K_d(t) * I_d(V_1) = I_{out}(V_1)$$

$$K_u(t) * I_u(V_2) + K_d(t) * I_d(V_2) = I_{out}(V_2)$$

- 2 equations, 2 unknowns' algorithm to extract $B_u(t)$, $A_u(t)$ and $B_d(t)$, $A_d(t)$

$$K_{u_max}(t) = K_{u0}(t) + B_u(t)(V_{cc_max} - V_{cc0}) + A_u(t)(V_{cc_max} - V_{cc0})^2$$

$$K_{u_min}(t) = K_{u0}(t) + B_u(t)(V_{cc_min} - V_{cc0}) + A_u(t)(V_{cc_min} - V_{cc0})^2$$



Achieved by adding delay elements that store

- The time of switching edges
- Time averaged V_{cc} since switching event happens

- K_u/K_d correction coefficients B and A are related to Process, Voltage and Temperature instead of only the supply voltage fluctuation.

DC Jitter Sensitivity

- Jitter sensitivity can be applied to calculate the total jitter

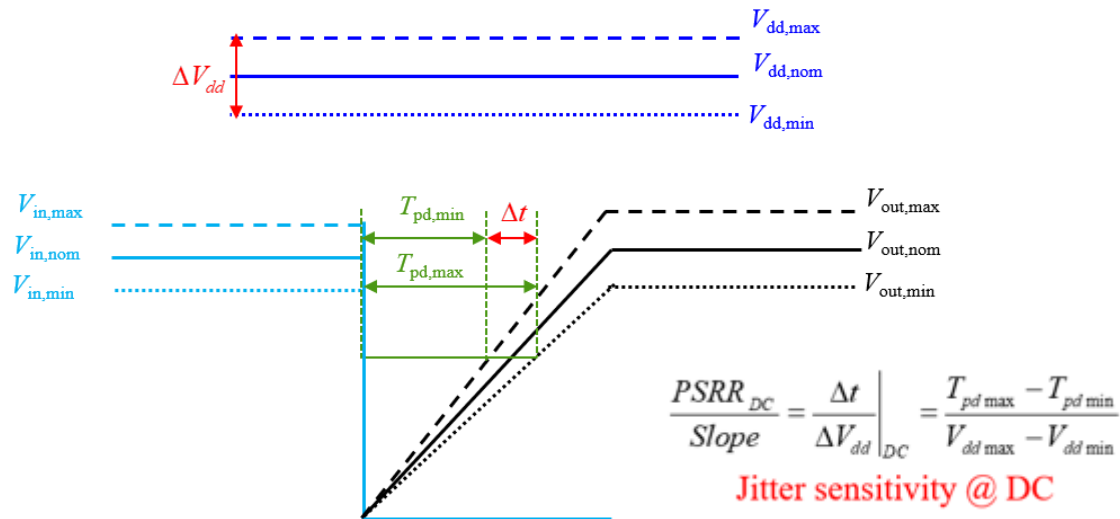
$$\text{Jitter Impact}(f) = \text{Jitter Sensitivity}(f) \cdot V_{\text{noise}}(f)$$

$$\text{Jitter Sensitivity}(\omega) = \frac{T_{pd \max} - T_{pd \min}}{V_{dd \max} - V_{dd \min}} PSRR'(\omega) e^{j\pi f T_{p0}} \text{sinc}(\pi f T_{p0})$$

*Jitter sensitivity @ DC

Frequency dependency due to time averaged effect (already considered by averaging the Vcc)

Frequency dependency due to PSRR (Power Supply Rejection Ratio)



Ku/Kd Modification Based on PSIJ Sensitivity

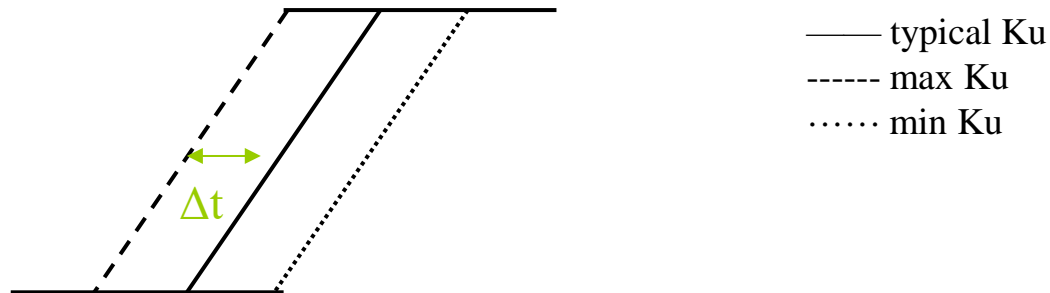
- Propose to use Jitter sensitivity to do modification

$$Ku/Kd_{\max/\min}(t) = Ku/Kd_{\text{typ}}(t \pm \text{DC Jitter sensitivity} \times \Delta V_{\text{dd}})$$



- Should exclude the original IBIS effect.
- Can include pre-driver PSIJ effect.

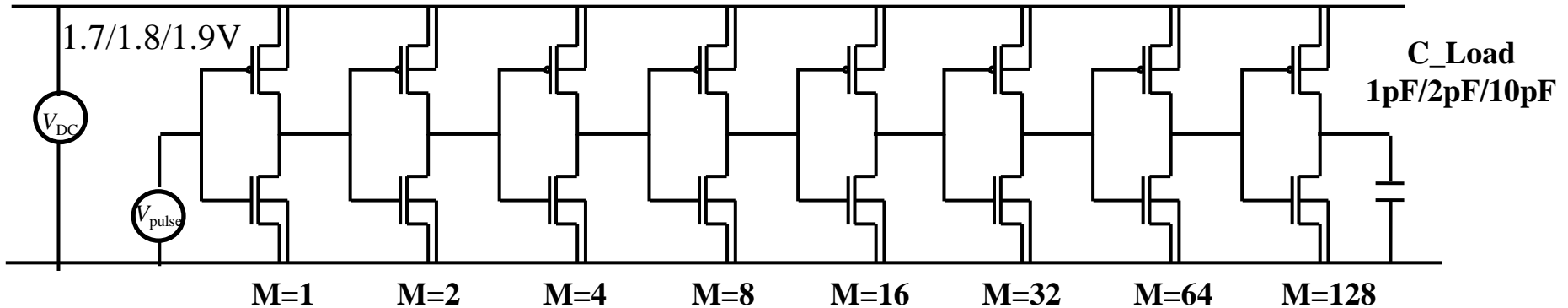
Ku for output rising edge:



$$\Delta t = (\text{Driver output PSIJ sensitivity} - \text{original IBIS PSIJ sensitivity} + \text{pre-driver PSIJ sensitivity}) * (\text{Vdd}_{\text{max}} - \text{Vdd}_{\text{typ}})$$

Simulation Validation – Inverter Chain

- 8 stage inverter chain with different load capacitance



180nm technology, nominal voltage 1.8V

< All NMOS >	< All PMOS >
nch_tn	pch_tn
W = 1 um	W = 2 um
L = 180 nm	L = 180 nm

Results Comparison – Inverter Chain Output Rising Edge

- 8 stage inverter chain with different load capacitance
- DC power noise 1.7V/1.8V/1.9V

	PSIJ Sensitivity (ps/V)					
	Load 1pF to V_{SS}		Load 2pF to V_{SS}		Load 10pF to V_{SS}	
SPICE	184.45		207		350	
Non-Power-aware IBIS	6.5		9.5		39.5	
Power-aware IBIS	35.5		54		217	
Proposed Algorithm	187		210.5		355	
	Δ (to SPICE)					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-Power-aware IBIS	177.95	96.48	197.5	95.41	310.9	88.71
Power-aware IBIS	148.95	80.75	153	73.91	133	38
Proposed Algorithm	2.55	1.38	3.5	1.69	5	1.43

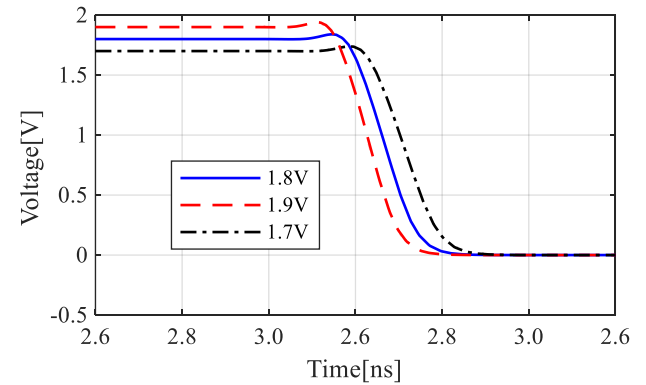
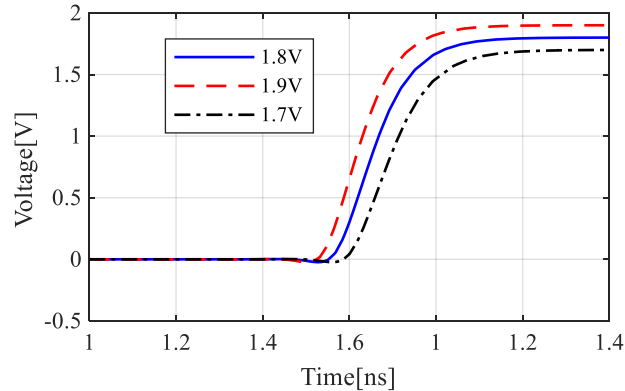
Results Comparison – Inverter Chain Output Falling Edge

- 8 stage inverter chain with different load capacitance
- DC power noise 1.7V/1.8V/1.9V

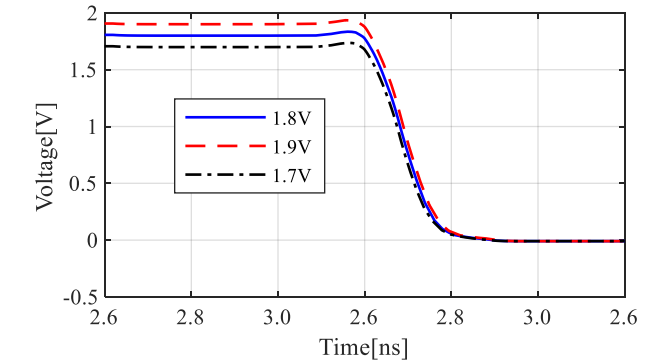
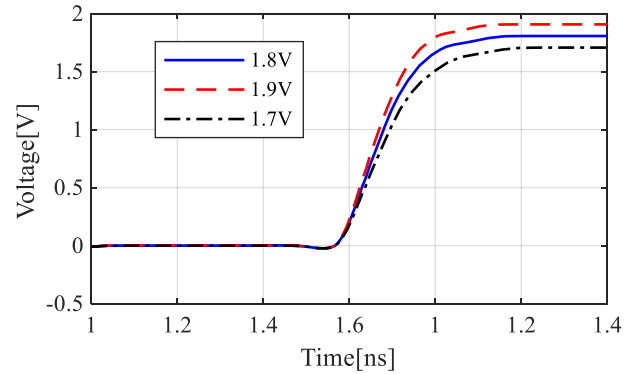
	PSIJ Sensitivity (ps/V)					
	Load 1pF to V_{SS}		Load 2pF to V_{SS}		Load 10pF to V_{SS}	
SPICE	193.91		194.16		188.71	
Non-Power-aware IBIS	-24.41		-36.07		-123.21	
Power-aware IBIS	-25		-35		-135	
Proposed Model	188.95		186.75		175.85	
	Δ (to SPICE)					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-Power-aware IBIS	218.32	112.59	230.23	118.58	311.92	165.29
Power-aware IBIS	218.91	112.89	229.16	118.03	323.71	171.53
Proposed Model	4.96	2.56	7.41	3.82	12.86	6.81

Output Waveform Comparison

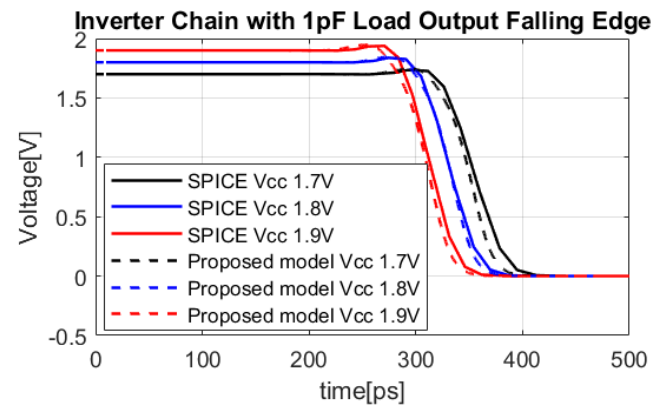
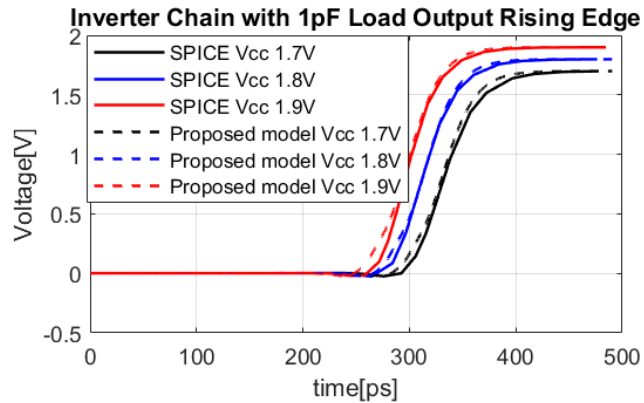
SPICE model



Power-aware IBIS model

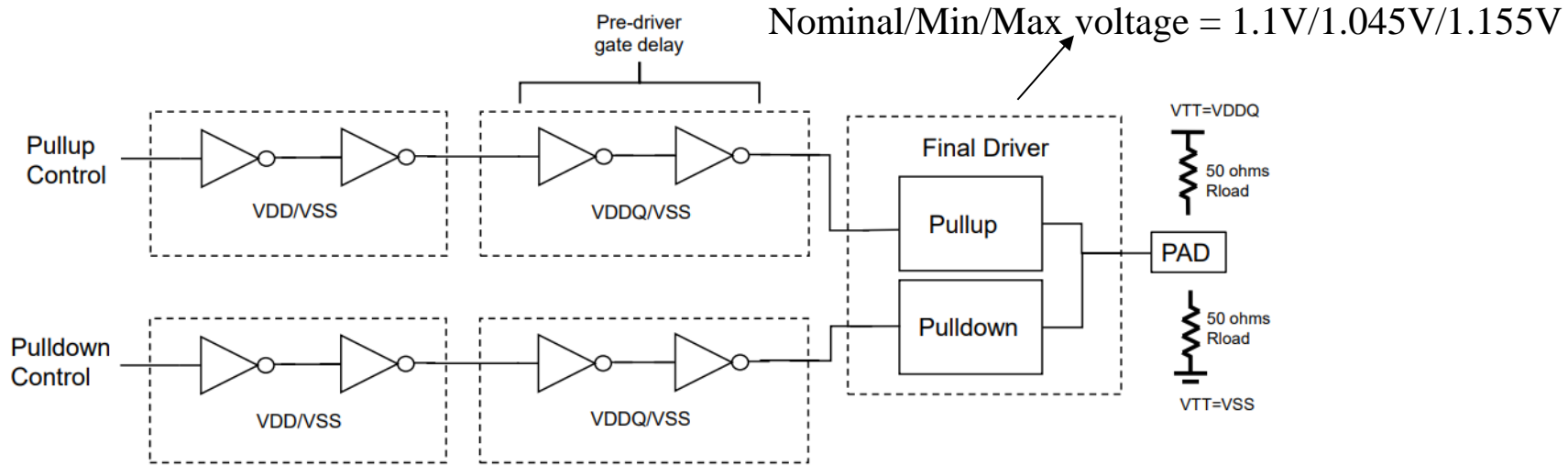


Proposed model compared with SPICE model



Simulation Validation -- DDRx DQ Tx Buffer

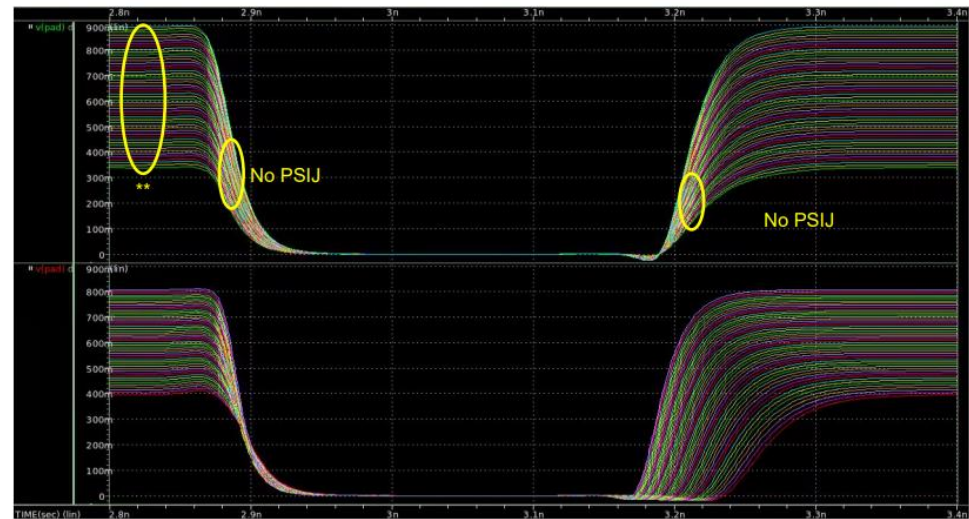
• DDRx DQ Tx Buffer with Pre-driver



- VDDQ Sweep 0.85-1.35V
- Typ Corner
- R_Load = 50 ohm
- $V_{TT} = V_{SS}$

IBIS

SPICE

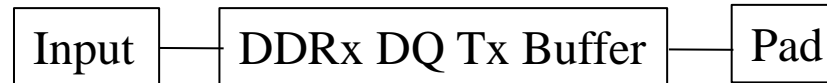


Pre-driver Included in Model

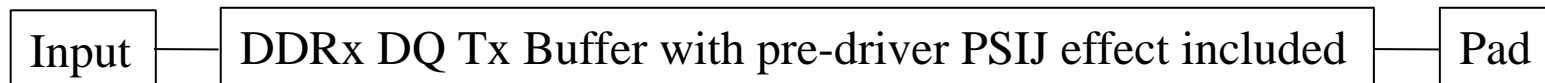
SPICE transistor level simulation



IBIS behavior model simulation can not simulate with pre-driver



Proposed model simulation



Results Comparison – DDRx DQ Tx Buffer Output Rising

- DDRx DQ Tx Buffer with Pre-Driver
- DC power noise 1.045V/1.1V/1.155V

	PSIJ Sensitivity (ps/V)							
	Load 50 ohm to V_{SS}		Load 50 ohm to V_{DDQ} (variable)		Load 50 ohm to V_{DDQ} (Fixed 1.1V)			
SPICE	156.65		134.17		95.45			
Non-Power-aware IBIS	15.45		38.18		6.36			
Power-aware IBIS	60		45.45		14.55			
Proposed Model	159.09		147.27		107.27			
	Δ (to SPICE)							
	Absolute error (ps/V)		%		Absolute error (ps/V)		%	
Non-Power-aware IBIS	141.2		90.14		95.99		71.54	
Power-aware IBIS	96.65		61.70		88.72		66.13	
Proposed Model	2.44		1.56		13.1		8.9	
	11.82		12.38					

Conclusion

- A behavior model based on driver DC jitter sensitivity is proposed to improve the IBIS simulation accuracy in time domain.
- Time averaged effect on power rail is considered.
- Pre-driver PSIJ effect can be included in IBIS simulation.