SPIM (Standard PI Model) in IBIS

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Presenter

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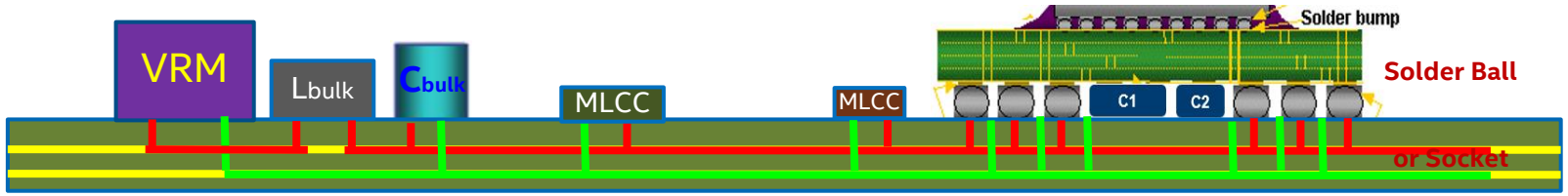
Kinger drives CPU+ dGPU better together strategy in mobile platforms and leads strategic PI design tool evolution in Client Computing Group.
Kinger was awarded Ph. D by Shanghai Jiao Tong University in 2001, and MBA degree by W.P. Carey business school in ASU in 2008.
Kinger works in signal & power integrity domains for 20+ years.
Kinger holds 12 granted patents, and published 30+ papers.

Agenda

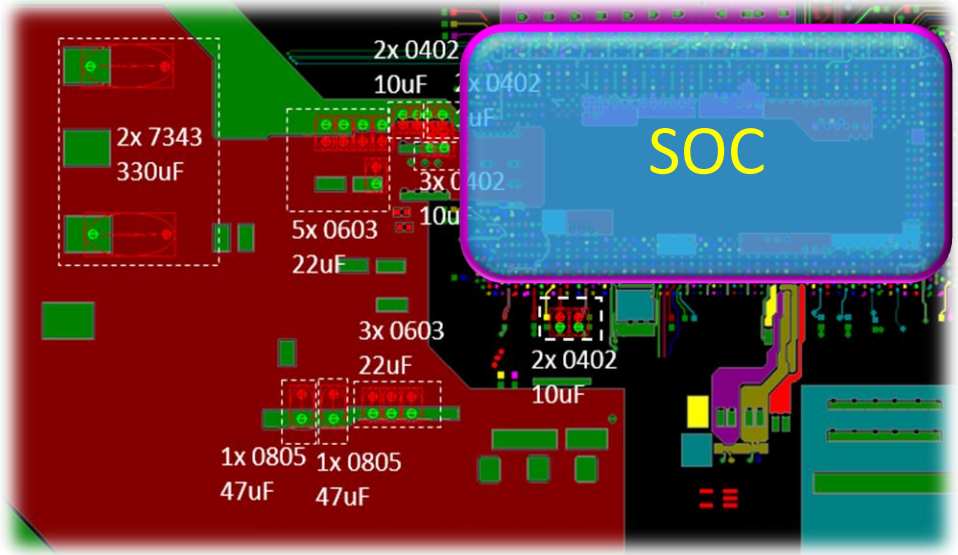
- Industry Platform PI Design Challenges
- Platform PI design Architecture Standardization
  - SPIM – Standard Power Integrity Model
  - SPIM stimulus and target definition
  - FastPI – Platform PI design Framework
- Keywords definition for .spim FILE in BIRD
- One example .spim FILE
- Tree Structure of .spim FILE
- FastPI Roadmap
- Next Steps

Platform PI design: Beyond Conventional Methodology

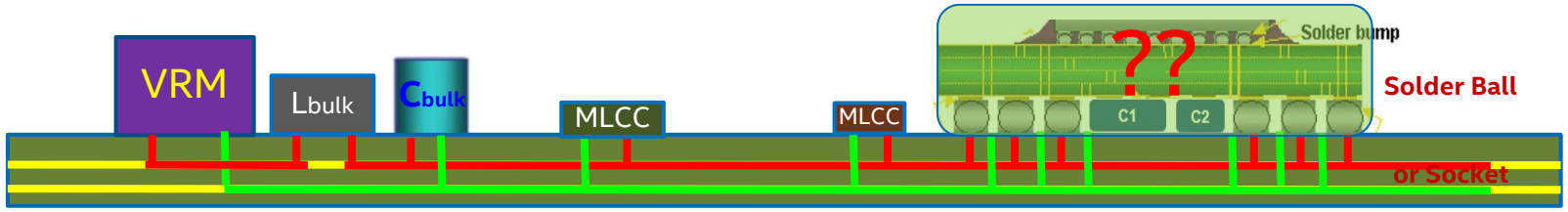


- More flexibility, besides copying exactly from reference design with platform design guideline
- More effective platform PDN optimization, instead of time-consuming what-if simulation
- More efficient platform PI design review and sign-off process

	8L-T3-DS (SD) BOM	
	Primary (TSC)	Secondary (BSC)
VCCin	2x 7343-330uF	4x 0402 1uF
	3x 0805-47uF	
	10x 0603-22uF	
	2x 0402-10uF	
VCCin_Aux	2x 7343-220uF 13x0402-10uF 2x0603 -22uF	12x0402 -10uF
VDDQ	2x0603-22uF 1x0603 (PH)	6x0402-1uF 2x0402-10uF 3x0402 (PH)

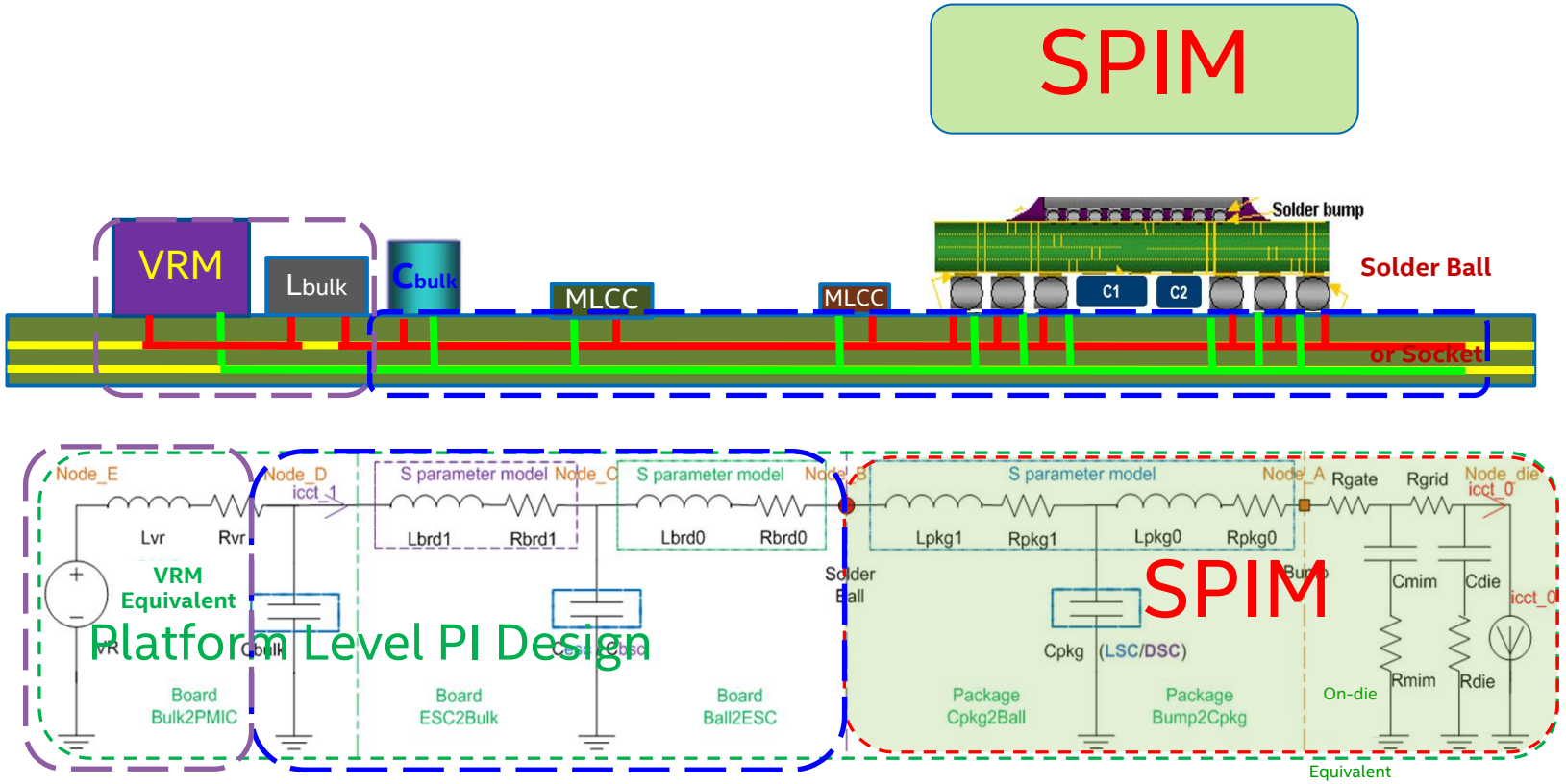


Platform PI design: Collateral, Architecture and Tools



- PI design collateral: Chip vendors to platforms designers
  - ✓ Minimal, while accuracy guaranteed
  - ✓ Sufficient, while IP protected
  - ✓ Standardized, and scalable
- PI design Architecture, Framework and Tool
  - ✓ Standard architecture
  - ✓ Flexible framework
  - ✓ Efficient simulation tools

Platform PI Design: SPIM- Standard PI Model



SPIM creation steps:

- Generation
- Correlation
- Verification

**IEEE paper: VRM Modeling for Platform FastPI upon SPIM

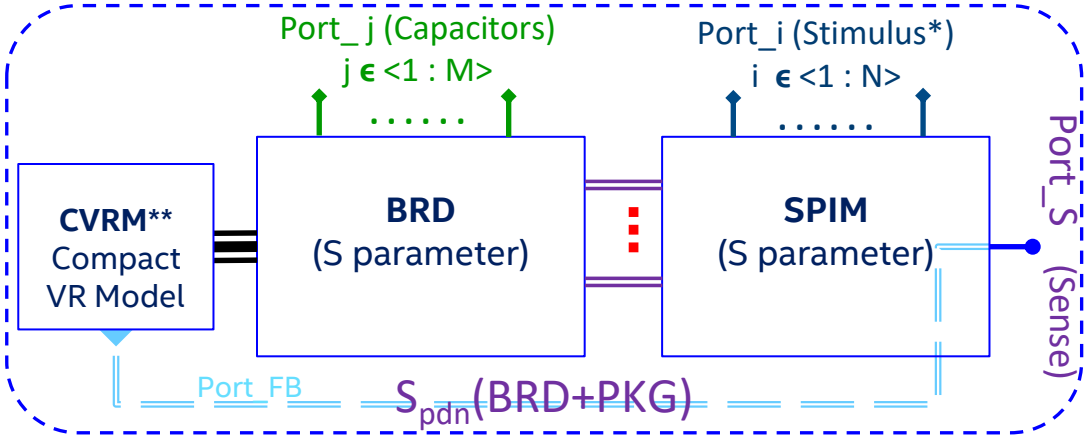
2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium

Xingjian Kinger Cai; Wei Qian; Chi-te Chen; etc., page 162, August 2021

- **SPIM:** Standardized PI Model, for each power rail in a SoC/PKG, or a module.

Platform PI Design: Stimulus & Target Definition

- Impedance at observing Port_S
  - $[S_{pdn}]$ ➔ $[Z_{pdn}]$, in FastPI
  - $[V] = [Z_{pdn}][I]$
  - $[V]=[v_1, v_2, \ldots, v_N, v_S]^T$
  - $[I]=[w_1, w_2, \ldots, w_N, 0]^T$
  - $\sum_{i=1}^{i=N} w_i = 1$, weighted normalization
  - $Z_S=V_S= \sum_{i=1}^{i=N+1}(Z_{pdn(N+1),i} * w_i)$
  - $Z_S= \sum_{i=1}^{i=N}(Z_{pdn(N+1),i} * w_i)$



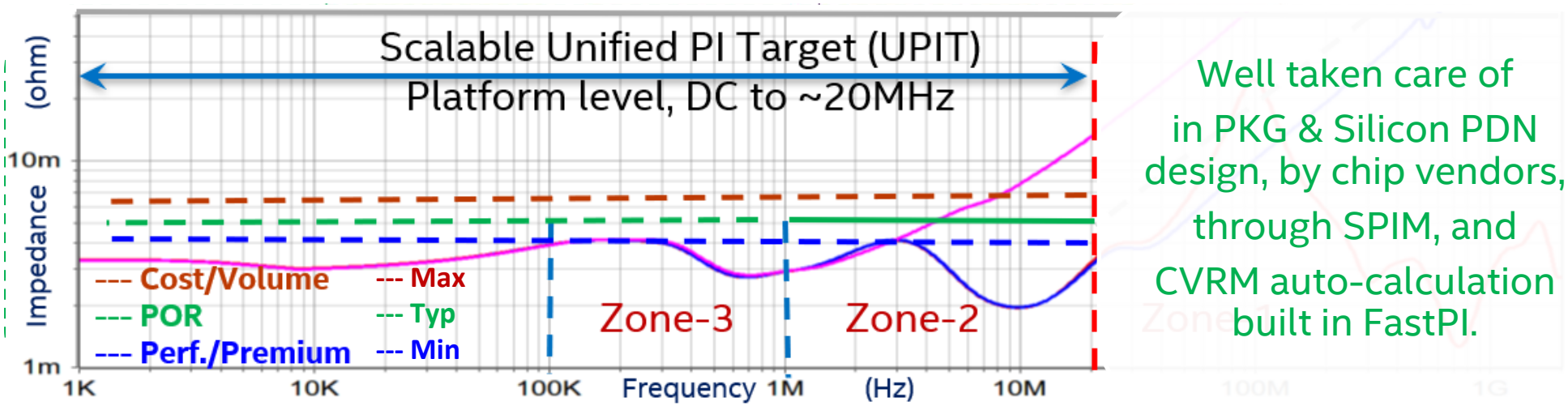
*The impedance, measured at the Port_FB differential pair, is equivalent to that observed at the observing port (Port_S), which is usually located somewhere in package.

**IEEE paper: VRM Modeling for Platform FastPI upon SPIM
2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium
Xingjian Kinger Cai; Wei Qian; Chi-te Chen; etc., page 162, August 2021

Impedance target is generally defined at an observing Port_S (where might align with the sensing/feedback).

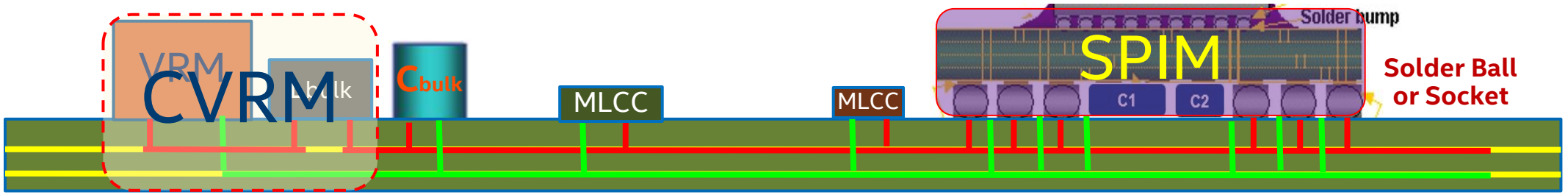
Intel FastPI: Platform PI Design Framework

- Enable board PDN design with “Electrical Equivalence”, away from “Physical Equivalence”
  - FastPI for board PI design, full design flexibility with SPIM and CVRM



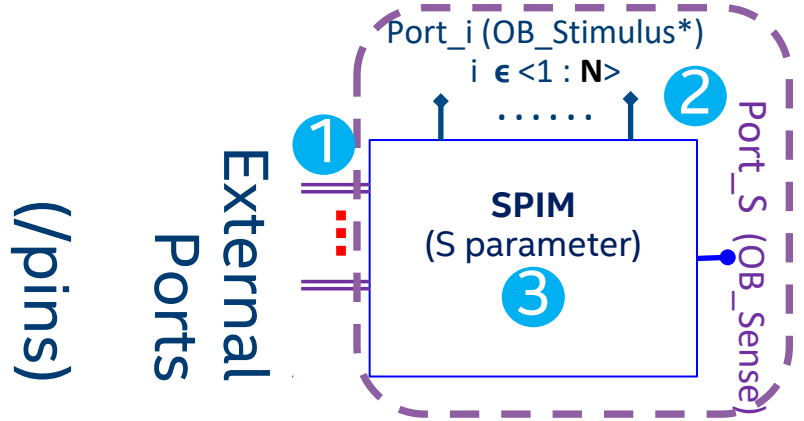
Well taken care of in PKG & Silicon PDN design, by chip vendors, through SPIM, and CVRM auto-calculation built in FastPI.

IEEE Paper: Scalable Platform Power Integrity Design Approach with Standard PI Model (SPIM) and Unified PI Target (UPIT)
2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)
Xingjian Kinger Cai; Yun Ling; Steven Yun Ji; Jimmy Hsiao; Chi-te Chen; Denis Chen, page 64-66, 14-18 May 2018



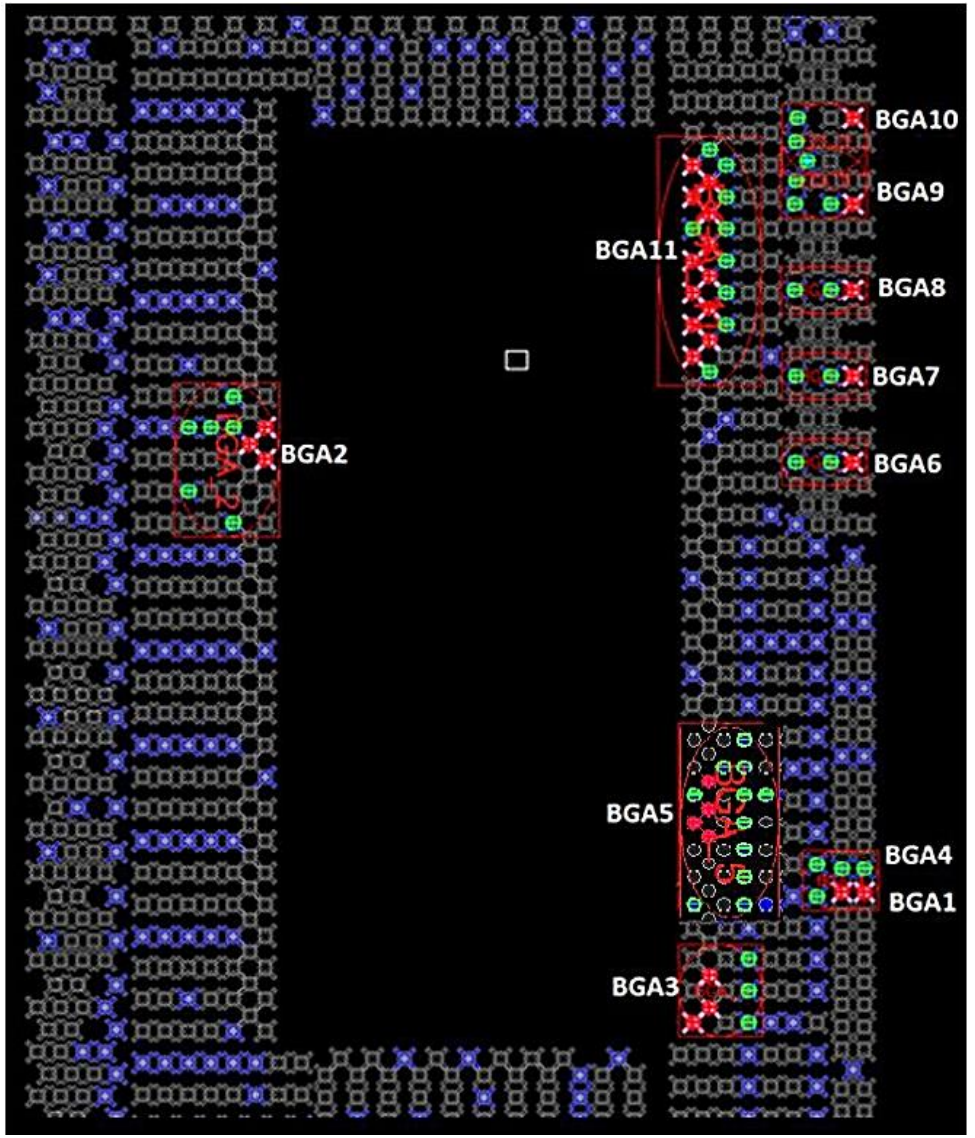
Keywords Defined in IBIS BIRD for spim FILE

1. [SPIM Pin Cluster]
2. [SPIM Port List]
3. OB_Stimulus and OB_Sense
4. [SPIM Touchstone File]
5. [SPIM Stimulus]
6. [SPIM Target]
7. [SPIM Observation Port]
8. [SPIM Rnetwork File]
9. [SPIM Current]
10. [SPIM Voltage List]
11. [SPIM Rail]
12. [Chip SPIM]
13. [Chip SPIM Group] , in *.ibs file



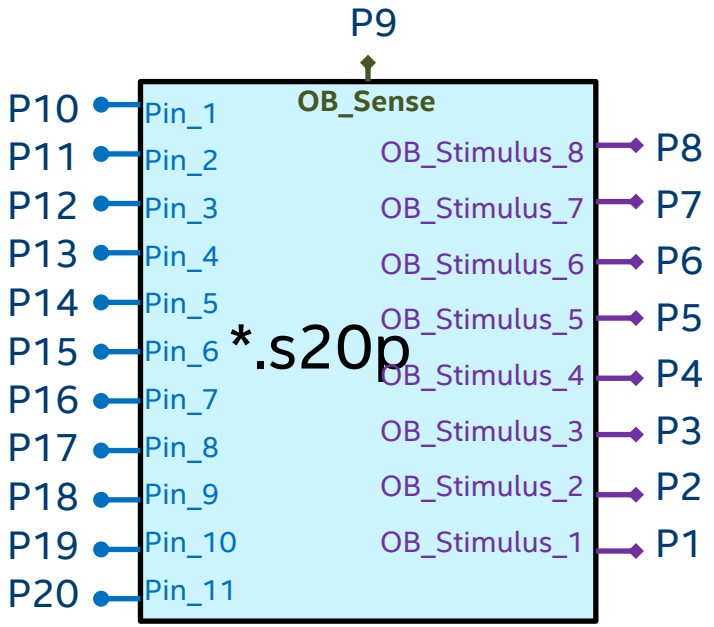
Example .spim FILE - [SPIM Pin Groups]

```
[Chip SPIM] Intel_CPU2

[SPIM Rail] VCC3

[SPIM Pin Cluster] VSS
| Pin_group_name    Pin_name

VCC3_1        AK1
VSS_VCC3_1    AM1 AM4 AK4

VCC3_2        BY39 BV39 BW40
VSS_VCC3_2    CB41 BY41 BP41 BY42 BY44 BT44

VCC3_3        AC10 AE10 AB12
VSS_VCC3_3    AB8 AD8 AF8

VCC3_4        AK2
VSS_VCC3_4    AM1 AM2 AM4

| …

VCC3_11        CY1
VSS_VCC3_11    CY5 CV5 CU4

[End SPIM Pin Cluster]
```



Example .spim FILE – [SPIM Port List]

```
[SPIM Port List]
|Port   Terminal_p          Terminal_n
1       OB_Stimulus_1_p     OB_Stimulus_1_n
2       OB_Stimulus_2_p     OB_Stimulus_2_n
3       OB_Stimulus_3_p     OB_Stimulus_3_n
4       OB_Stimulus_4_p     OB_Stimulus_4_n
5       OB_Stimulus_5_p     OB_Stimulus_5_n
6       OB_Stimulus_6_p     OB_Stimulus_6_n
7       OB_Stimulus_7_p     OB_Stimulus_7_n
8       OB_Stimulus_8_p     OB_Stimulus_8_n
9       OB_Sense_p          OB_Sense_n
10      VCC3_1              VSS_VCC3_1
11      VCC3_2              VSS_VCC3_2
12      VCC3_3              VSS_VCC3_3
13      VCC3_4              VSS_VCC3_4
14      VCC3_5              VSS_VCC3_5
15      VCC3_6              VSS_VCC3_6
16      VCC3_7              VSS_VCC3_7
17      VCC3_8              VSS_VCC3_8
18      VCC3_9              VSS_VCC3_9
19      VCC3_10             VSS_VCC3_10
20      VCC3_11             VSS_VCC3_11
[End SPIM Port List]
```



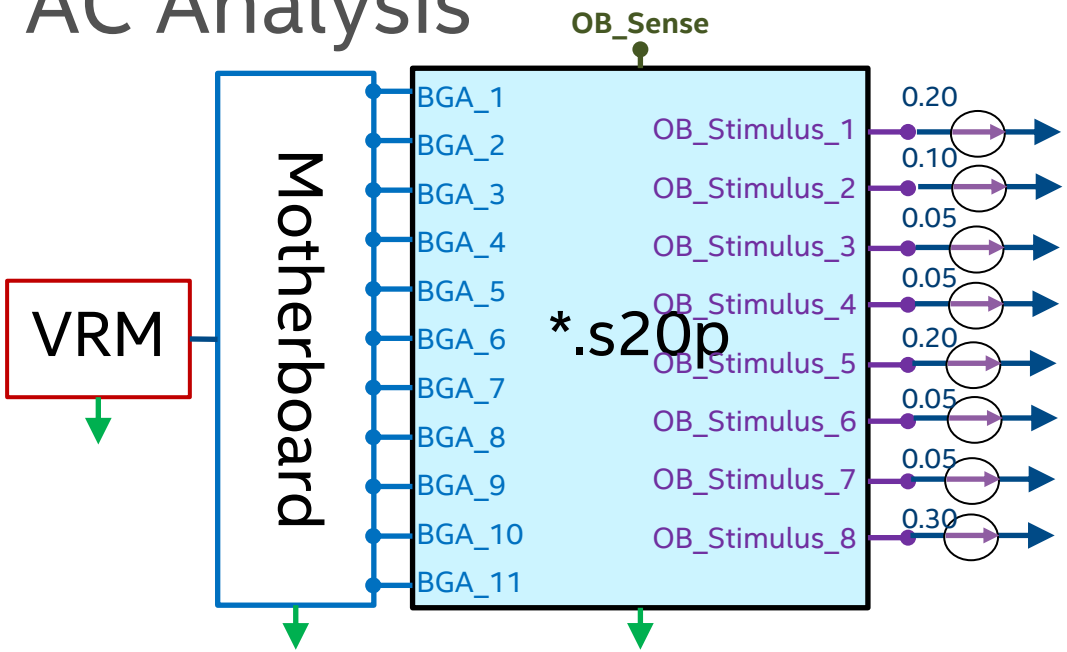
Both OB_Stimulus_ and OB_Sense_ are reserved terminal prefixes.

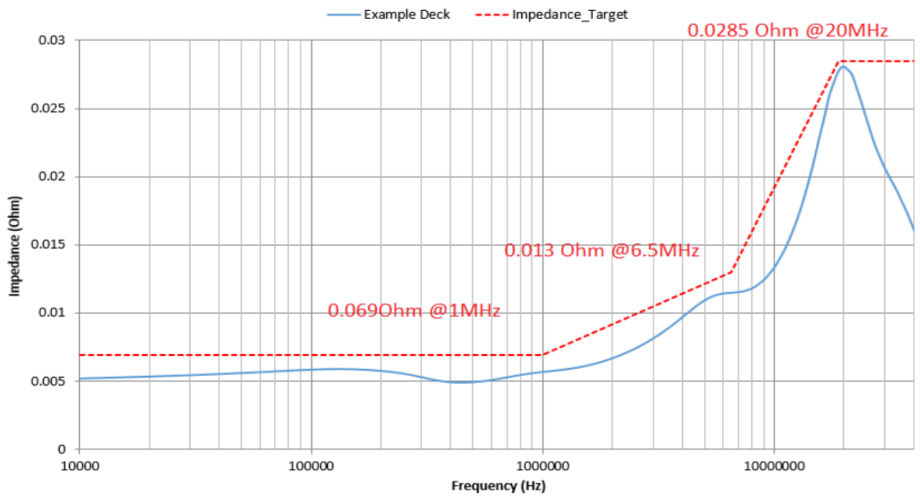
Example .spim FILE - Supports PI AC Analysis

```
[SPIM Touchstone File]
| file_type file_reference
File_TS <path>Intel_CPU2_VCC3_PKG.s20p
[End SPIM Touchstone File]
|*** Here below explains how to use
*.snp s-element model in IBIS-ISS.
|.model pkg_model S N=20 tstonefile
|  ='Intel_CPU2_VCC3_PKG.s20p'
|S_one_ref
|+ OB_Stimulus_1
|+ OB_Stimulus_2
|+ OB_Stimulus_3
|+ OB_Stimulus_4
|+ OB_Stimulus_5
|+ OB_Stimulus_6
|+ OB_Stimulus_7
|+ OB_Stimulus_8
|+ OB_Sense
|+ BGA_1
|+ BGA_2
|+ BGA_3
|+ BGA_4
|+ BGA_5
|+ BGA_6
|+ BGA_7
|+ BGA_8
|+ BGA_9
|+ BGA_10
|+ BGA_11
|+ 0
|+ mname=pkg_model
```

```
[SPIM Stimulus]
|OB_Stimulus    Weighting
OB_Stimulus_1    0.20
OB_Stimulus_2    0.10
OB_Stimulus_3    0.05
OB_Stimulus_4    0.05
OB_Stimulus_5    0.20
OB_Stimulus_6    0.05
OB_Stimulus_7    0.05
OB_Stimulus_8    0.30
[End SPIM Stimulus]
```

```
[SPIM Target]
[SPIM Observation Port] OB_Sense
| Z(Frequency) Z(typ) Z(min) Z(max)
10000          0.0069 NA     NA
1000000        0.0069 NA     NA
6500000        0.0130 NA     NA
19000000       0.0285 NA     NA
40000000       0.0285 NA     NA
[End SPIM Target]
```





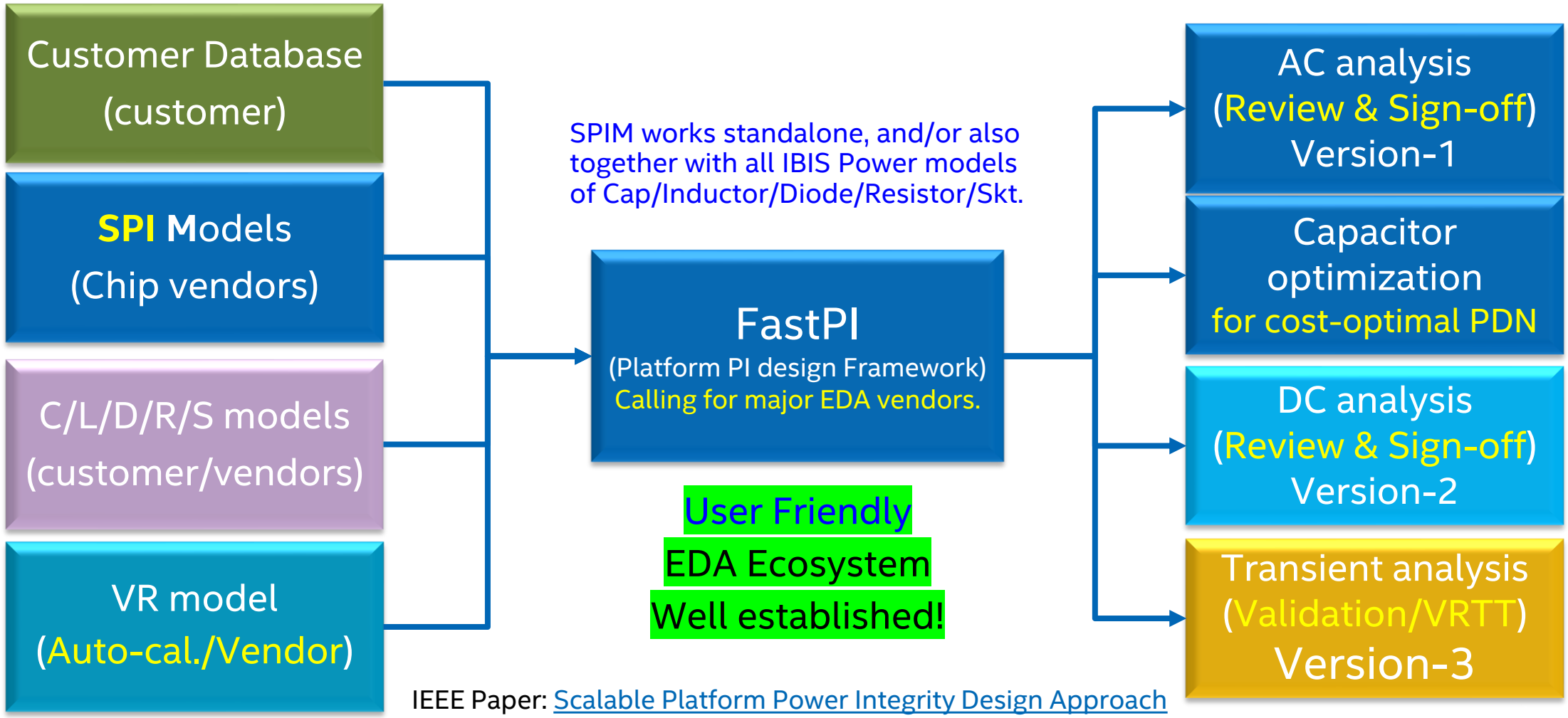
Example .spim FILE - Supports Power DC Analysis

```
[Rnetwork File]
| file_type file_reference
File_IBIS_ISS <path>My_CPU2_VCC3_PKG_Rnetwork.ckt
| …
[End SPIM Rnetwork File]
|
[SPIM Current]
| I(name)     I(typ)      I(min)       I(max)
VCC3           4.50       NA           7.50
[End SPIM Current]
|
|************************************************
[SPIM Voltage List]
| V(name)      V(typ)         V(min)         V(max)
VCC3           1.000          0.900           1.100
[End SPIM Voltage List]
|
|************************************************
[End SPIM Rail]        | VCC3
|************************************************
[End Chip SPIM]        | Intel_CPU3
```

Tree Structure of .spim FILE

```
.spim FILE
-----------
  |-- File Header Section
  |   -------------------
  |     |-- [IBIS Ver]
  |     |-- [Comment Char]
  |     |-- [File Name]
  |     |-- [File Rev]
  |     |-- [Date]
  |     |-- [Source]
  |     |-- [Notes]
  |     |-- [Disclaimer]
  |     |-- [Copyright]
  |
  |-- [Chip SPIM]
  |   -----------------
  |     |-- [Manufacturer]
  |     |-- [Description]
  |     |
  |     |-- [SPIM Rail]
  |     |   ------------
  |     |     |-- [SPIM Pin Cluster]
  |     |     |   -----------------
  |     |     |     |-- [End SPIM Pin Cluster]
  |     |     |     |
  |     |     |-- [SPIM Port List]
  |     |     |   ----------------
  |     |     |     |-- [End SPIM Port List]
  |     |     |
.
  |     |     |-- [SPIM Touchstone File]
  |     |     |   --------------------------
  |     |     |     |-- [SPIM Stimulus]
  |     |     |     |   ---------------
  |     |     |     |     |-- [End SPIM Stimulus]
  |     |     |     |-- [SPIM Target]
  |     |     |     |   ------------
  |     |     |     |     |-- [SPIM Observation Port]
  |     |     |     |     |-- [End SPIM Target]
  |     |     |     |-- [End SPIM Touchstone File]
  |     |     |
  |     |     |-- [SPIM Rnetwork File]
  |     |     |   ------------------------
  |     |     |     |-- [SPIM Current]
  |     |     |     |   --------------
  |     |     |     |     |-- [End SPIM Current]
  |     |     |     |-- [SPIM Voltage List]
  |     |     |     |   ---------------
  |     |     |     |     |-- [End SPIM Voltage List]
  |     |     |     |-- [End SPIM Rnetwork File]
  |     |     |-- [End SPIM Rail]
  |     |
  |     |-- [End Chip SPIM]
  |
  |-- [End]
```

FastPI (Platform PI Design with SPIM) Roadmap



IEEE Paper: Scalable Platform Power Integrity Design Approach with Standard PI Model (SPIM) and Unified PI Target (UPIT)

Next Steps:

- Submit BIRD of .spim FILE and all relevant keywords in IBIS
- Call for EDA vendors to support .spim FILE in IBIS
- Call for chip vendors to support .spim FILE in IBIS
- Call for platform designers to support .spim FILE in IBIS

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