

IBIS Open Forum Minutes

Meeting Date: November 11, 2022 Meeting Location: 2022 Virtual Asian IBIS Summit - Japan

VOTING MEMBERS AND 2022 PARTICIPANTS

AMD (Xilinx) Analog Devices (Maxim Integrated)

ANSYS Applied Simulation Technology Aurora System Broadcom Cadence Design Systems

Celestica Cisco Systems Dassault Systemes Google Huawei Technologies Infineon Technologies AG Instituto de Telecomunicações Intel Corporation

Keysight Technologies

Luminous Computing Marvell MathWorks Micron Technology

Micron Memory Japan, K.K. MST EMC Lab

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Casio Computer Co., Ltd. Ciena CMK Corporation Cornelis Networks Cybernet Systems Co., Ltd. De Montfort University Faurecia Clarion Electronics Co., Ltd. FICT Limited

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In the list above, attendees at the meeting are indicated by *. Those submitting an email ballot for their member organization for a scheduled vote are indicated by ^. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The connection information for future IBIS teleconferences is as follows:

Microsoft Teams meeting

Join on your computer or mobile app Click here to join the meeting

Join with a video conferencing device

<u>106010980@teams.bjn.vc</u> Video Conference ID: 114 666 897 5 Alternate VTC dialing instructions

Or call in (audio only) +1 267-768-8015,554664847# United States, Philadelphia Phone Conference ID: 554 664 847# Find a local number | Reset PIN Learn More | Meeting options

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The Virtual Asian IBIS Summit – Japan was held online. About 134 individuals representing 78 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

https://ibis.org/summits/nov22b/

A summit recording has been uploaded and is available by direct link:

https://ibis.org/summits/nov22b/summit_recording.mp4

Randy Wolff welcomed everyone to the 17th annual IBIS Summit - Japan. He said it was good to see so many attendees for a virtual event. Hopefully next year we will all be together in person. Randy thanked JEITA for hosting the Summit and for help organizing this event. He also said thank you to the many co-sponsors, and special thanks to Bob Ross and other IBIS officers for helping organize the Summit and to Ted Mido for helping with translations. He also thanked the presenters.

Randy noted there would be several presentations covering current and proposed IBIS features. Participants could follow along by downloading the slides from the IBIS Summits webpage. He said he hoped everyone enjoyed the presentations, and he looked forward to good discussions and sharing knowledge and ideas to improve IBIS.

MEETING WELCOME

Hayato OGAWA (Keysight Technologies, Japan) Chair, JEITA EDA Model Specialty Committee (Start 00:08:45, Duration 4:45)

Hayato Ogawa thanked attendees for joining, noting that this was the 17th year of the IBIS Summit in Japan. He introduced the EDA Model Specialty Committee under the JEITA/EC Center. The committee has a website and a YouTube channel. More information at:

https://ec.jeita.or.jp/eda/

He also thanked the sponsors of the IBIS Summit.

IBIS CHAIR'S REPORT

Randy WOLFF (Micron Technology, USA) (Chair, IBIS Open Forum) (Start 00:26:15, Duration 15:15)

Randy Wolff introduced the list of officers of the IBIS organization. He also shared slides on the IBIS Meetings, outlining when meetings are regularly scheduled for each task group, as well as

the Open Forum meeting where official voting and planning occurs. Summit meetings such as this are usually held multiple times a year, including at DesignCon in Santa Clara, California, European IBIS Summit with IEEE Workshop on SPI, IEEE Workshop on EMC+SIPI, and Asian IBIS Summits for Japan, Taiwan, and China. The parent organization of IBIS is SAE-ITC. He showed a slide detailing the task groups as well.

He announced IBIS Version 7.2 will include BIRD213.1 for PAMn support and BIRD211.4 for major work in flow issues in re-drivers. BIRD217 introduces a new requirement for clocked IBIS-AMI models. BIRD218 will be a simplification to some pin rules in EMD. The Editorial and Advanced Technology Modeling task groups are working on a clarification BIRD for clock_times with use of the new clocked IBIS-AMI models. The goal is to approve IBIS 7.2 in late January.

Future Work:

Randy showed a slide outlining future work, such as equalization with DDR5, clock/data relationships, and a renewed focus on power integrity such as power supply induced jitter modeling, modeling voltage regulators, and other topics. Randy also said the Interconnect task group has in development a pole-residue format for an upcoming Touchstone 3.0 specification. Also, further improvements to IBIS-ISS, which is a standard SPICE format.

Call for Volunteers:

Randy presented a slide calling for volunteers and outlined which roles are available to make contributions and participate in collaboration, as well as the email reflector and website information. He further announced that presentations are always welcome.

Official Proceedings:

Randy announced the processes to express a technical idea as part of a Task Group and mentioned that experienced members can assist with formatting and syntax for creating technical proposal documents such as in BIRD format.

Website:

Randy presented the website and outlined the available resources provided by the IBIS organization [available at this link: <u>https://ibis.org/</u>].

IBIS ELECTRICAL MODULE DESCRIPTION (EMD) OVERVIEW

Randy WOLFF (Micron Technology, USA) (Start 00:46:15, Duration 40:00)

Synopsis: Presentation agenda as follows:

- Review IBIS EBD Modeling
- EMD Goals
- Overview
- Syntax Details
- Key Rules
- EMD Examples
- Conclusions

Q&A session:

A question was asked about the difference between IBIS-ISS supported by Interconnect Model syntax released in IBIS 7.0 and EMD.

Randy answered that IBIS-ISS and Touchstone can be the formats of the models, and EMD or Interconnect Model syntax are IBIS wrappers around these models. IBIS EMD describes the purpose of IBIS-ISS terminals such as if they are signals, powers, or grounds. The IBIS wrapper makes it easier for EDA tools to use the IBIS-ISS model in simulation.

A follow-up question asked if any examples of the EMD syntax are available to help learn how to create models. Randy replied that he thought it was a good idea to provide an example. He would work to release some model examples publicly on the IBIS website.

MAXIMUM FREQUENCY FOR S-PARAMETER MODEL USED IN CHANNEL SIMULATION

Masaki KIRINAKA (FICT Limited, Japan) (Start 01:27:00, Duration 38:00)

The presentation was given live. The following is an approximate translation of the presentation.

I am Kirinaka of FICT Corporation. I will give a presentation titled "Maximum Frequency for Sparameter Model used in Channel Simulation".

Slide 2:

The purpose of this presentation. Recently, when you try to perform a simulation, it has become very convenient to have most of the models available, connect the obtained models, and immediately start the simulation. If the waveform quality is OK, the analysis tends to be completed without checking each model's quality. Therefore, this time, in Channel Simulation using IBIS-AMI, we investigated whether each S-parameter model in the analog channel has data up to the frequency required for analysis. We also investigated how to deal with missing frequencies in S-parameter models.

Slide 3:

This is the analog channel for 28 Gbps NRZ transmission. From left to right, the transmitter IBIS-AMI, on-die S-parameter model, package S-parameter model, board S-parameter model, AC coupling capacitor S-parameter model, receiver package S-parameter model, on-die S-parameter model, and IBIS-AMI are connected in this order. Except for IBIS-AMI, the rest are composed of S-parameter models. We investigated whether the maximum frequency of each S-parameter model satisfied the required frequency in this analysis.

Slide 5:

First, determine the maximum frequency required for the analysis. It will be the bandwidth of the transmitter's output waveform. Here is a simulation circuit to find the bandwidth. A 100Ω termination resistor is connected to the transmitter on-die model of S-parameter, and a transient analysis is performed at a repetition frequency of 14 GHz Nyquist frequency of 28 Gbps NRZ. Here is the waveform observed at the termination resistor. The Fourier transform result is shown here, and it can be determined that the effective frequency, or bandwidth, that constitutes the transmitter output waveform is the third harmonic of 14 GHz, or up to 42 GHz. Therefore, to verify the response of the analog channel to this transmitter output waveform, the maximum frequency for each S-parameter model should be 42 GHz or higher.

Slide 6:

Using this maximum frequency of 42 GHz, we checked the analog channel for the 28 Gbps NRZ transmission mentioned earlier to see if the maximum frequency of each S-parameter model in

the configuration was sufficient. Only the S-parameter model of AC coupling capacitor had a maximum frequency below 10 GHz and did not reach 42 GHz. So, it is necessary to extrapolate to get that S-parameter model to be above 42 GHz.

Slide 7:

Extrapolation of the original S-parameter of the AC coupling capacitor was performed by the Sparameter model extraction function of the SI simulator. Here are the two S21 curves obtained for S-parameters above 42 GHz by extrapolation. The red curve is obtained by the extrapolation method that extends the maximum frequency point of the original S-parameter. Hereafter, it will be referred to as the constant extrapolation method. The blue curve is obtained by extrapolation by linearly connecting and extending several points around the maximum frequency of the original S-parameter. Hereafter, it will be referred to as the linear extrapolation method. The difference between the two methods at Nyquist frequencies of 14 GHz, 16 GHz, and 28 GHz for 28 Gbps, 32 Gbps, and 56 Gbps NRZ transmissions is shown in the figure. There is little difference at 14 and 16 GHz, but a large difference at 28 GHz. Which extrapolation method is closer to the actual S-parameters?

Slide 8:

Now, let's look at the difference between the two extrapolation methods using the eye diagram as well. The left column is based on the constant extrapolation method and the right column is based on the linear extrapolation method. As shown in the S21 comparison earlier, there is little difference in the eye waveforms for the 28Gbps and 32Gbps NRZs, but the eye opening is very different for the 56Gbps NRZ.

Slide 9:

We have verified which extrapolation method is closer to the measured S-parameter of the AC coupling capacitor by comparing them with the actual measurement results. As shown in the figure on the left, we obtained the measured S-parameter values by taking the difference between the measured S-para values of the wiring without the capacitor and that with the capacitor. The only difference between the two wirings is the presence or absence of the mounting pad portion of the capacitor. The right figure shows the measured S-parameter of both wirings. The red curve is SDD21 of the wiring without the capacitor, and the blue curve is SDD21 of the wiring with the capacitor.

Slide 10:

Before taking the difference in both S-parameters, we verified by simulation whether this difference was due to capacitor loss or the effect of the capacitor mounting pad. The simulation method was based on the original wiring model with capacitor mounting pads shown in Figure 1, the model shown in Figure 2, which was created by shorting the mounting pad section with a wiring conductor, and the original wiring model without capacitor mounting pads shown in Figure 3. The effect of the capacitor mounting pad was verified by comparing the S-parameter of the two models obtained by simulation. The right figure shows the S-parameters obtained by simulation. The red curve is the S-parameter of the wiring model without capacitor mounting pad in Figure 3, and the blue curve is the S-parameter of the wiring model with capacitor mounting pad shorted in Figure 2. Looking at these data, the difference between the two S-parameters becomes larger around 24 GHz, and it is assumed that the effect of the capacitor mounting pad begins to appear around this frequency. Therefore, we decided to use the measured S-parameter data up to 24 GHz to estimate the SDD21 of the capacitor.

Slide 11:

Here is the result of estimating the S-parameter of the capacitor using measured S-parameter up to 24 GHz. The red curve is the measured S-parameter of the wiring without capacitor, the blue curve is the measured S-parameter of the wiring with capacitor, and the difference between the two, or the S-parameter of the capacitor, is the gray curve. The S-parameter generated by obtaining an approximate formula from this gray curve and extrapolating above 24 GHz is the green dotted line.

Slide 12:

This graph plots the red curve based on the constant extrapolation method mentioned earlier, the blue curve based on the linear extrapolation method, and the green curve based on the approximation formula, or experimental formula, just obtained. Up to this point, the 28Gbps analysis has used S-parameter based on the linear extrapolation method. Comparing the linear extrapolation S-parameter with the S-parameter from the experimental formula, the two were close up to 14 GHz and 16 GHz, but at 42 GHz, the third harmonic of 14 GHz, the S-parameter of linear extrapolation showed higher loss by 1.4dB. As shown earlier, up to 28 Gbps and 32 Gbps, there was no difference in eye diagram for either the constant or linear extrapolation methods, but when the Nyquist frequency becomes 56 Gbps NRZ or 112 Gbps PAM4 at 32 GHz, the S-parameter of the linear extrapolation method is 0.5 dB larger loss than the S-parameter of the experimental formula. The simulation results are also expected to be worse. Therefore, it is our future challenge to find a way to extrapolate the S-parameter model of the AC coupling capacitor to match the S-parameter of the experimental formula and the S-parameter of the analysis accuracy.

Slide 13:

Finally, let me summarize. We investigated the frequency of each S-parameter model for the analog channel in the IBIS-AMI channel analysis. The S-parameter of the AC coupling capacitor was insufficient for the maximum frequency required for the analysis, so it was extrapolated by the simulator. Two different S-parameter models were generated by the extrapolation. Up to 32Gbps, there was almost no difference in eye diagram between the two extrapolated models. At 56 Gbps NRZ (Nyquist frequency of 28 GHz), there was a large difference in eye opening between the two models. So, we investigated which of the two S-parameter models was closer to the measured data. The results showed that neither of the two models matched the measured data exactly. Since only two S-parameter models can be obtained with the current extrapolation method, we need to find a way to extrapolate the original S-parameters to match the measured data in the future.

That concludes my presentation. Thank you for your kind attention.

Q&A session:

Ted Mido said: How we can extrapolate when the model does not cover the necessary frequency, like in this case to cover 28 or 56 Gbps, but the capacitor only covers to 10 GHz? Kirinaka-san is trying to cover this situation. Ted asked Randy and Bob for comments if they had encountered this situation. Randy commented that it is a difficult problem to solve, and he has not had much experience with solving this issue. Randy asked if Kirinaka-san always has an issue getting better capacitor models from vendors. He could ask for measurements to a larger bandwidth. Bob commented that this is a difficult problem. He is surprised that the empirical formula doesn't produce great results, and the best solution is to get measurements to a higher frequency.

SPIM (STANDARD PI MODEL) IN IBIS

Kinger CAI (Intel Corp., USA) Chi-te CHEN (Intel Corp., USA) [Presented by Kinger CAI (Intel Corp. USA)] (Start 02:11:00, Duration 23:15)

Synopsis: Presentation agenda as follows:

- Industry Platform PI Design Challenges
- Platform PI design Architecture Standardization
 - SPIM Standard Power Integrity Model
 - SPIM stimulus and target definition
 - FASTPI Platform PI design Framework
- Keywords definition for .spim file in BIRD
- One example .spim file
- FastPI Roadmap
- Next Steps

Q&A session:

Randy Wolff asked Kinger if he sees other companies besides Intel providing similar types of power integrity models. Kinger responded he sees other companies providing some much simpler ways with less information or less accurate ways to ask their customers to do platform PI signoff. The purpose is to provide a simple but more accurate way to help the platform designer by standardizing the communication and signoff methodology. There might be some inaccuracies that could lead to platform overdesign, but this wastes cost. They'd like to make cost-optimal designs for the performance target. From the customer side, they are also using the signoff methodology with other chipset vendors. The customers believe the Intel methodology is the most accurate and achieves the cost-optimal design, and they'd like it to be an industry standard to get similar data from other chipset vendors.

[PSIJ SENSITIVITY] IN IBIS

Kinger CAI (Intel Corp., USA) Fern Nee TAN (Intel Corp., USA) Chi-te CHEN (Intel Corp., USA) [Presented by Kinger CAI (Intel Corp. USA)] (Start 02:34:30, Duration 20:15)

Synopsis: Presentation agenda as follows:

- Background
- HSIO architecture: Serial & Parallel
- Status Quo, for jitter analysis
- New system jitter analysis methodology
- [PSIJ Sensitivity] in IBIS
- [PSIJ Sensitivity] application
- Next Steps

Q&A session:

Bob Ross commented that he thought this PSIJ sensitivity proposal would be addressed as a BIRD before SPIM since it is a simpler proposal.

OPEN DISCUSSION AND CLOSING REMARKS

(Start 02:55:00, Duration 22:00)

Randy asked if any participants were developing IBIS 7.0 models using IBIS 7.0 Interconnect Model syntax for modeling packages or on-die interconnect. Yoshitomi-san at Kioxia was considering making a model including IBIS-ISS. Randy commented that he sees many EDA tools supporting the syntax, so now is a good time for model makers to start creating these models.

Kobayashi-san asked: In PI simulation, is it possible to model the behavior of the current consumption of the die? Randy commented that Kinger's proposal for SPIM would be a new methodology for modeling the on-die power currents. Ted Mido asked if one would have to get the model from the chip vendor. Kinger said it gets back to basics. Intel invented IBIS to protect sensitive IP information. It is likely with any chip vendor that they won't provide the detailed Icc(t) profiles at the transistor level. So, if you want to calculate the power, what will be provided is the summed Vcc current and voltage so you can calculate the DC power, and Intel will provide the max current. This helps you design the voltage regulator.

Kinger noted that for the SPIM model, it can cover anything the chip vendor will provide. The template is there, starting with frequency domain. The strategy is that the detailed on-die PI and package design has been well taken care of by the chip vendor. At the platform level, you only need to take care of up to a certain frequency within the design target. The chip vendor can guarantee the voltage waveform at the transistor level is good to meet the committed performance in terms of IO rail noise impact.

Ted asked what a system designer can get, such as max voltage variation as a single number, but can you get a PWL source that mimics the power rail voltage and current. Kinger said, conversely, you should ask what you need the detailed Icc profile for. If the chip vendor gives you that current profile, then they also need to provide the on-die power grid model and on-die cap information. Then you'd ask what the Vmin at the transistor level is. This is sensitive information that the chip vendor doesn't want to provide. For the system level, all the on-die and package design is already completed. You will have no impact from the platform level to the package and silicon level.

Ted asked what information the system designer can get with further inquiry. Kinger said that for DC you get the Icc max and average. This is more for reliability issues, ensuring the currents are relatively balanced through the BGA balls, otherwise the worst BGA ball will melt down. SPIM provides the current information at the bump level. Also, AC simulation tells you weighting at the stimulus ports to tell you locations with heavy or light loading in the circuit blocks. Use this unbalanced AC source to run AC simulations in frequency domain to meet the impedance target at the observation port.

Kinger added that originally no chip vendor would provide a chip-level model, and IBIS came out of that circumstance. Now there are S-parameters for package models extending the traditional IBIS model. SPIM is similar, providing the AC source at the bump-level and the S-parameter from bump to BGA to help customers do the platform level PI design. Ted summarized that SPIM is providing a model that is accurate enough for the need. Randy Wolff thanked everyone for attending the 17th IBIS Summit for Japan. He noted excellent presentations and good discussion. He thanked the presenters and JEITA for the excellent hosting. He looked forwarding to meeting again next year, hopefully in person. He noted people could reach out to him in person with any questions.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held on November 18, 2022. The following IBIS Open Forum teleconference meeting is tentatively scheduled for December 9, 2022.

NOTES

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- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/ http://www.ibis.org/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/ http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/ http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS (attendee X; absent -)

		Standards Ballot				
	Interest	Voting	Sept. 30.	Oct. 21.	Nov. 4.	Nov. 11.
Organization	Category	Status	2022	2022	2022	2022
AMD (Xilinx)	Producer	Inactive	-	-	-	-
Analog Devices (Maxim	Producer	Inactive	-	-	-	-
Integrated)	User	A	X	X		Y
ANSYS	User	Active	Х	Х	-	х
Applied Simulation Technology	User	Inactive	-	-	-	-
Aurora System	User	Inactive	-	-	-	Х
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Inactive	Х	-	-	Х
Celestica	User	Inactive	-	-	-	-
Cisco Systems	User	Inactive	-	-	-	-
Dassault Systemes	User	Inactive	-	-	-	-
Google	User	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	Х	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Instituto de Telecomunicações	User	Inactive	-	-	-	-
Intel Corp.	Producer	Active	Х	Х	Х	Х
Keysight Technologies	User	Inactive	-	-	-	Х
Luminous Computing	General Interest	Inactive	-	-	-	-
Marvell	Producer	Inactive	-	Х	-	-
MathWorks	User	Inactive	Х	Х	-	-
Micron Technology	Producer	Active	Х	Х	Х	Х
MST EMC Lab	User	Inactive	-	-	Х	-
SerDesDesign.com	User	Inactive	-	-	-	-
Siemens EDA (Mentor)	User	Active	Х	Х	-	Х
STMicroelectronics	Producer	Inactive	Х	Х	-	-
Svnopsvs	User	Active	Х	Х	Х	х
Teraspeed Labs	General Interest	Active	Х	Х	Х	х
Waymo	User	Inactive	Х	Х	-	-
ZTE Corp.	User	Inactive	-	-	х	-
Zuken	User	Active	Х	Х	Х	Х

= Temporarily not a voting member

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership •
- Membership dues current
- Must not miss two consecutive meetings (voting by email counts as attendance) Interest categories associated with SAE standards ballot voting are:

 - Users members that utilize electronic equipment to provide services to an end user. •
 - Producers members that supply electronic equipment. •
 - General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations, and associations, and/or consumers.