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Investigate EMD model specification

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The Future is Interconnected

Agenda

- Motivation
- What is EMD?
- EMD FILE STRUCTURE
- Understand EMD through IBIS V7.2 examples
- Improvements from EBD model to EMD model
- Summary

Motivation

- We think there will be opportunities to use EMD models in the future.
- Therefore, this time, We tried to understand the EMD model specifications.
- We also considered the advantages over conventional EBD based on EMD specifications.

What is EMD?

- EMD is an abbreviation for Electrical Module Description.
- IBIS standard for modeling modules such as DIMMs.
- Added from IBIS V7.1 (ratified on December 10, 2021)
- Can analyze more electrical problems than EBD (traditional module description).
- Consists of two types of files (XXX.emd, YYY.ems)
  (YYY.ems may not exist.)

EMD FILE STRUCTURE

EMD File

.emd FILE
- File Header Section
  - **[IBIS Ver]**
  - **[Comment Char]**
  - **[File Name]**
  - **[File Rev]**
  - **[Date]**
  - **[Source]**
  - **[Notes]**
  - **[Disclaimer]**
  - **[Copyright]**
- **[Begin EMD]**
  - **[Manufacturer]**
  - **[Description]**
  - **[Number of EMD Pins]**
  - **[EMD Pin List]** signal_name, signal_type, bus_label
    - **[End EMD Pin List]**
  - **[EMD Parts]**
    - **[End EMD Parts]**
  - **[EMD Designator List]**
    - **[End EMD Designator List]**
  - **[Designator Pin List]** signal_name, signal_type bus_label
    - **[End Designator Pin List]**
  - **[Voltage List]**
    - **[End Voltage List]**
  - **[EMD Group]**
    - **[End EMD Group]**
  - **[End EMD]**

The EMD Set may or may not be inside XXX.emd.
EMD Set is a collection of module wiring models.

- **[EMD Set]**
  - **[Manufacturer]**
  - **[Description]**
  - **[EMD Model]** Param, File_TS, File_IBIS-ISS, Unused_port_termination, Number_of_terminals
    - **[End EMD Model]**
  - **[End EMD Set]**
- **[End]**

EMS File

.ems FILE
- File Header Section
  - **[IBIS Ver]**
  - **[Comment Char]**
  - **[File Name]**
  - **[File Rev]**
  - **[Date]**
  - **[Source]**
  - **[Notes]**
  - **[Disclaimer]**
  - **[Copyright]**
- **[EMD Set]**
  - **[Manufacturer]**
  - **[Description]**
  - **[EMD Model]** Param, File_TS, File_IBIS-ISS, Unused_port_termination, Number_of_terminals
    - **[End EMD Model]**
  - **[End EMD Set]**
- **[End]**

Understand EMD through IBIS V7.2 examples

IBIS V7.2 provides an example of EMD modeling for DDR4 RDIMM address net.
Using this example, I tried to understand the EMD model.

RDIMM FIGURES FOR EXAMPLES IN 13.5.2 THROUGH 13.5.4

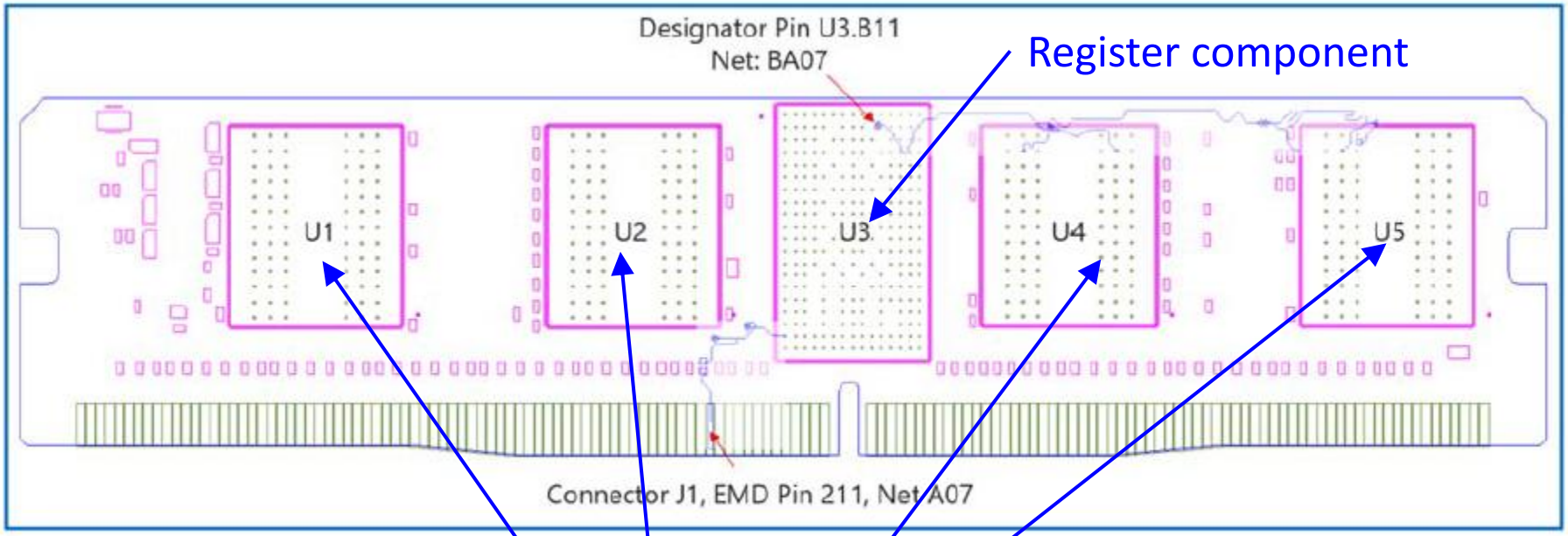


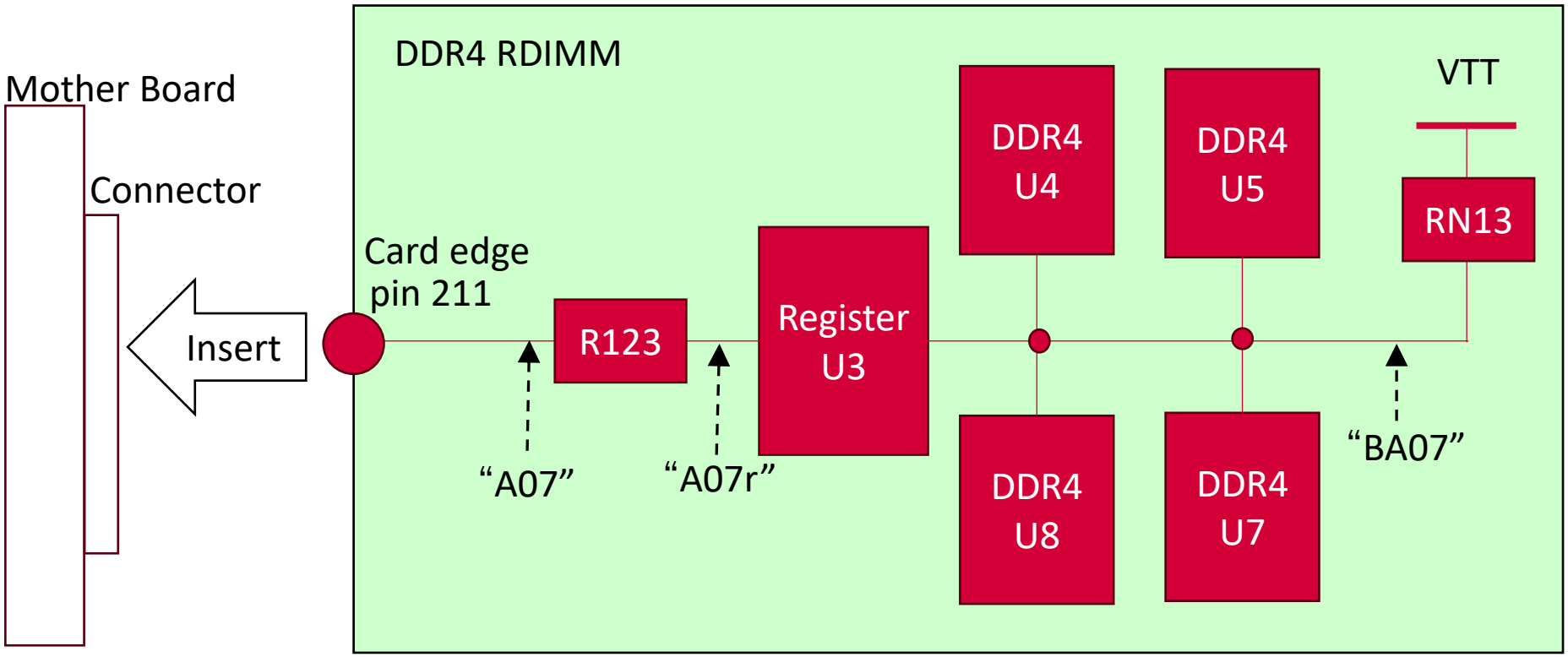
Figure 55 – DDR4 Registered DIMM with Labeling

DRAM components (back side U7-U11)

Understand EMD through IBIS V7.2 examples

Block diagram of EMD (ELECTRICAL MODULE DESCRIPTION) part

Address line “A7”



Understand EMD through IBIS V7.2 examples

Modeling part in DIMM : Extended Net

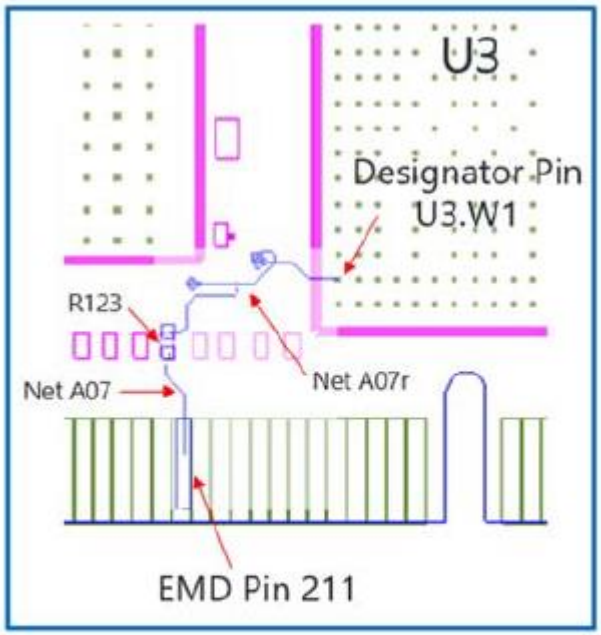
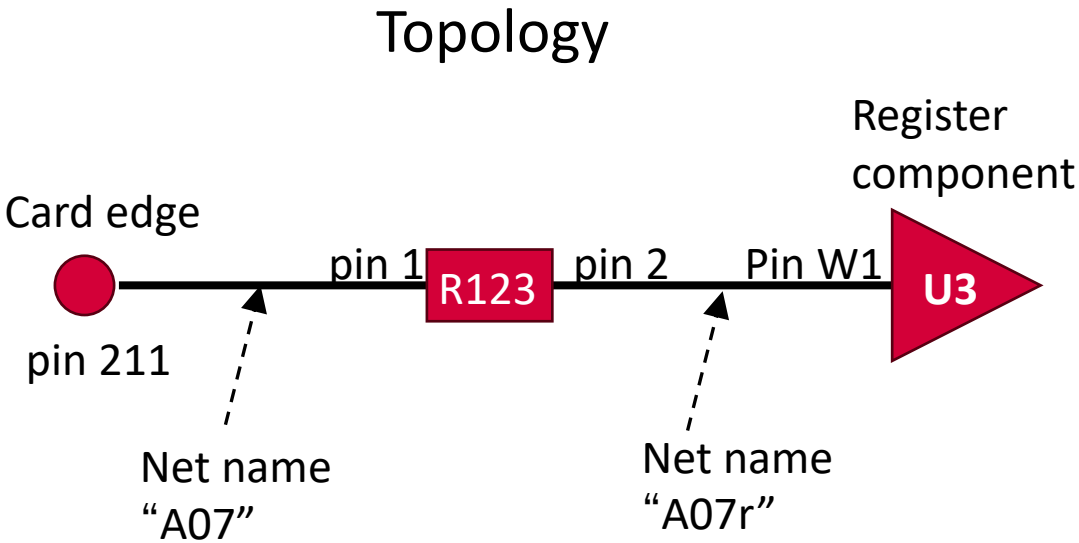


Figure 56 – Extended Net



Understand EMD through IBIS V7.2 examples

Modeling part in DIMM : Internal Net

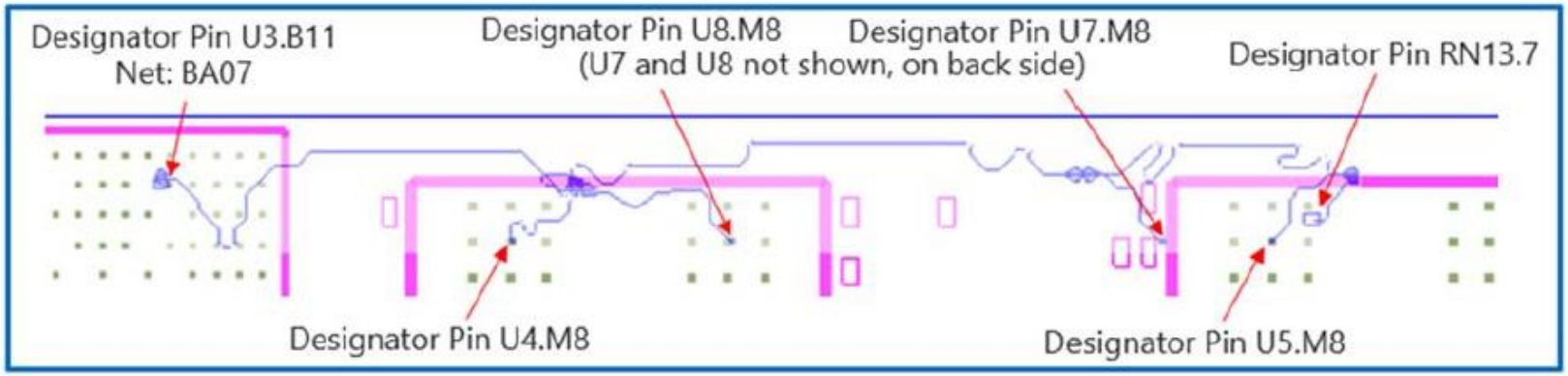
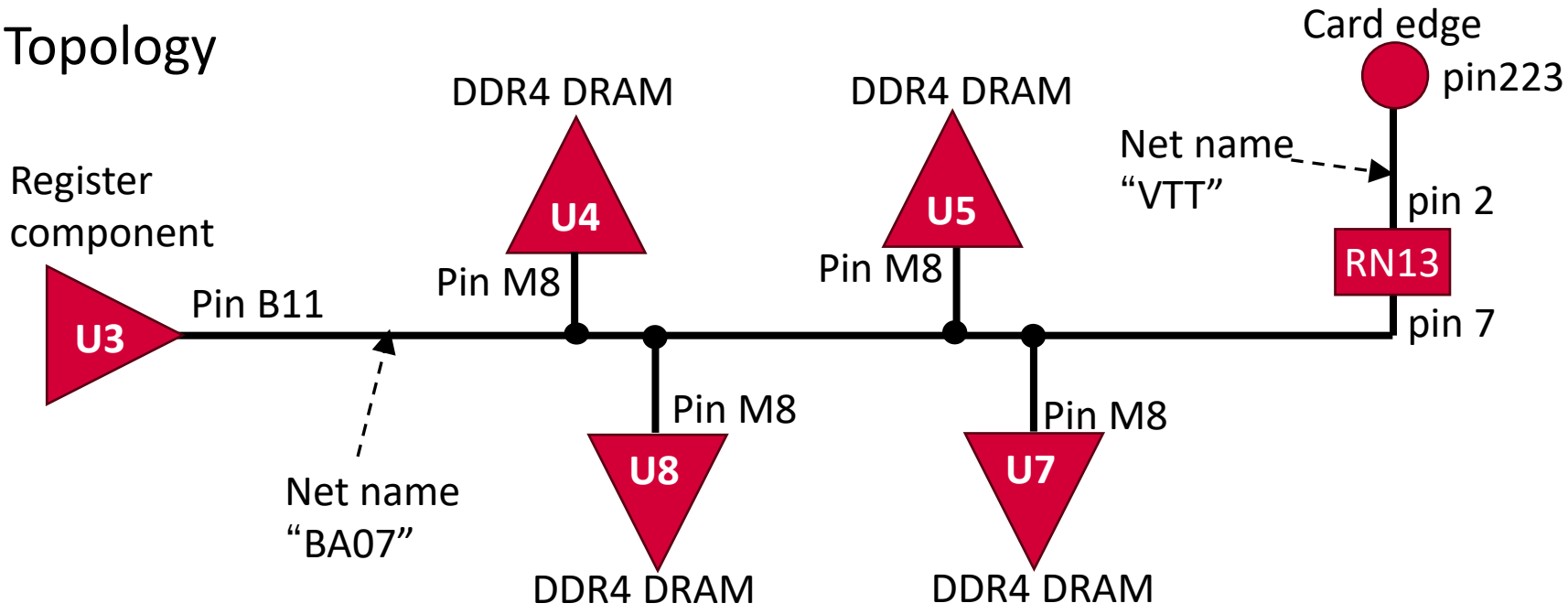


Figure 57 – Internal Net

Topology

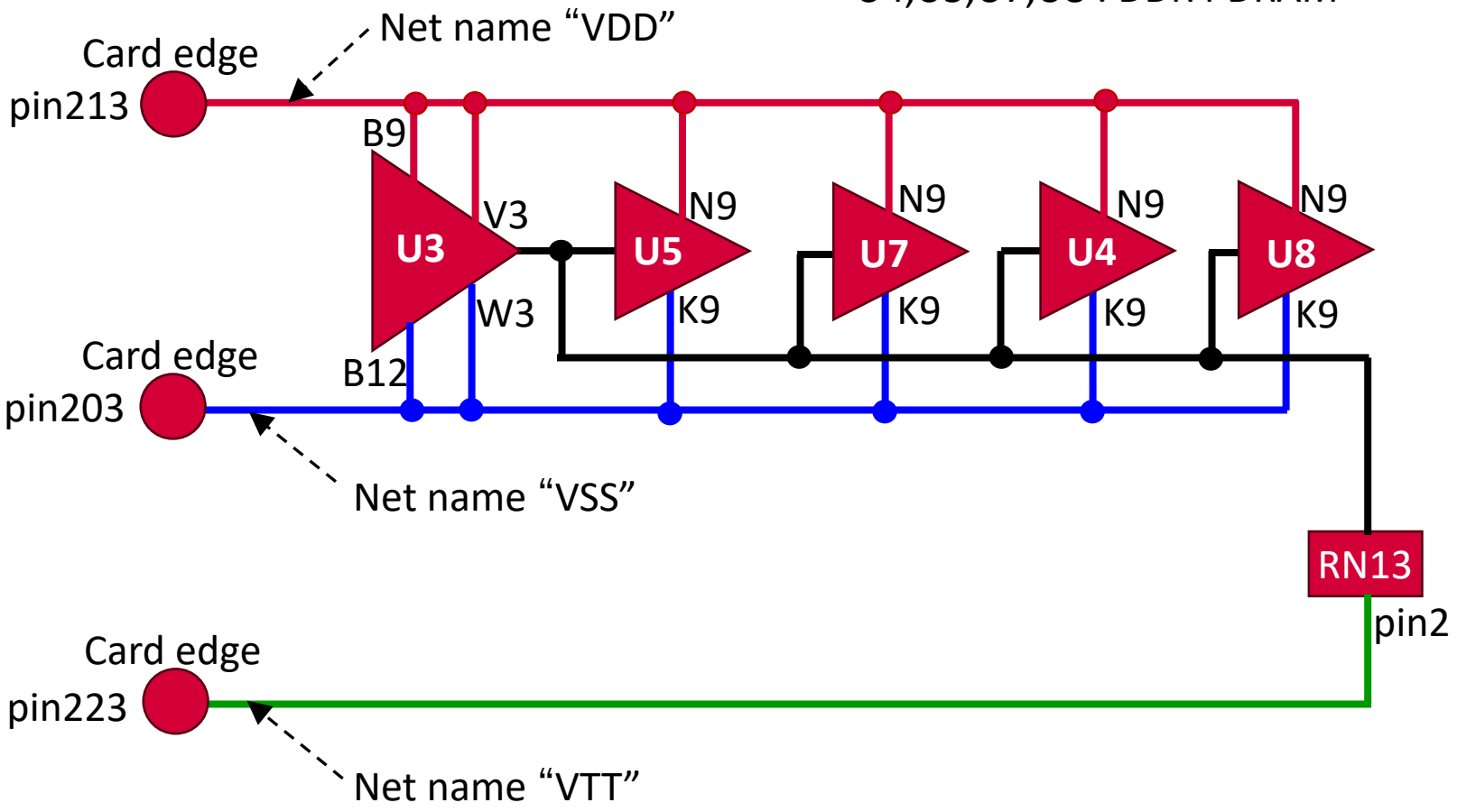


Understand EMD through IBIS V7.2 examples

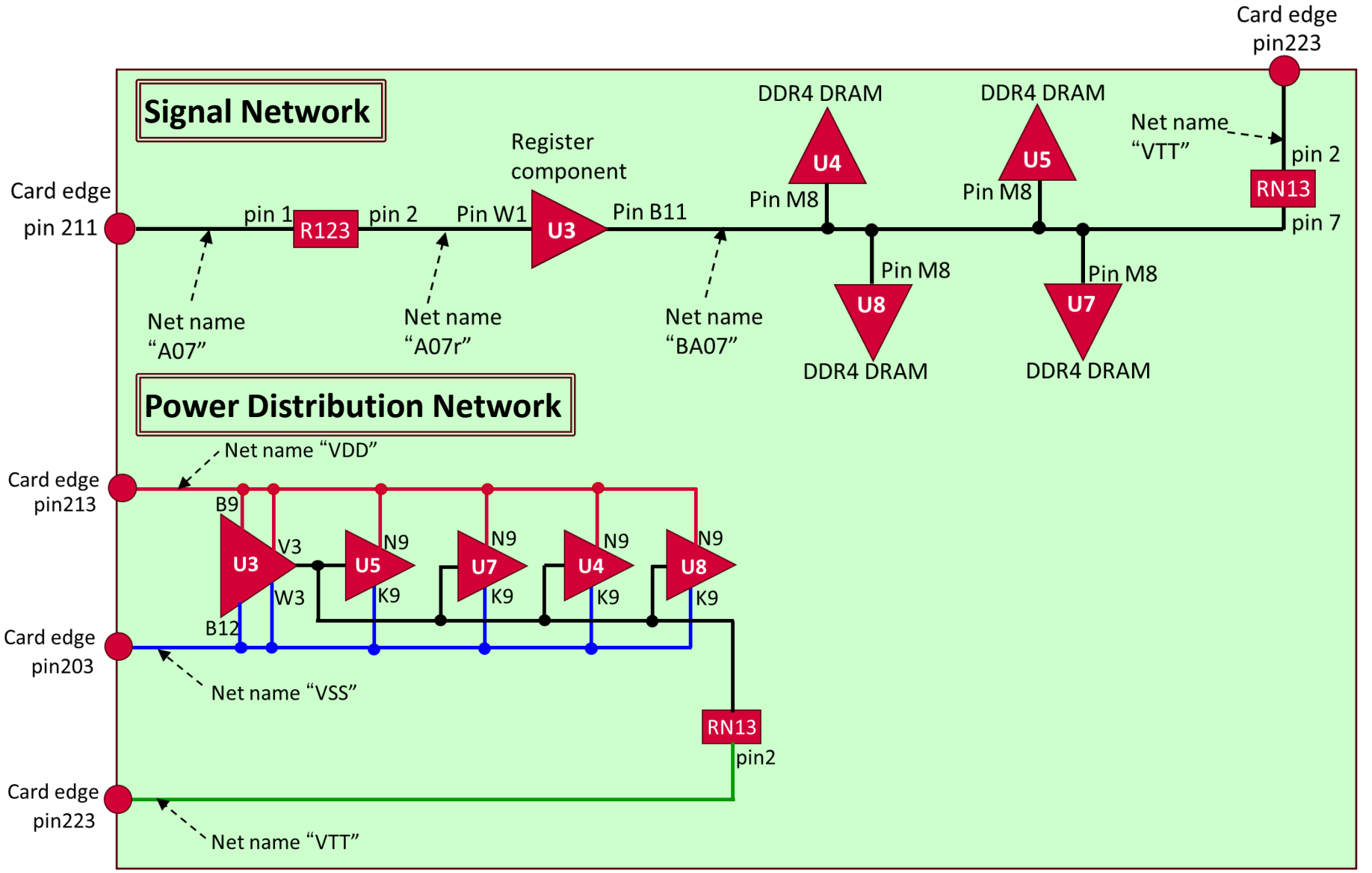
Modeling part in DIMM : Power Distribution Network

Topology

U3：Register component
U4,U5,U7,U8 : DDR4 DRAM



Understand EMD through IBIS V7.2 examples



Understand EMD through IBIS V7.2 examples

13.5.2 EXAMPLE 1 (R123 AND RN13 EMBEDDED IN A07_1 AND BA07_1)

```
|************************************************************
| EMD Syntax Example 1 (Net A07 with Embedded Resistors)
| Using DDR4 RDIMM Example
[Begin EMD] DDR4_RDIMM_1
[Number of EMD Pins] 4
[EMD Pin List] signal_name signal_type bus_label
203 VSS GND
211 A07
212 VDD POWER VDD1
223 VTT POWER
[End EMD Pin List]
[EMD Parts]
DDR4_Reg_253b register.ibs DDR4_Register
DDR4_x8_78b dram.ibs DDR4_8Gb_x8
[End EMD Parts]
[EMD Designator List]
U3 DDR4_Reg_253b
U4 DDR4_x8_78b
U5 DDR4_x8_78b
U7 DDR4_x8_78b
U8 DDR4_x8_78b
[End EMD Designator List]
[Designator Pin List] signal_name signal_type bus_label
U3.B9 VDD POWER VDD1
U3.B11 BA07
U3.B12 VSS GND
U3.V3 VDD POWER VDD1
U3.W1 A07
U3.W3 VSS GND
|
U4.K9 VSS GND
U4.M8 BA07
U4.N9 VDD POWER VDD1
|
U5.K9 VSS GND
U5.M8 BA07
U5.N9 VDD POWER VDD1
|
U7.K9 VSS GND
U7.M8 BA07
U7.N9 VDD POWER VDD1
|
U8.K9 VSS GND
U8.M8 BA07
U8.N9 VDD POWER VDD1
[End Designator Pin List]
[Voltage List]
VDD 1.200 1.140 1.260
VSS 0.000 0.000 0.000
VTT 0.600 0.570 0.630
[End Voltage List]
[EMD Group] Addr_07_Group_1
Addr_07_1 NA
[End EMD Group]
[End EMD]
[EMD Set] Addr_07_1
[Manufacturer] NoName Corp.
[EMD Model] A07_1
File_IBIS-ISS A07.iss A07_1
Number_of_terminals = 6
1 Pin_I/O pin_name 211
2 Pin_I/O pin_name U3.W1 | Connection from 211 to U3.W1 includes
| Series Resistor modeled in A07.iss A07_1
3 Pin_Rail bus_label VDD1
4 Pin_Rail signal_name VSS
5 Pin_Rail bus_label U3.VDD1
6 Pin_Rail bus_label U3.VSS
[End EMD Model]
[EMD Model] BA07_1
File_IBIS-ISS A07.iss BA07_1
Number_of_terminals = 18
1 Pin_I/O pin_name U3.B11
2 Pin_Rail bus_label U3.VDD1
3 Pin_Rail signal_name U3.VSS
4 Pin_I/O pin_name U4.M8
5 Pin_Rail bus_label U4.VDD1
6 Pin_Rail signal_name U4.VSS
7 Pin_I/O pin_name U5.M8
8 Pin_Rail bus_label U5.VDD1
9 Pin_Rail signal_name U5.VSS
10 Pin_I/O pin_name U7.M8
11 Pin_Rail bus_label U7.VDD1
12 Pin_Rail signal_name U7.VSS
13 Pin_I/O pin_name U8.M8 | Termination Resistor to VTT
| included in A07.iss BA07_1
14 Pin_Rail bus_label U8.VDD1
15 Pin_Rail signal_name U8.VSS
16 Pin_Rail bus_label VDD1
17 Pin_Rail signal_name VTT
18 Pin_Rail signal_name VSS
[End EMD Model]
[End EMD Set]
|************************************************************
```

Understand EMD through IBIS V7.2 examples

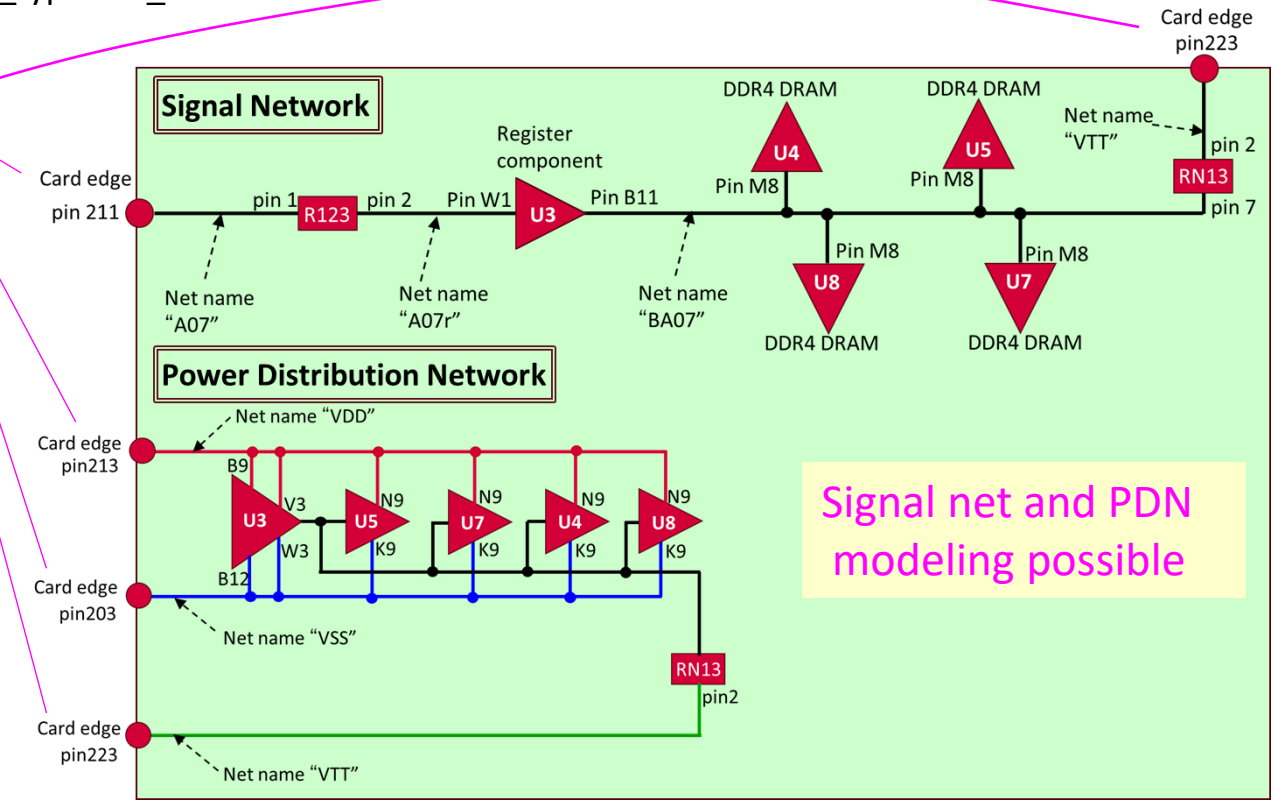
13.5.2 EXAMPLE 1 (R123 AND RN13 EMBEDDED IN A07_1 AND BA07_1)
|**********
| EMD Syntax Example 1 (Net A07 with Embedded Resistors)
| Using DDR4 RDIMM Example

Define pins to connect the module to other external boards.

[Begin EMD] DDR4_RDIMM_1
[Number of EMD Pins] 4
[EMD Pin List] signal_name signal_type bus_label
203 VSS GND
211 A07
212 VDD POWER VDD1
223 VTT POWER
[End EMD Pin List]

Pin Name
Net Name
VG Type
Bus Label

Reserved Model Name
- POWER
- GND
- NC



Signal net and PDN modeling possible

Understand EMD through IBIS V7.2 examples

```
[EMD Parts]
DDR4_Reg_253b  register.ibs  DDR4_Register
DDR4_x8_78b    dram.ibs      DDR4_8Gb_x8
[End EMD Parts]
```

Parts Name

IBIS file (,EMD file)

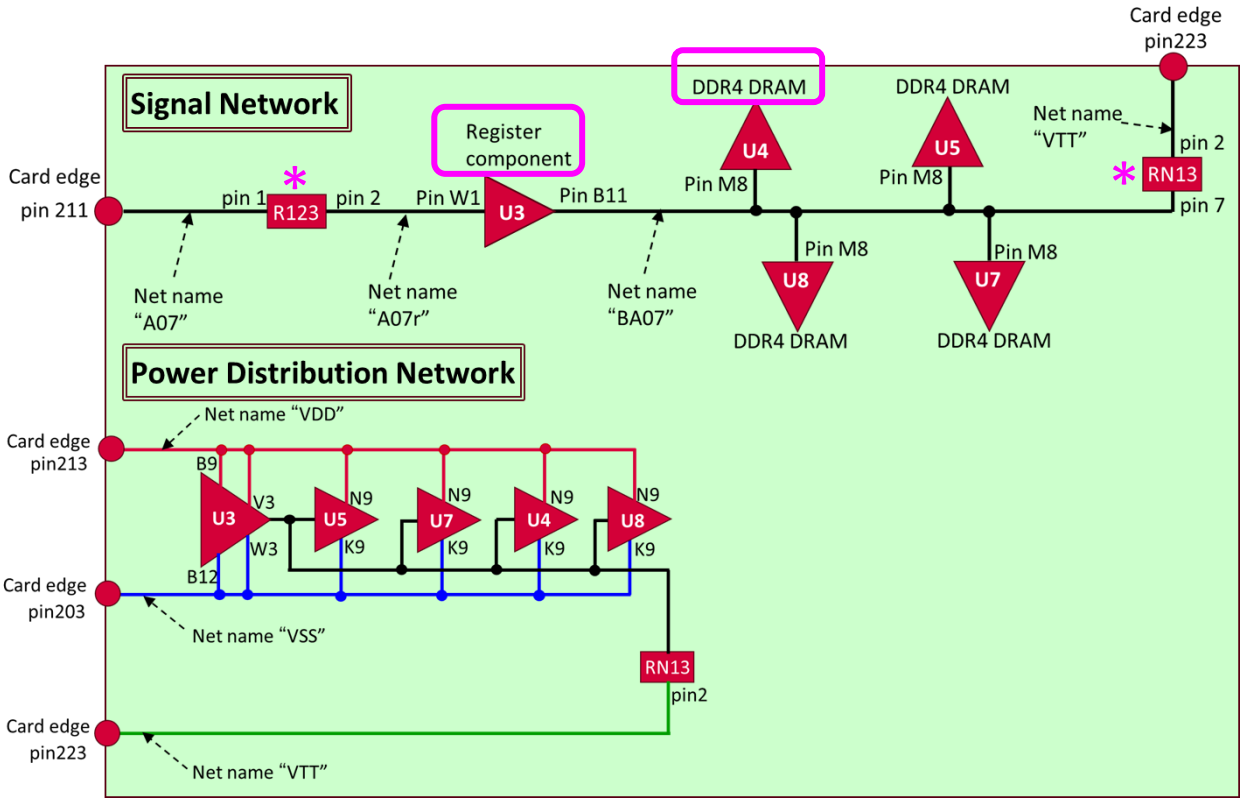
Component Name

*In this example, resistors R123 and RN13 are included in the wiring model, so there is no IBIS definition.

```
[EMD Designator List]
U3        DDR4_Reg_253b
U4        DDR4_x8_78b
U5        DDR4_x8_78b
U7        DDR4_x8_78b
U8        DDR4_x8_78b
[End EMD Designator List]
```

Parts No.

Parts Name

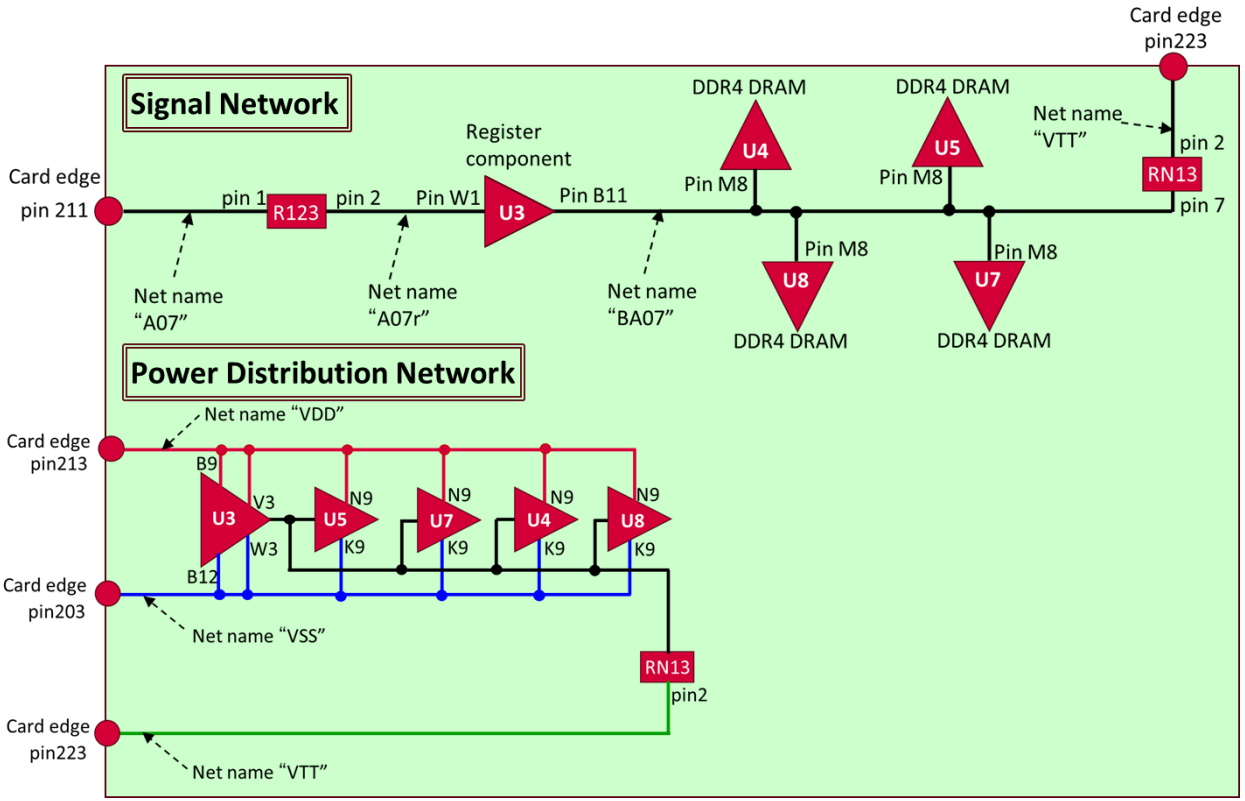


Understand EMD through IBIS V7.2 examples

```
[Designator Pin List] signal_name signal_type bus_label
U3.B9     VDD   POWER VDD1
U3.B11    BA07
U3.B12    VSS   GND
U3.V3     VDD   POWER VDD1
U3.W1     A07
U3.W3     VSS   GND
|
U4.K9     VSS   GND
U4.M8     BA07
U4.N9     VDD   POWER VDD1
|
U5.K9     VSS   GND
U5.M8     BA07
U5.N9     VDD   POWER VDD1
|
U7.K9     VSS   GND
U7.M8     BA07
U7.N9     VDD   POWER VDD1
|
U8.K9     VSS   GND
U8.M8     BA07
U8.N9     VDD   POWER VDD1
[End Designator Pin List]
```

Parts No. | Pin Name | Net Name | VG Type | Bus Label

Define connections between elements inside the module.



Understand EMD through IBIS V7.2 examples

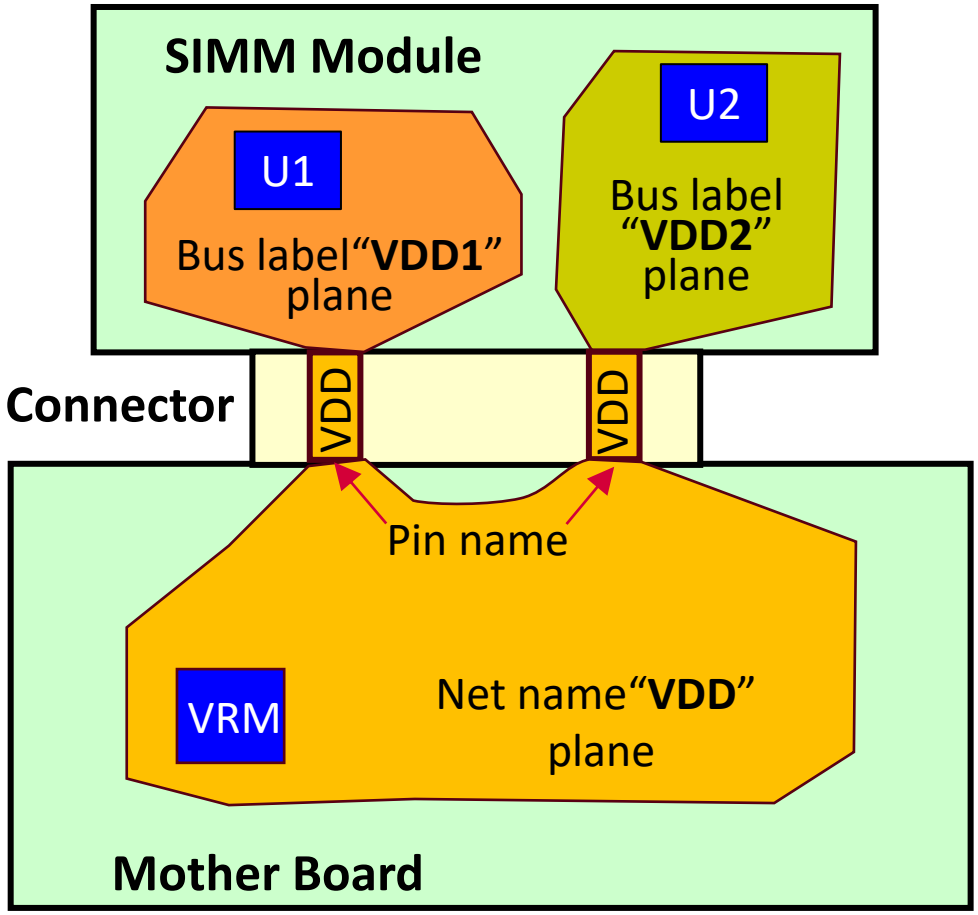
Example:
| A SIMM Module Example:
|
[Begin EMD] 16X8_SIMM
[Manufacturer] NoName Corp.
[Number Of EMD Pins] 6
[EMD Pin List] signal_name signal_type bus_label
A1 VSS GND
A2 DQ1
A3 DQ2
A4 VDD POWER VDD1
A5 VDD POWER VDD2
A6 VDDQ POWER
[End EMD Pin List]
[Designator Pin List] signal_name signal_type bus_label
U1.11 VSS GND
U1.12 DQ1
U1.13 DQ2
U1.14 VDD POWER VDD1
U2.21 VDD POWER VDD2
U2.22 DQ1
U2.23 DQ2
U2.24 VDDQ POWER
[End Designator Pin List]

Net Name

Bus Label

Questions about how to use bus labels

Is the image below the correct way to use the bus label?



VRM : Voltage Regulator Module

Understand EMD through IBIS V7.2 examples

```
[Voltage List]
VDD 1.200 1.140 1.260
VSS 0.000 0.000 0.000
VTT 0.600 0.570 0.630
[End Voltage List]
```

Specify the voltage level of power supply and GND.

```
[EMD Group] Addr_07_Group_1
Addr_07_1 NA
[End EMD Group]
[End EMD]
```

The module wiring model aggregate name (EMD set name) is listed.

EMD Set Name

Path of EMD set file (YYY.ems).
"NA" if the EMD. Set is in XXX.emd.

Understand EMD through IBIS V7.2 examples

```
[EMD Set] Addr_07_1
[Manufacturer] NoName Corp.
```

Define EMD set name.
Models included in the set.
- No.1 A07_1
- No.2 BA07

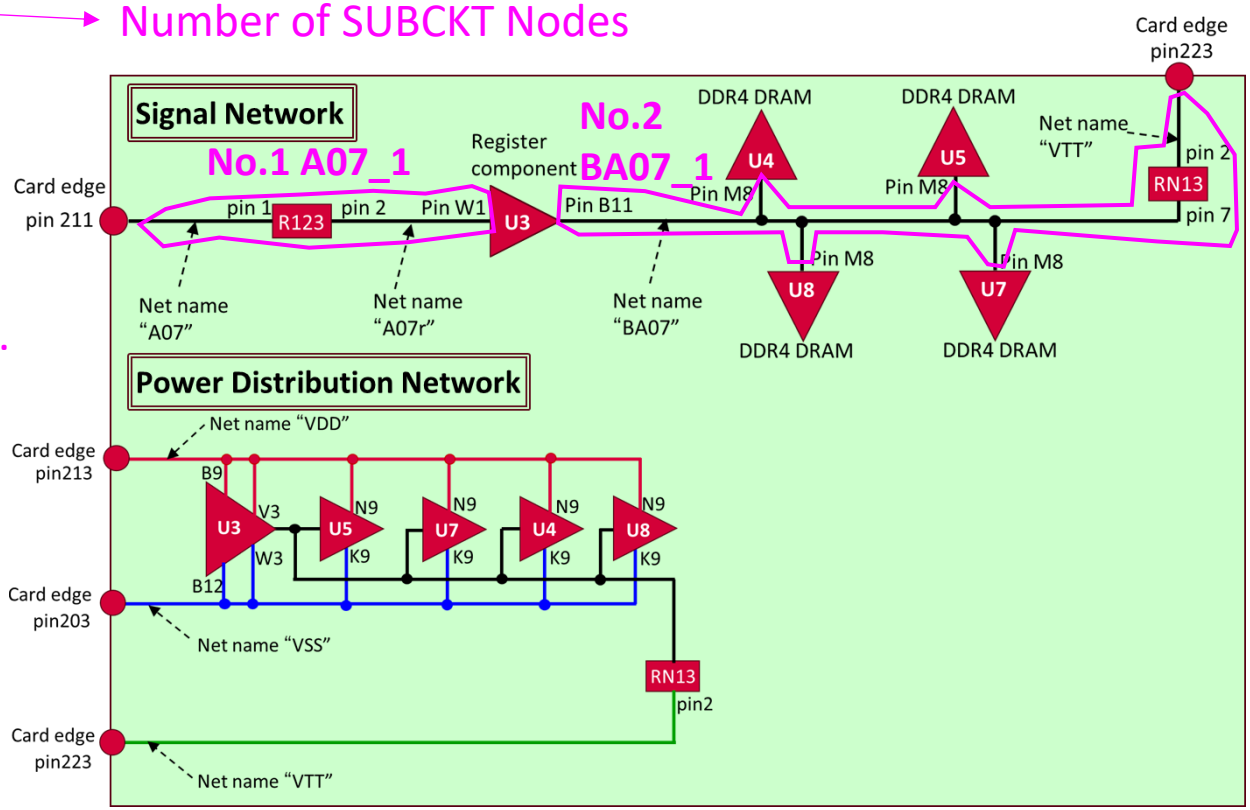
Defining EMD model No.1 A07_1.

```
[EMD Model] A07_1
File_IBIS-ISS A07.iss A07_1

Number_of_terminals = 6

| Connection from 211 to U3.W1
| includes Series Resistor
| modeled in A07.iss A07_1
```

Model format: IBIS-ISS, model file name, SUBCKT name

Number of SUBCKT Nodes

- Multi-Line model can be used.
- Touchstone model format can also be used.
  Subparameter "File_TS"



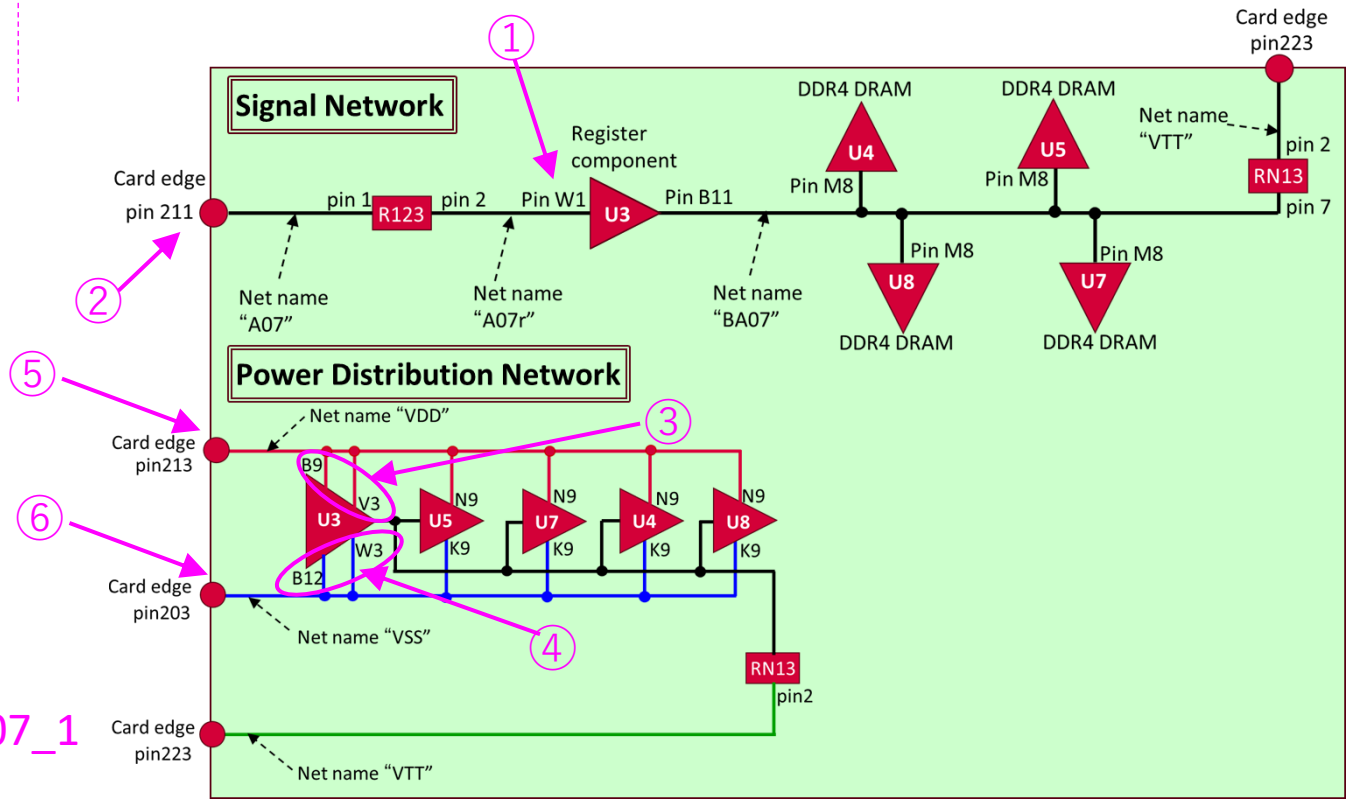
Understand EMD through IBIS V7.2 examples

Subckt Node No.

Subckt Node's net position

1	Pin_I/O	pin_name	211 → ②
2	Pin_I/O	pin_name	U3.W1 → ①
3	Pin_Rail	bus_label	VDD1 → Is the node position ⑤?
4	Pin_Rail	signal_name	VSS → Is the node position ⑥?
5	Pin_Rail	bus_label	U3.VDD1 → Is the node position around ③?
6	Pin_Rail	bus_label	U3.VSS → Is the node position around ④?

Node Type
Pin_I/O : Sig
Pin_Rail : Pow, GND



[End EMD Model]

End of EMD model No.1 A07_1 definition.

Understand EMD through IBIS V7.2 examples

```
[EMD Model] BA07_1
File_IBIS-ISS A07.iss BA07_1
Number_of_terminals = 18
1 Pin_I/O pin_name U3.B11
2 Pin_Rail bus_label U3.VDD1
3 Pin_Rail signal_name U3.VSS
4 Pin_I/O pin_name U4.M8
5 Pin_Rail bus_label U4.VDD1
6 Pin_Rail signal_name U4.VSS
7 Pin_I/O pin_name U5.M8
8 Pin_Rail bus_label U5.VDD1
9 Pin_Rail signal_name U5.VSS
10 Pin_I/O pin_name U7.M8
11 Pin_Rail bus_label U7.VDD1
12 Pin_Rail signal_name U7.VSS
13 Pin_I/O pin_name U8.M8
| Termination Resistor to VTT
| included in A07.iss BA07_1
14 Pin_Rail bus_label U8.VDD1
15 Pin_Rail signal_name U8.VSS
16 Pin_Rail bus_label VDD1
17 Pin_Rail signal_name VTT
18 Pin_Rail signal_name VSS
[End EMD Model]
```

Defining EMD model No.2 **BA07_1.**

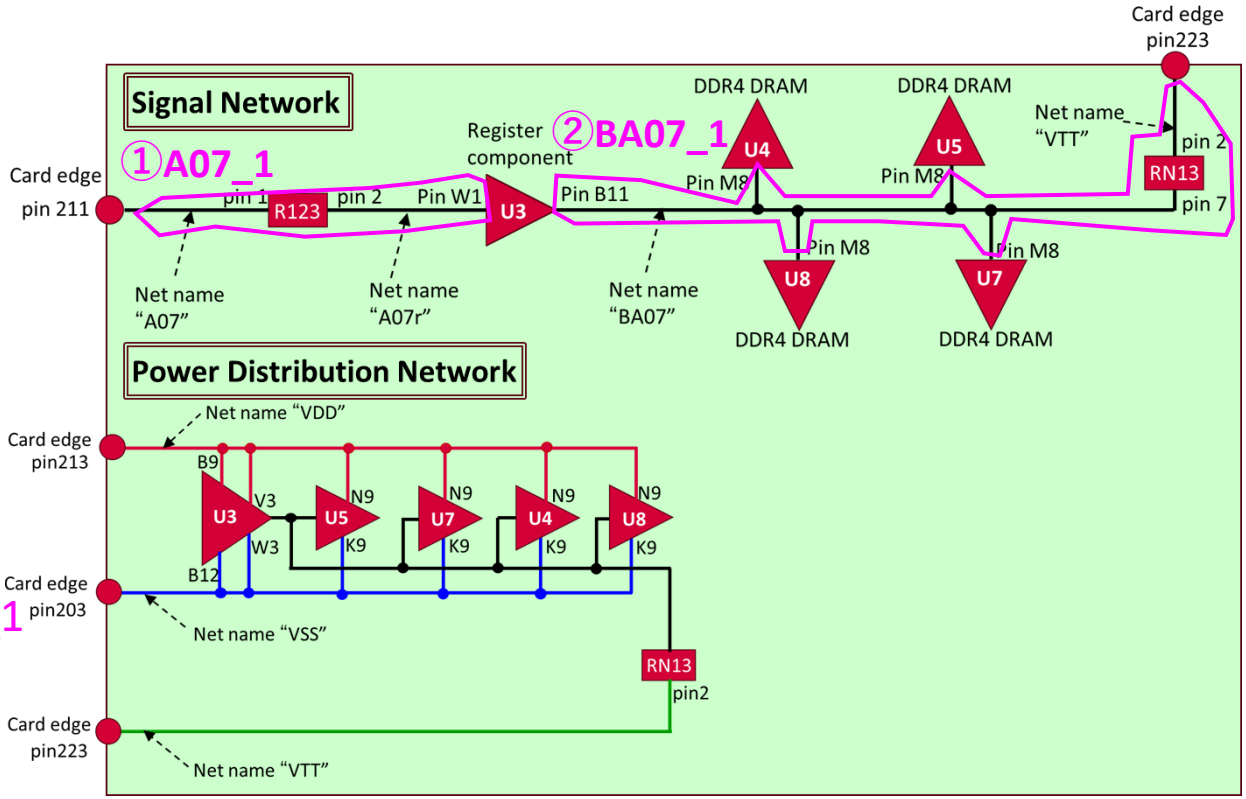
Model format: IBIS-ISS, model file name, SUBCKT name

Number of SUBCKT Nodes

End of EMD model No.2 BA07_1 definition.

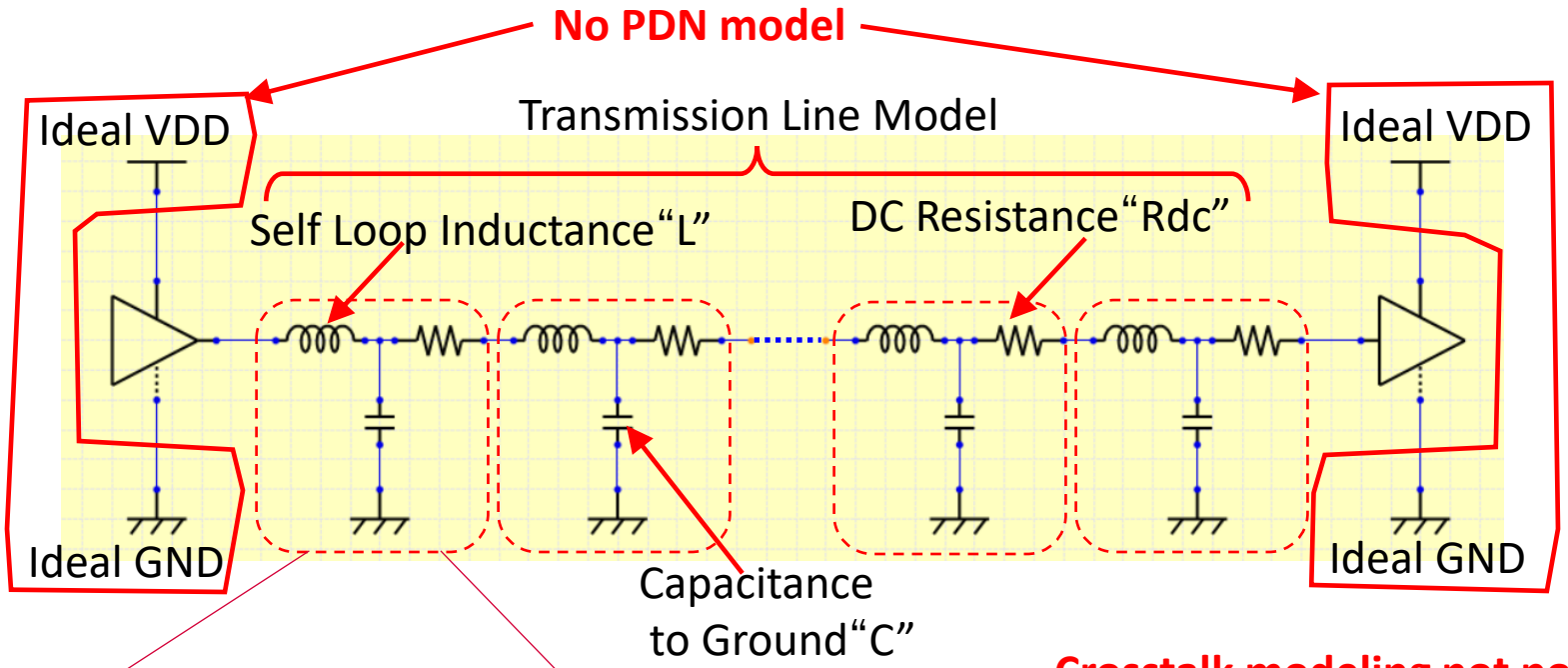
```
[End EMD Set]
|*****************************
```

End of EMD set definition

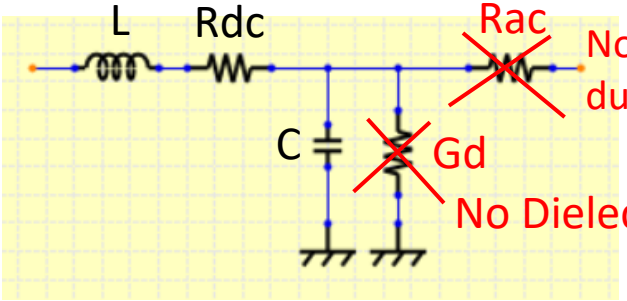


Improvements from EBD model to EMD model

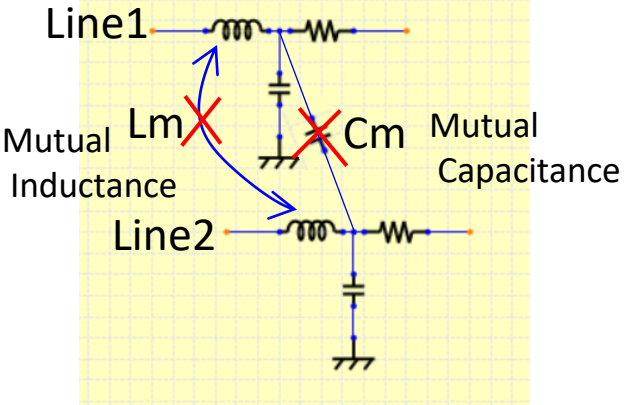
Modeling Electrical Modules using EBD



No High Frequency Loss



Crosstalk modeling not possible

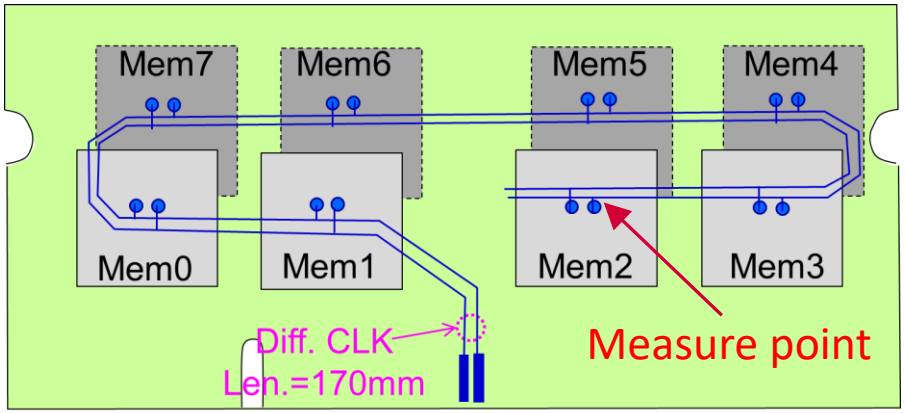


Improvements from EBD model to EMD model

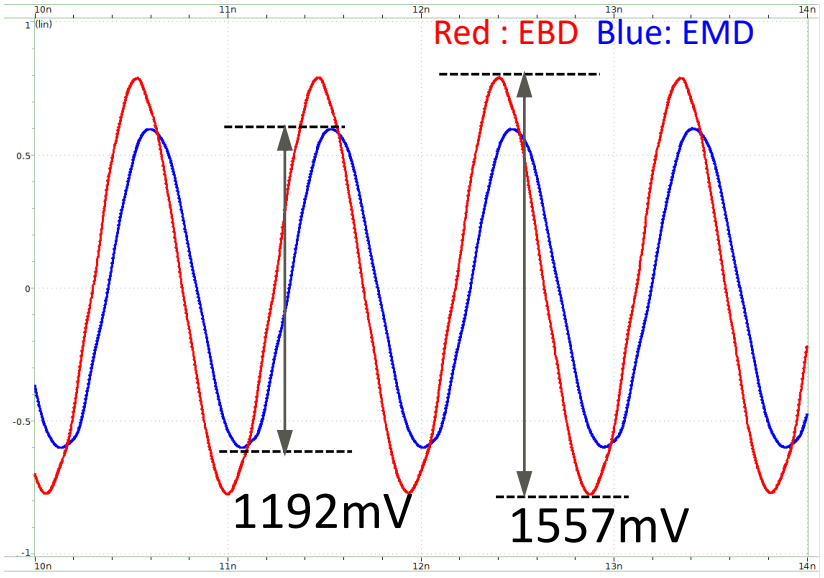
EMD model can be modeled with IBIS-ISS (Rs, Gd of W-element) and Touchstone, so high frequency loss model is possible.

Example
[DDR4 SODIMM] Waveform comparison:
Line Model with LCR only (=EBD) vs. Line Model with Skin-Effect and Dielectric Loss (=EMD)

DDR4 Unbuffered SO-DIMM Raw Card A
2666Mbps (CLK freq.=1333MHz)



Differential CLK Waveform at Mem2



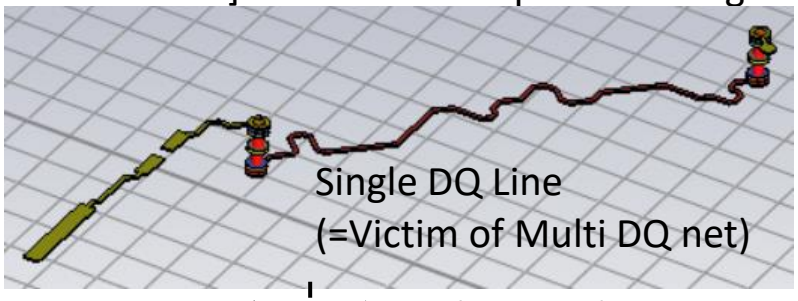
Line Model with LCR only (=EBD)
Line Model with Skin-Effect and Dielectric Loss (=EMD)
} 23% Difference!!

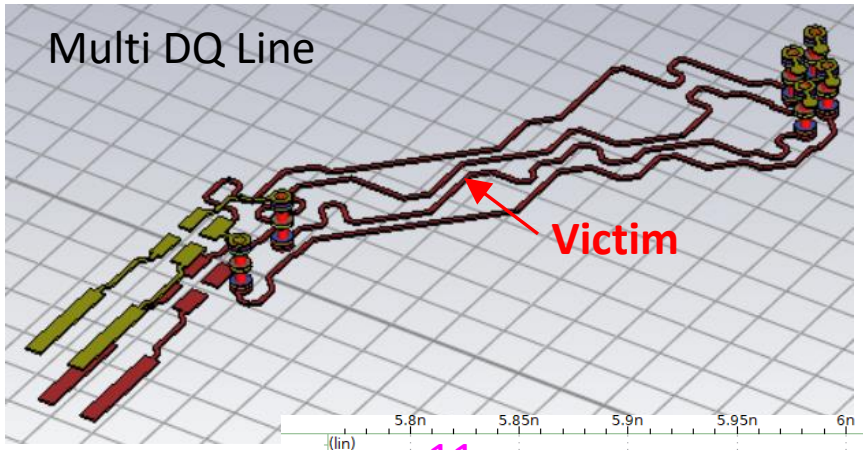
Improvements from EBD model to EMD model

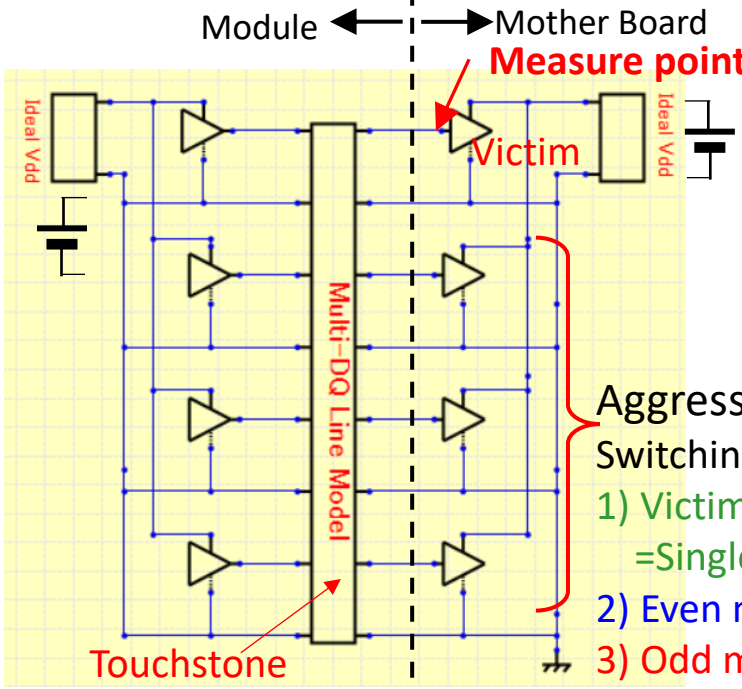
EMD model can model Multi-Line using IBIS-ISS (W-element) and Touchstone, so crosstalk modeling is possible.

Example

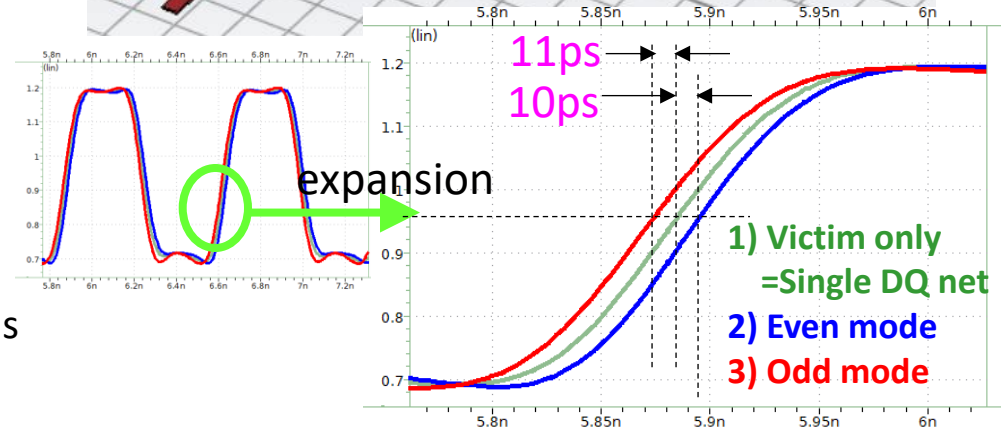
[DDR4 SODIMM] Waveform comparison: Single Line Model (=EBD) vs. Multi-Line Model (=EMD)







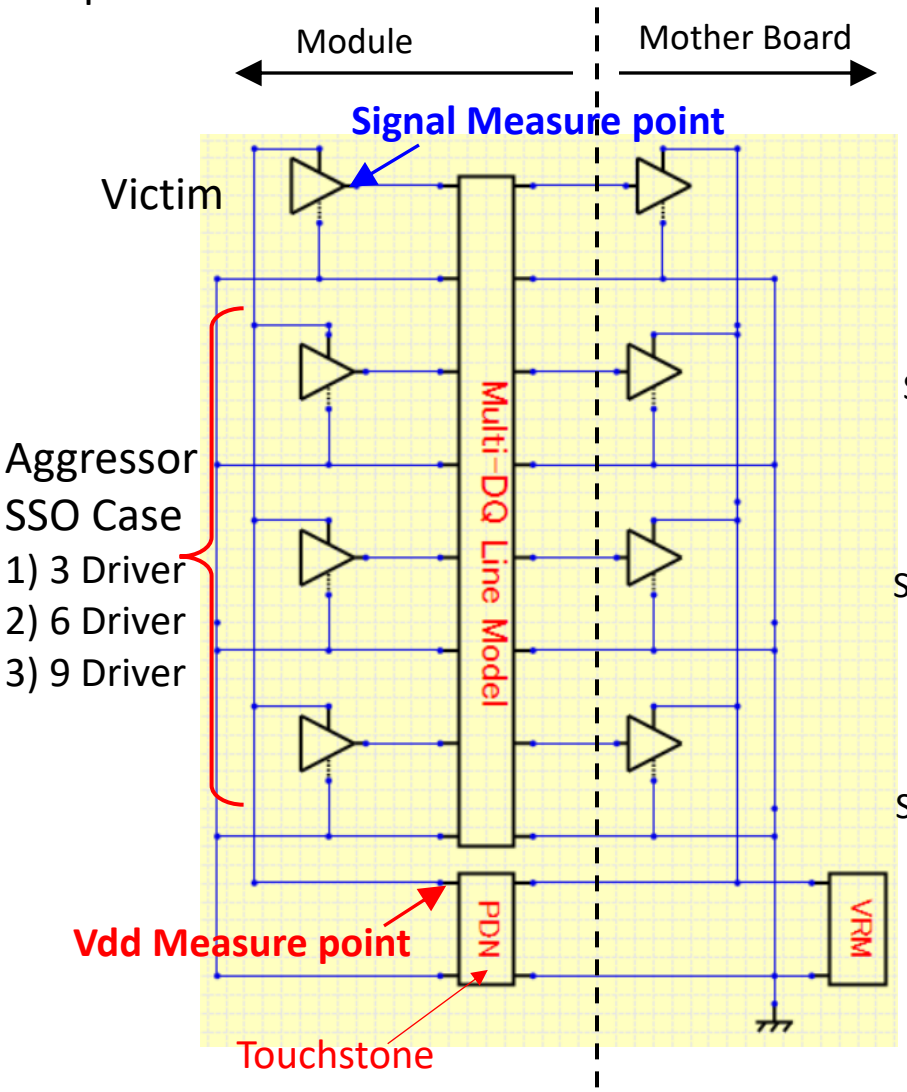
Aggressor:
Switching patterns
1) Victim only
=Single DQ net
2) Even mode
3) Odd mode



EMD model allows simulations that take into account delay variations due to crosstalk.

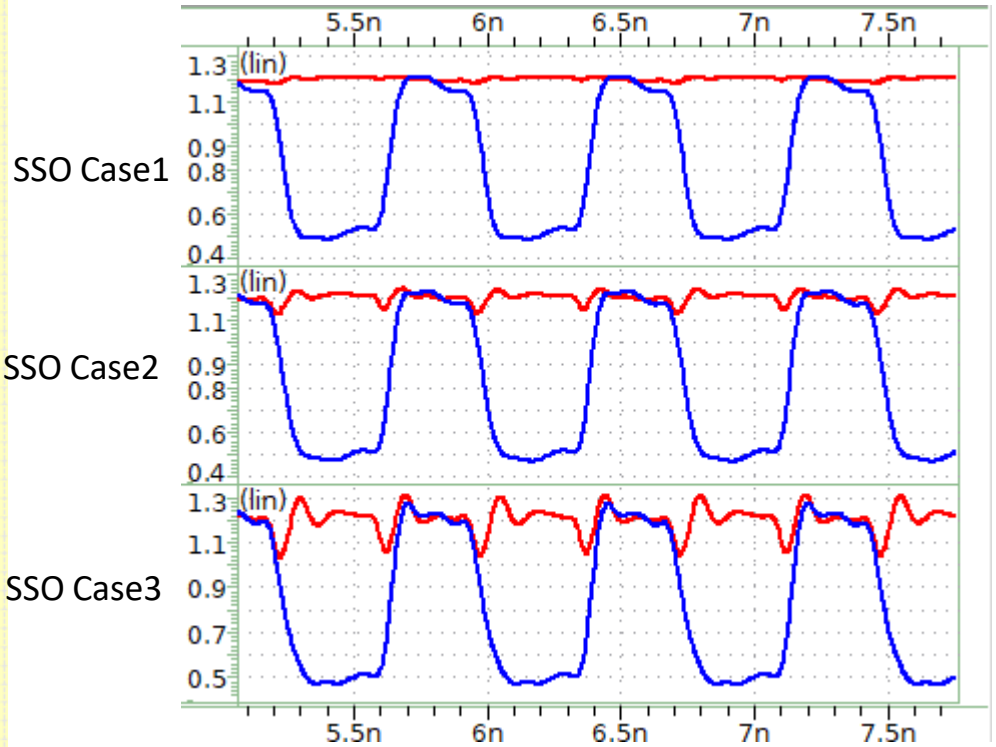
Improvements from EBD model to EMD model

Since the EMD model can also model PDN, Power-aware simulation (including Vdd noise) is possible.



Red: Vdd

Blue: Victim Driver Output



Summary

- We investigated the EMD specifications based on the examples shown in the IBIS V7.2.
- We also considered the advantages over EBD from the EMD specifications.
- EMD model can be modeled with IBIS-ISS (Rs, Gd of W-element) and Touchstone, so high frequency loss model is possible.
- EMD model can model Multi-Line using IBIS-ISS (W-element) and Touchstone, so crosstalk modeling is possible.
- Since the EMD model can also model PDN, Power-aware simulation (including Vdd noise) is possible.
- From the above, the EMD model can be expected to produce results with higher analytical accuracy than the EBD model.

Reference

- “IBIS (I/O Buffer Information Specification) Version 7.2”, ratified 27 January 2023 by the IBIS Open Forum https://ibis.org/ver7.2/

The Future is Interconnected