Hardware and AI/ML: Applications of SIPI & IBIS

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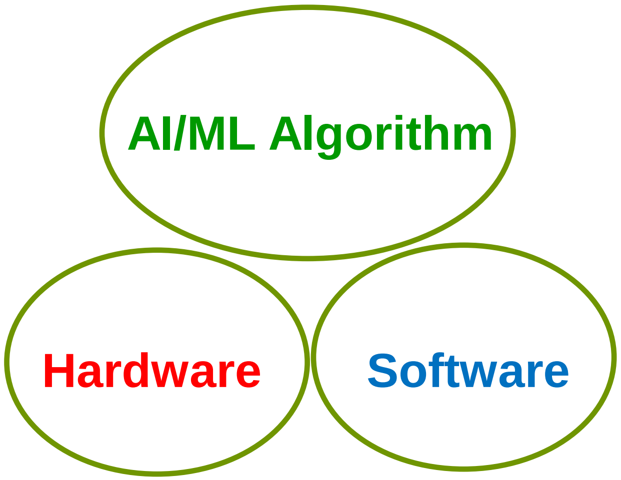
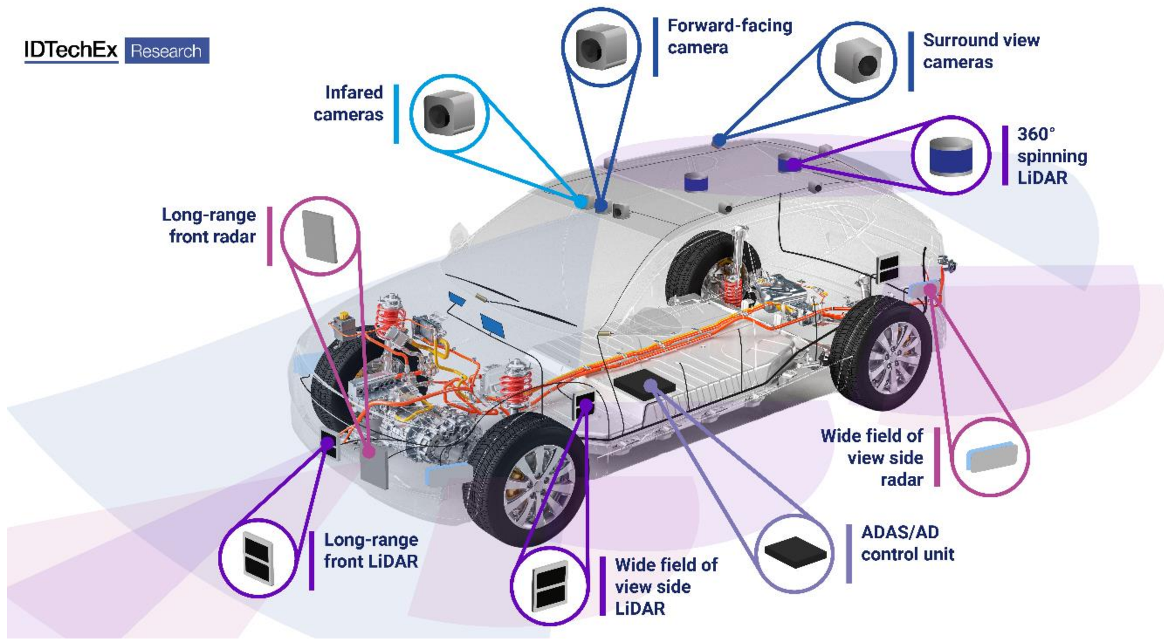
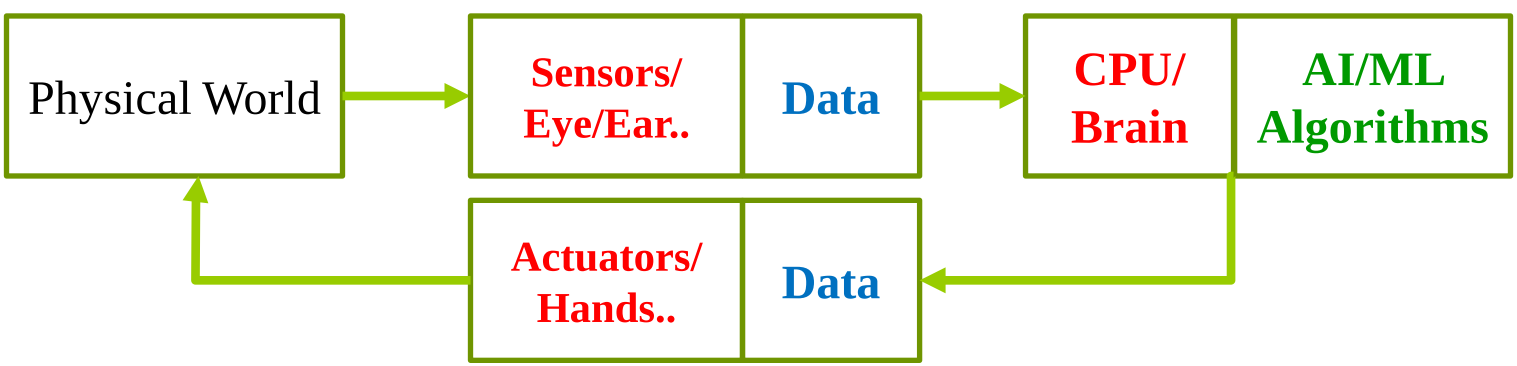
Agenda

- Hardware Plays Critical Roles in AI/ML
- Human vs Silicon Evolutions
- SIPI Demands & Challenges
- AI/ML and Hardware Can Help Each Other
- SIPI AI/ML Case Studies
  - Placement optimization of decoupling capacitors
  - PDN Impedance Prediction (CNN-GA)
  - Eye-diagram-metrics prediction with DNN
  - Eye-diagram generation with RNN
- IBIS AI/ML Usage Cases
  - IBIS + AI/ML for SIPI design and simulations
    - IBIS keywords are very useful as AI/ML parameters
  - Use AI/ML to generate more accurate IBIS models

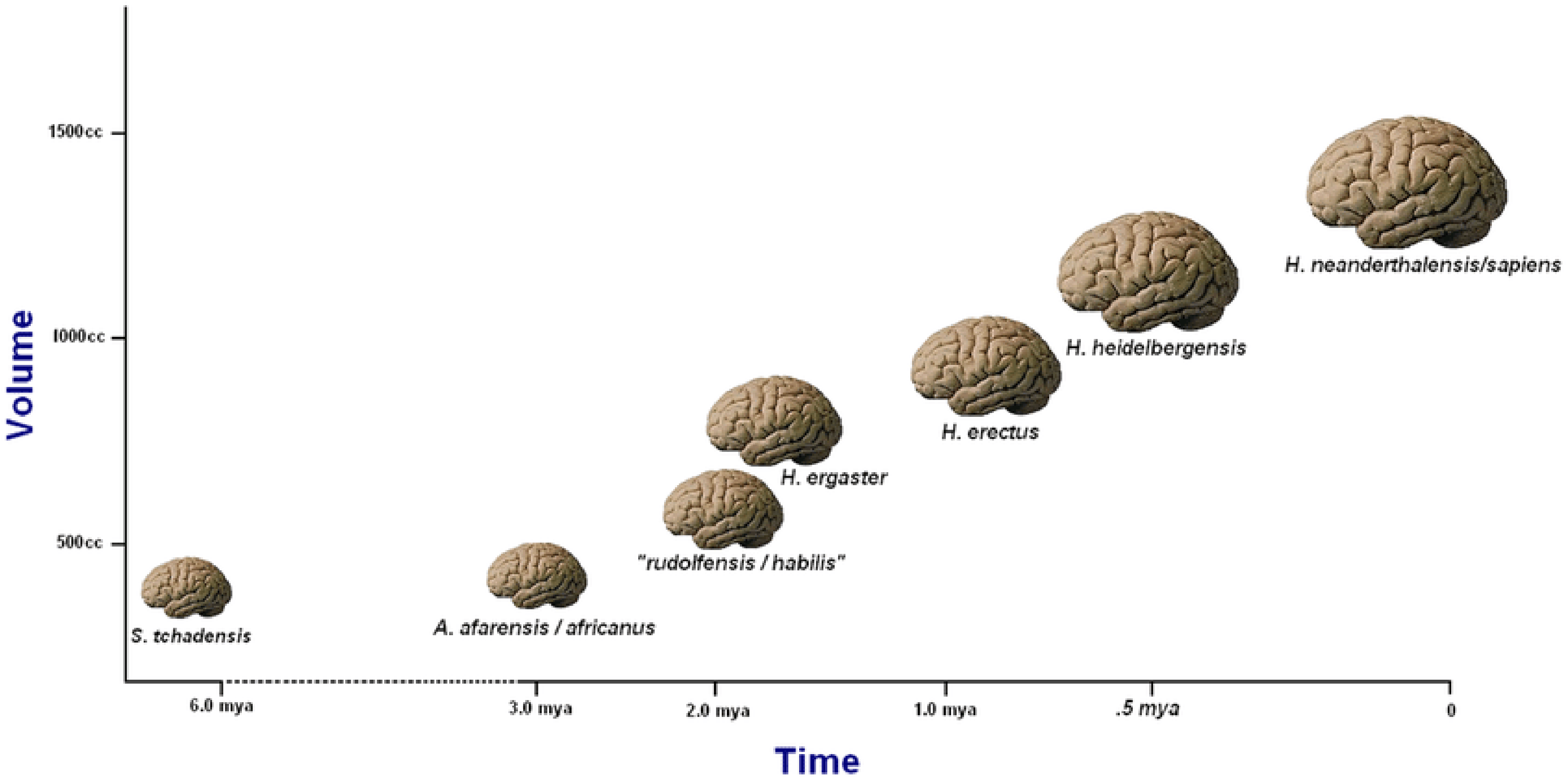
Hardware Plays Critical Roles in AI/ML







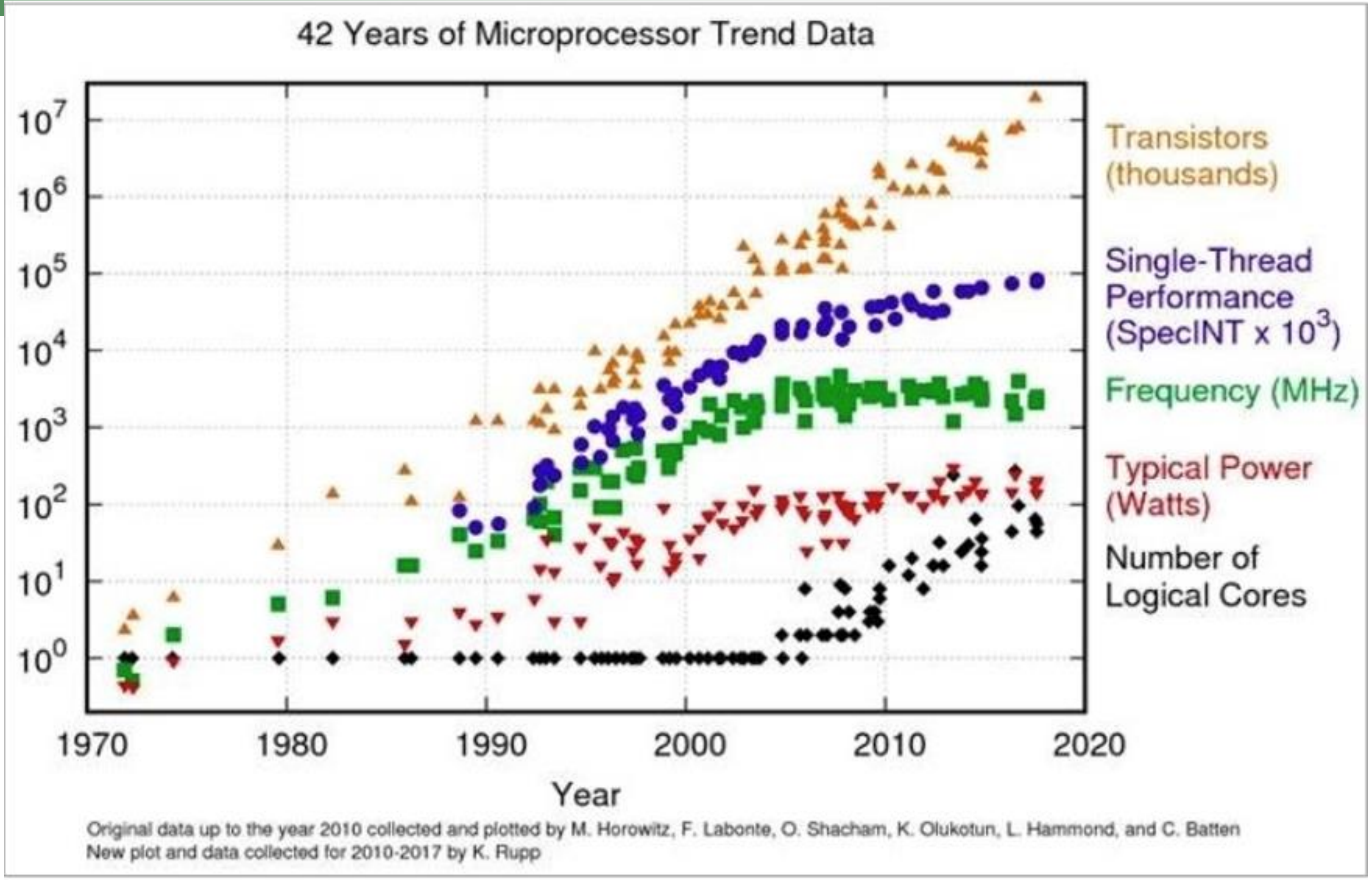
Human Evolution Over Millions Years



3X increase over 6 million years

Reference: How Could Language Have Evolved?DOI:10.1371/journal.pbio.1001934

Silicon Evolution in 42 Years



Source: M. Horowitz, et al. 2010, K. Rupp, 2017.

Figure 20 Tradeoffs in MPU performance after the power limit was reached.

10^7 X increase over 42 years!

Reference: INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™ 2023 IRDS SEMICONDUCTOR CRISES AND ROADMAPS, RESCUES PAOLO GARGINI, IRDS CHAIRMAN

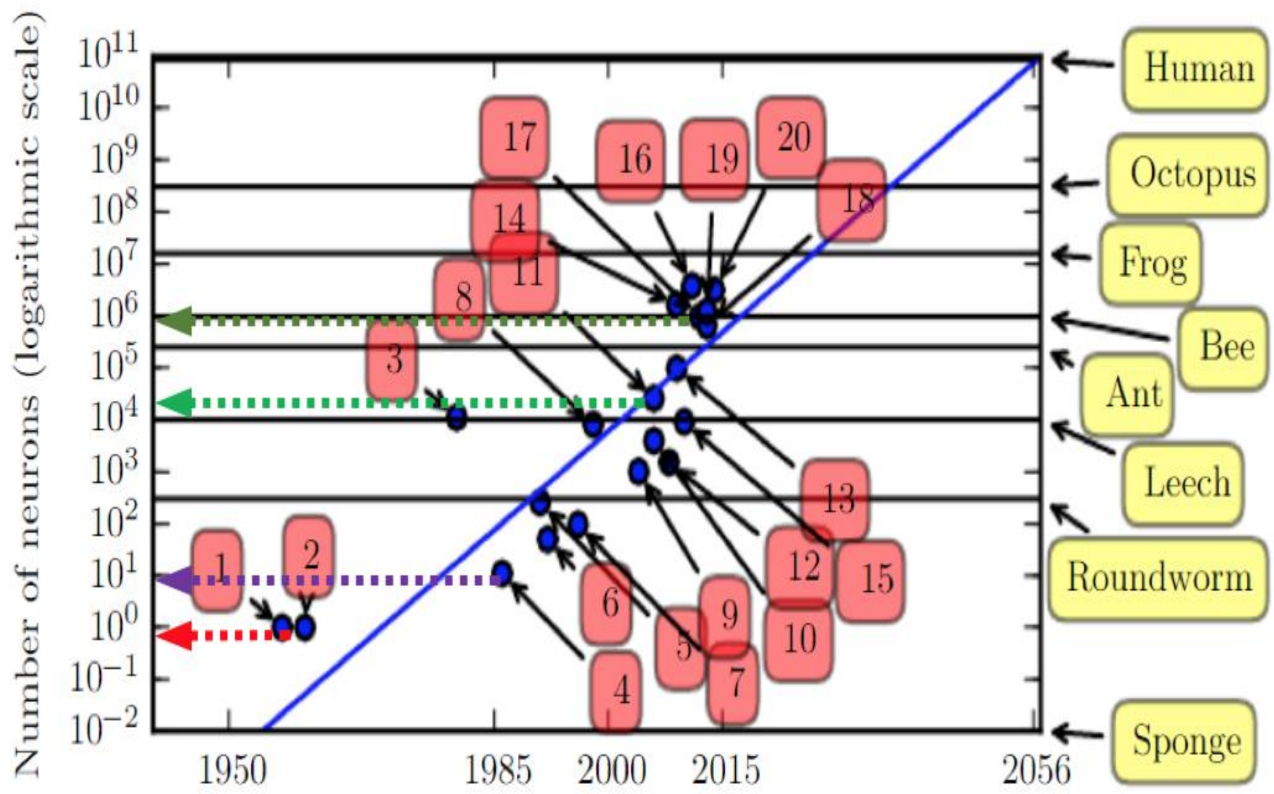
Machine vs Living Creatures

Multi-GPU convolutional neural network (2012)

GPU accelerated convolutional neural network (2006)

Early back-propagation network (1986)

Perception (1958)



Neural Network Size Grows with Hardware Advancement

Ivan Goodfellow et al.

Silicon/Hardware is evolving much faster, but still fall behind Human

Signal Integrity Demands & Challenges

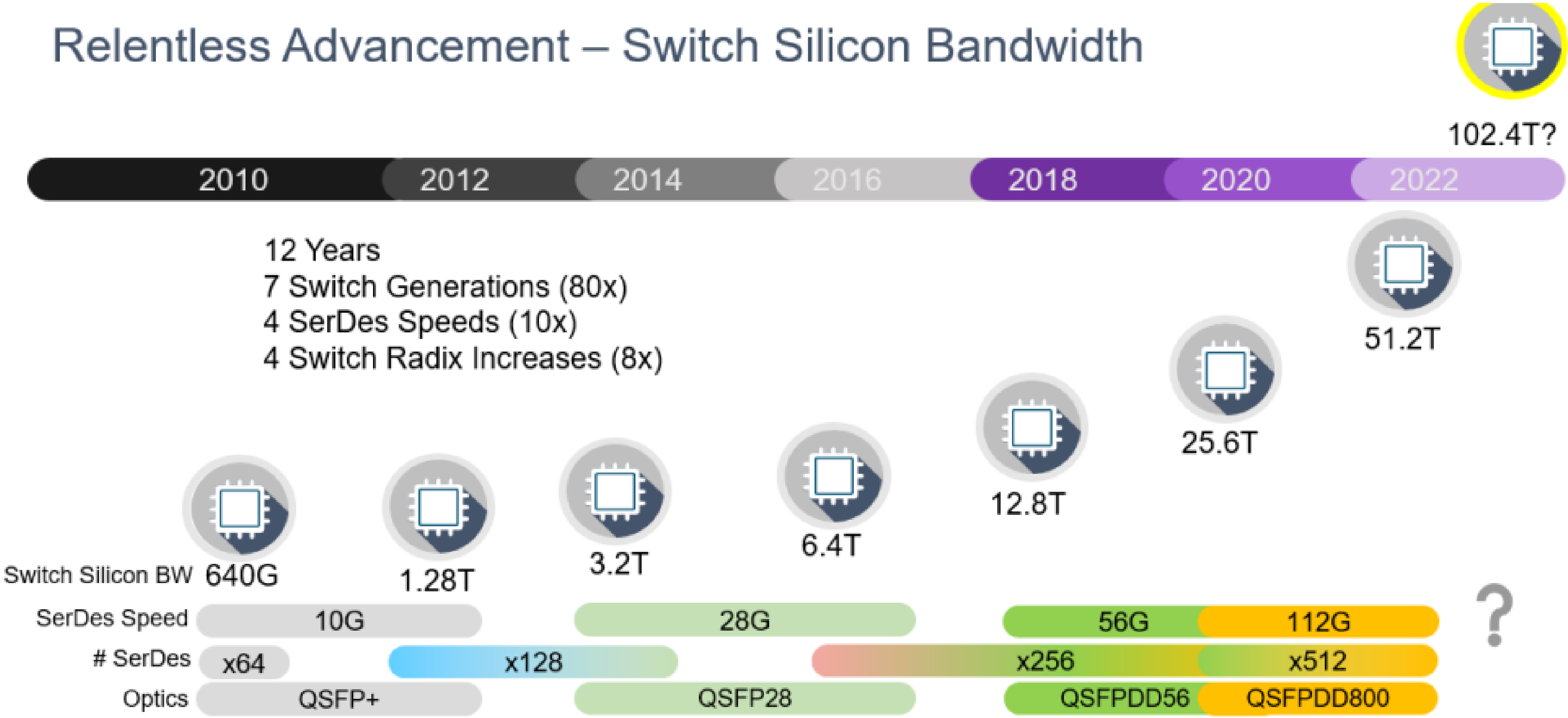


Figure 3 Relentless advancement – switch silicon bandwidth

Reference: OIF Next Generation CEI-224G Framework
https://www.oiforum.com/wp-content/uploads/OIF-FD-CEI-224G-01.0.pdf

Power Integrity Demands & Challenges

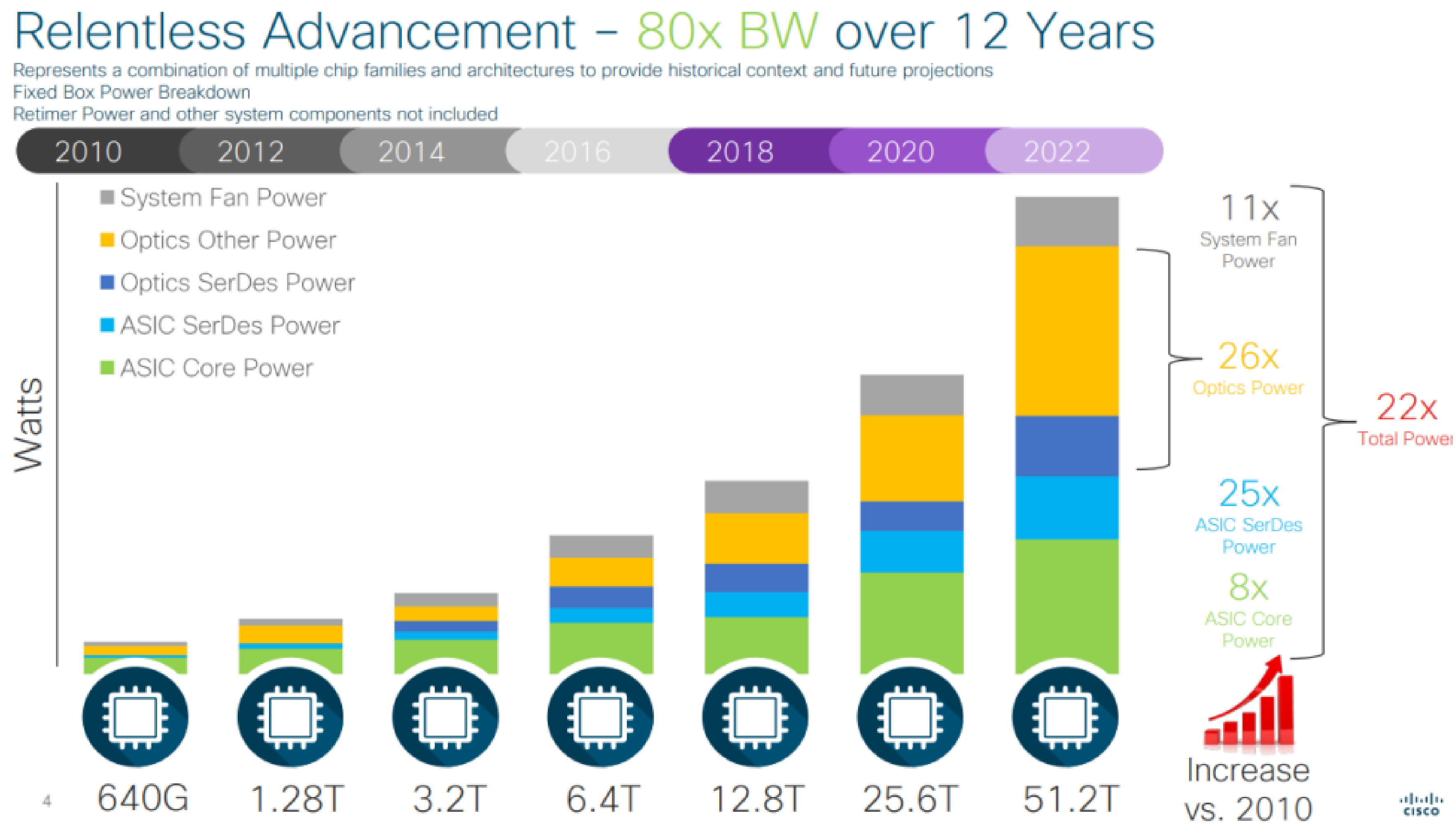
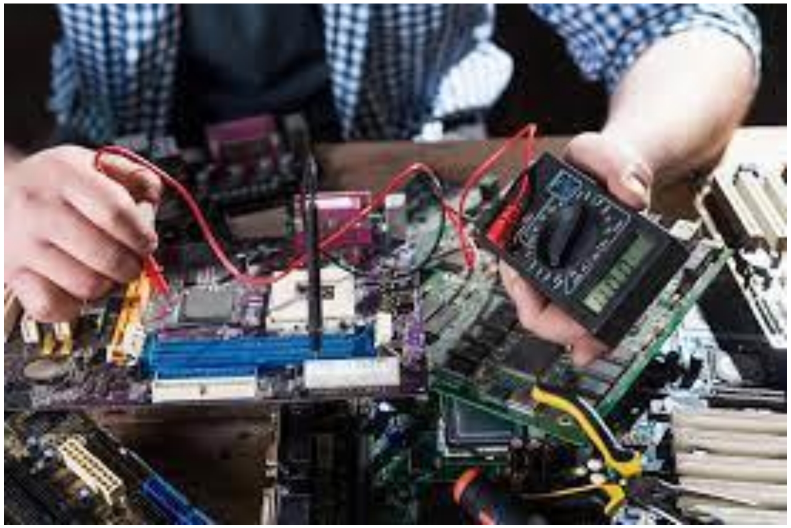


Figure 4 Relentless advancement – 80x BW over 12 years

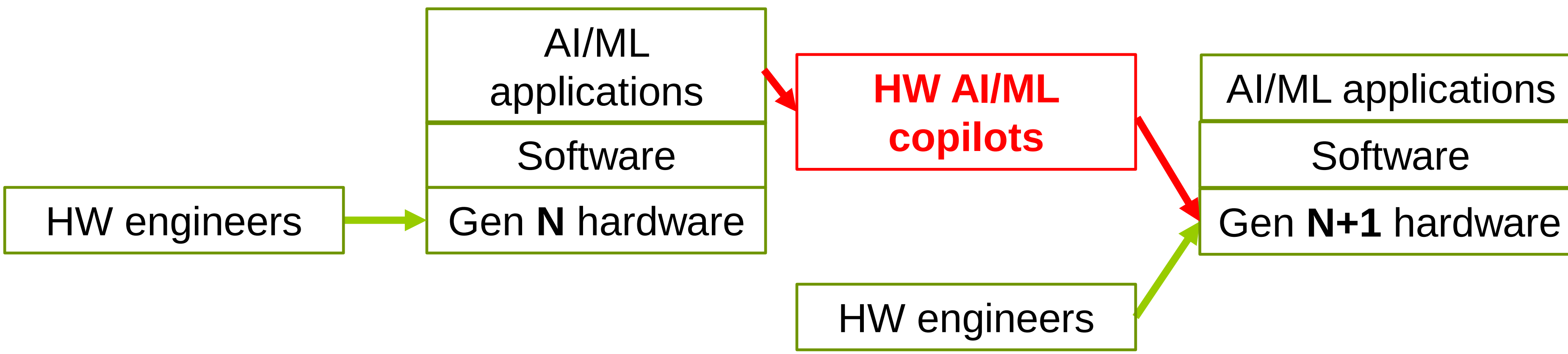
Reference: OIF Next Generation CEI-224G Framework
https://www.oiforum.com/wp-content/uploads/OIF-FD-CEI-224G-01.0.pdf

AI/ML and Hardware Can Help Each Other



Hardware is hard!

Hardware is fun!

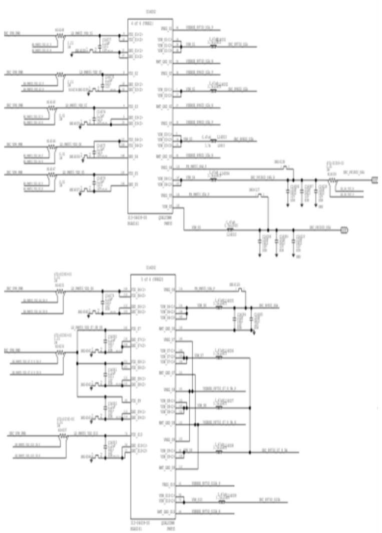


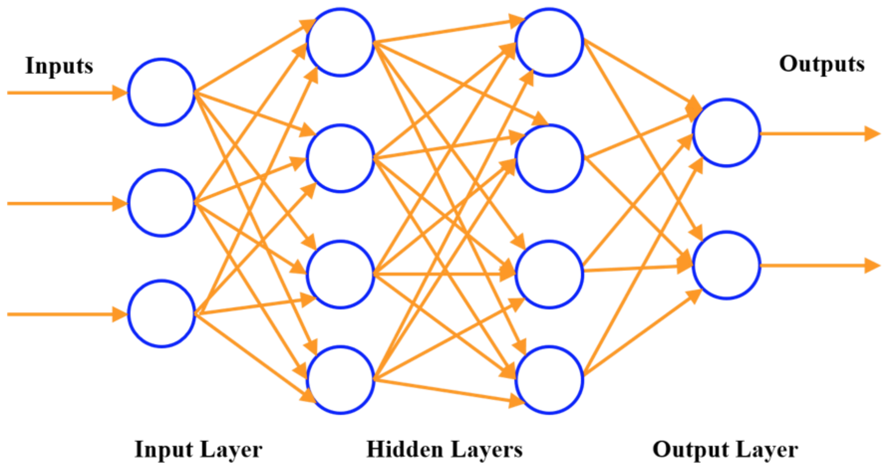
Advanced HW AI/ML copilots are expected to significantly improve the hardware design. This will enable a positive feedback loop between Hardware Design and AI/ML applications.

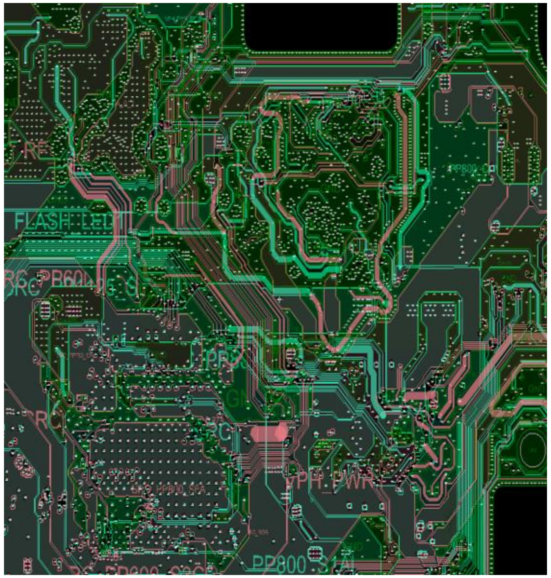
More Advanced Hardware for AI/ML

Current Silicon/Hardware cannot meet exponential growth of AI/ML!
nVidia is a $T dollar company now. We need more advanced hardware!

More Powerful AI/ML for Hardware Design





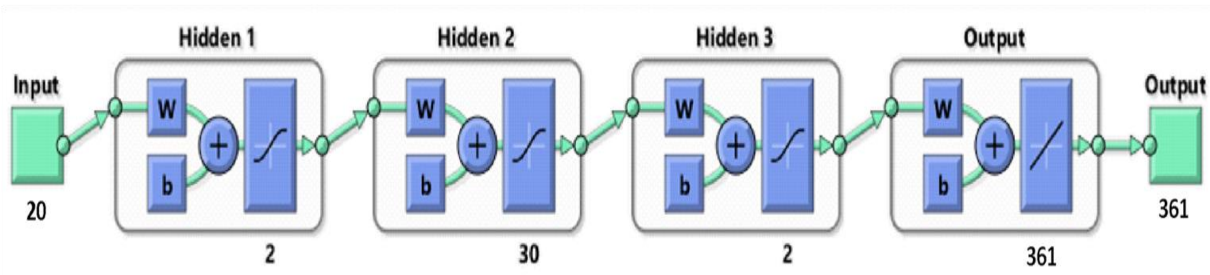


Schematic

Layout

Mark Hayter, Plenary Talk, 2018 IEEE EMC Symposium, Singapore

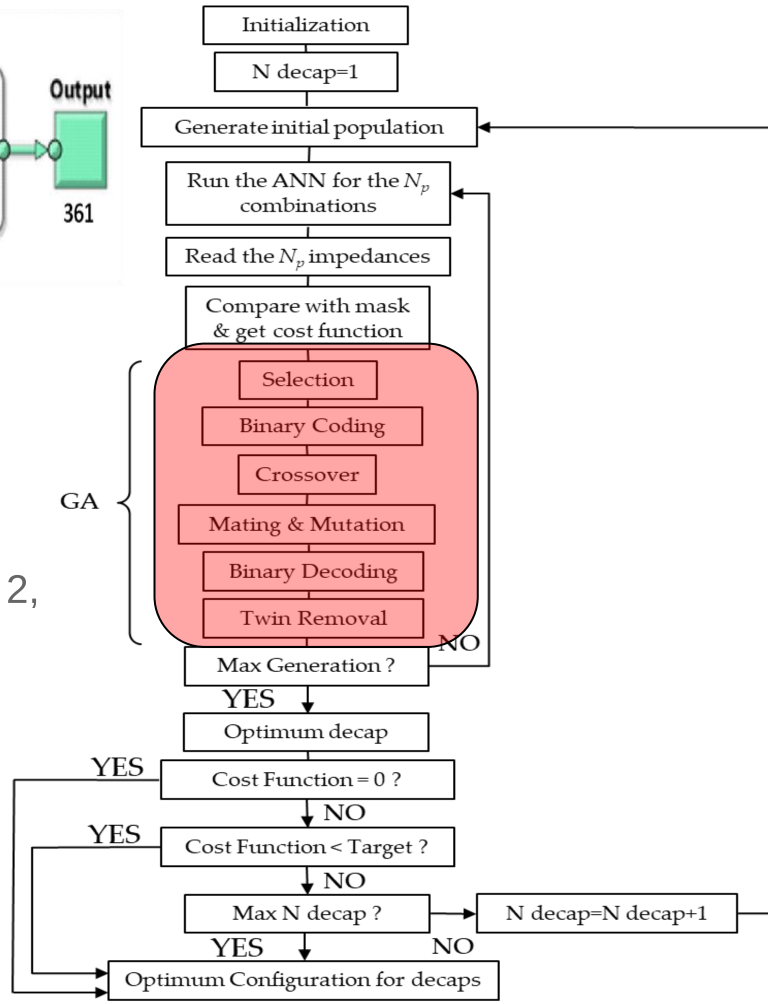
Case Study: Optimization for Decap Placement (ANN-GA)



Input: decaps value and location

Output: PDN impedance

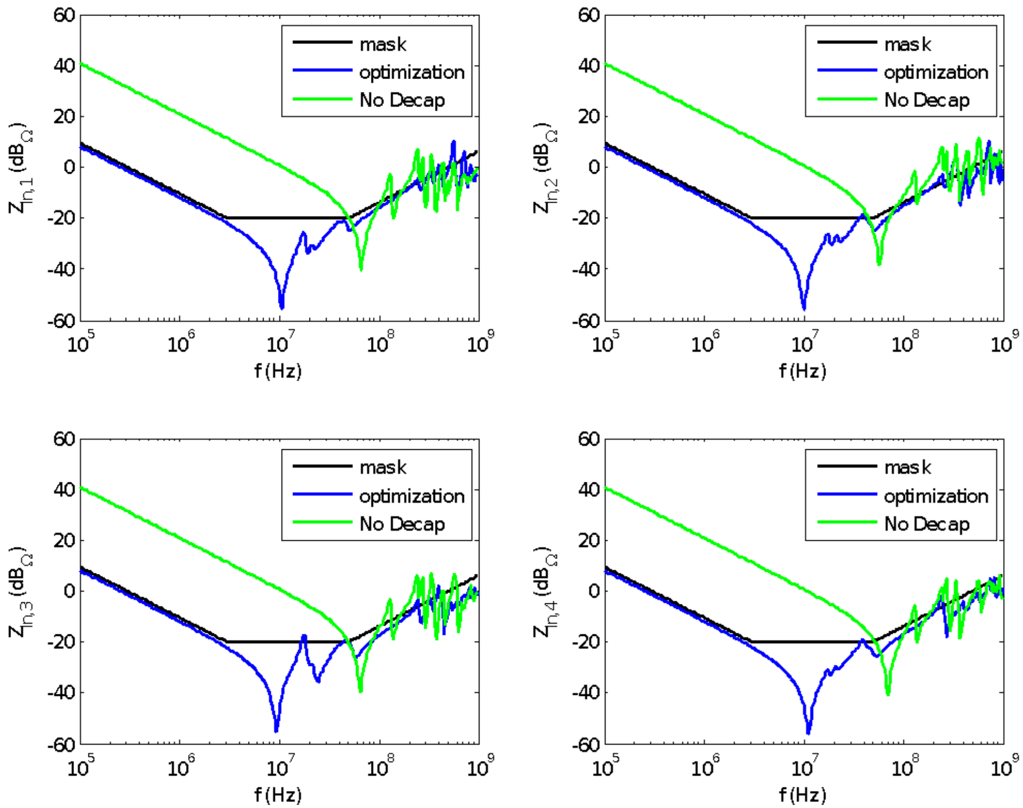
- The final architecture consists on 3 hidden layer (width of 2, 30 and 2, respectively)
- The output layer has size of 361 : the values of **Zin(f)** at the 361 frequency points of the spectrum

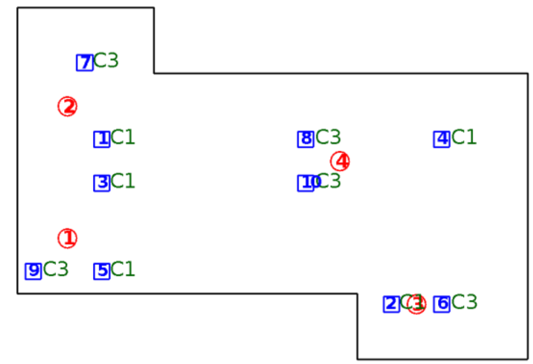


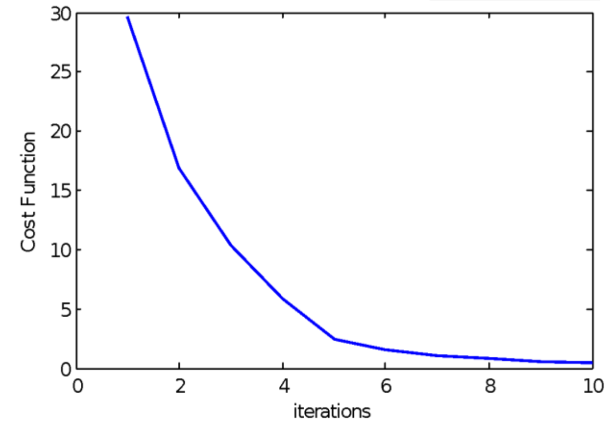
Results of the Optimization

Elementary capacitors			
	C (nF)	ESL (pH)	ESR (mΩ)
C_1	100	222	8.9
C_2	47	154	21.4
C_3	22	142	25.2

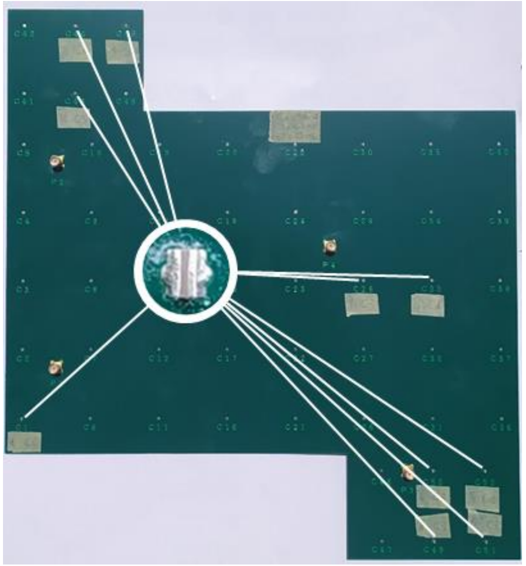
Pop: 10 chrom
gen: 10
f_{max}: 1 GHz
iter: 10



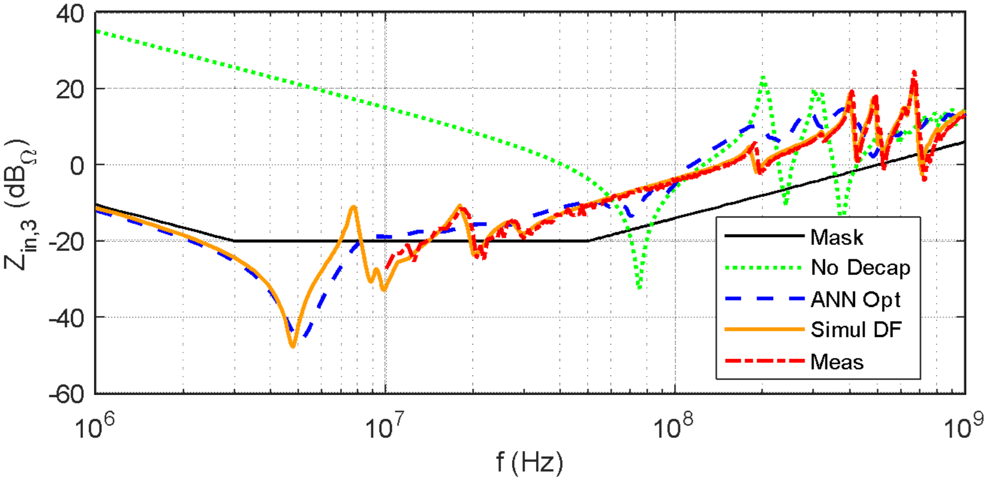




Lab Validations



Decap locations in the real board

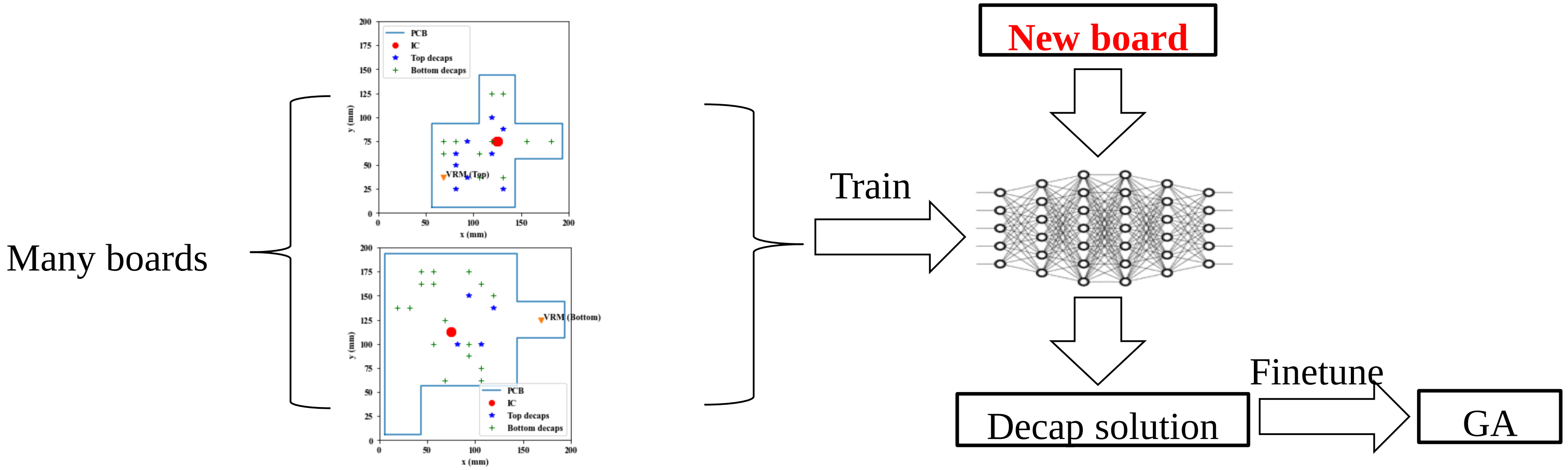


Z_{in} at Port 3:

- from **ANN-GA**
- from **measurement**
- from **simulation**

Case Study: PDN Impedance Prediction (CNN-GA)

Deep learning to optimize Decap placement given any: board shape, stack-up, IC location, and # of decaps

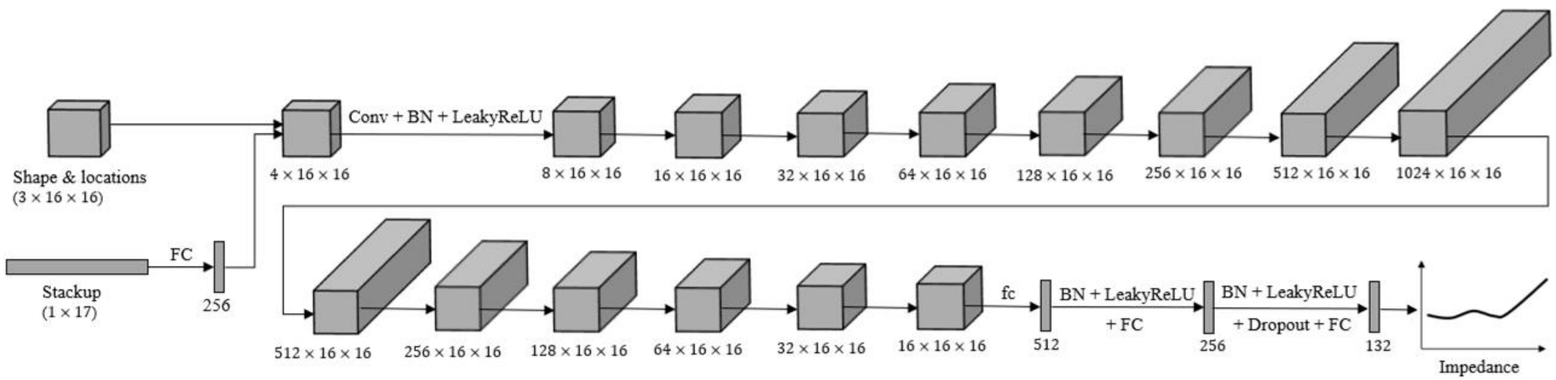


Two step approach: trained network + fine tune (GA)

Use the predicted solution by the DRL as a seeded solution of the GA

Case Study: PDN Impedance Prediction

Convolutional neural network (CNN) structure:



- Training: 1.3M board
- Testing: 10K board
- Training time: 80 hours (1 NVIDIA Tesla K80 GPU)

Case Study: PDN Impedance Prediction

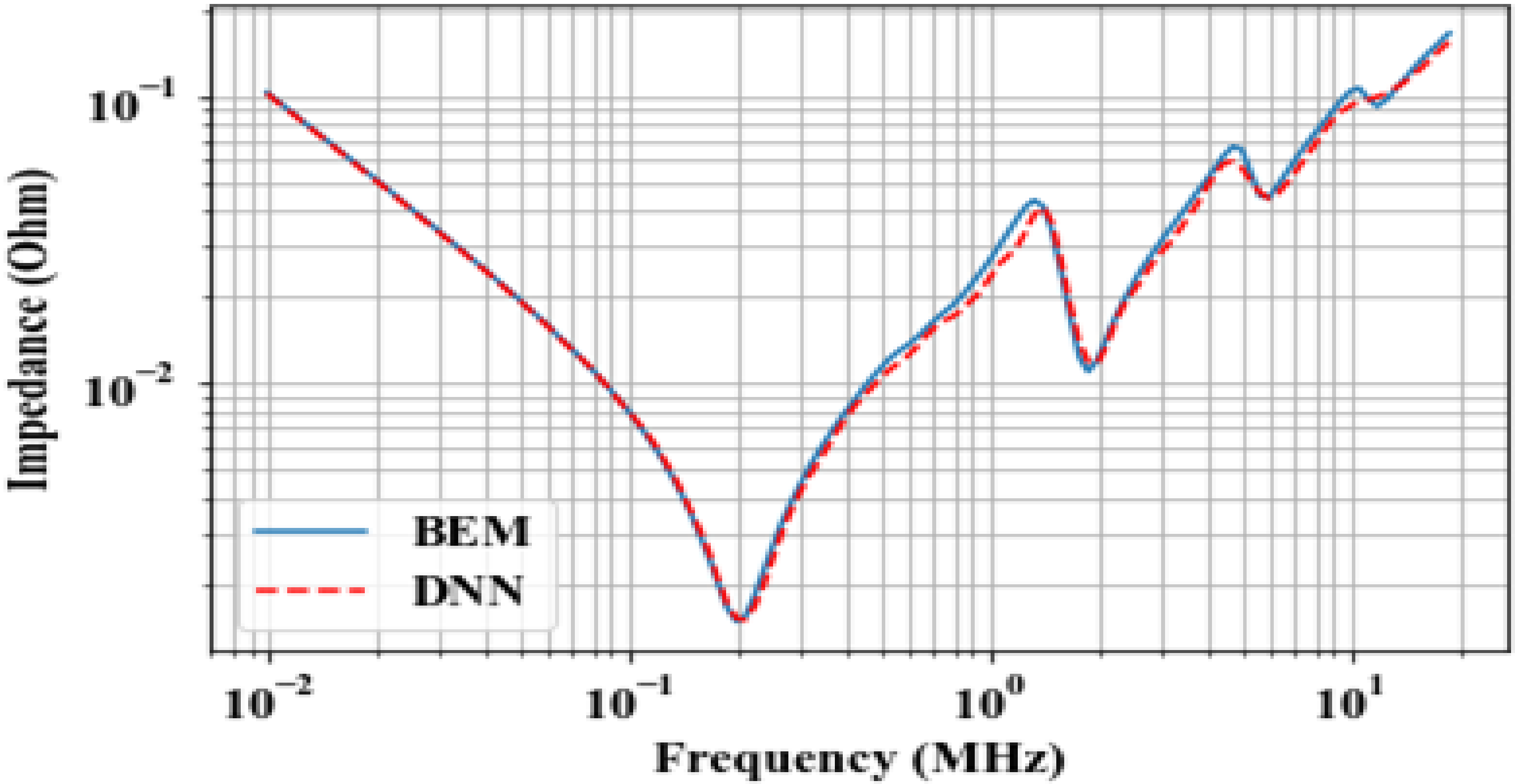
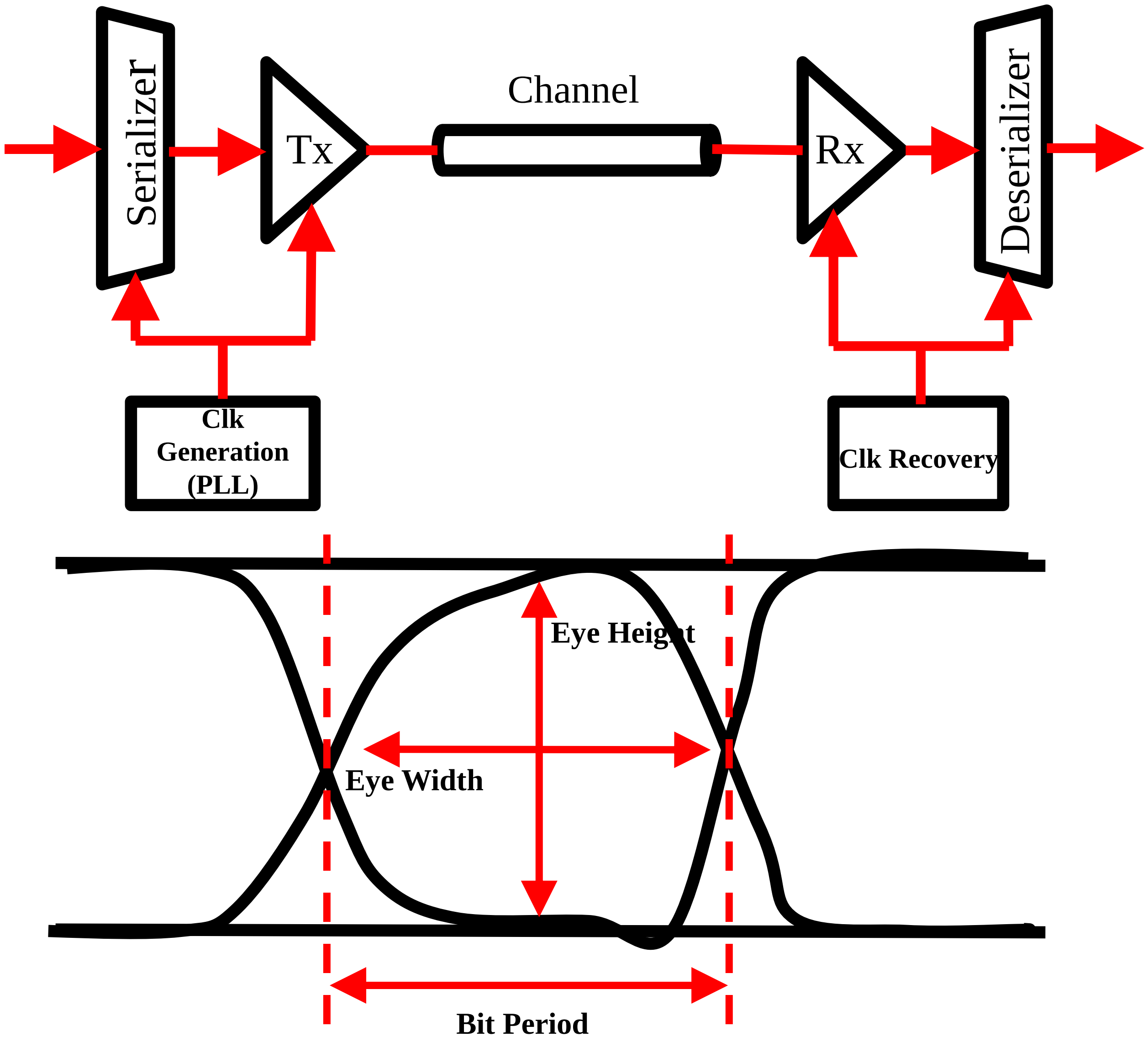


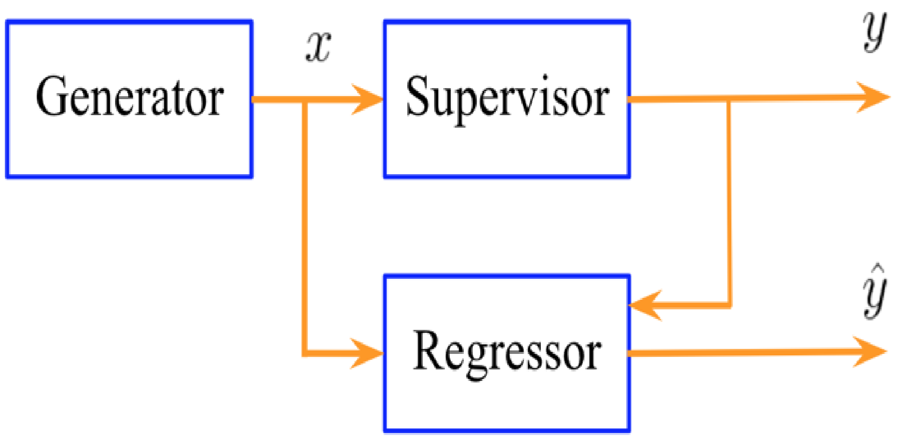
TABLE 2 Time comparison

Methods	Case 1	Case 2
Full-wave simulation	35 min	40 min
Boundary element method	10 s	30 s
Deep neural network	0.1 s	0.1 s

Case Study: ML in High-Speed Channel Modeling



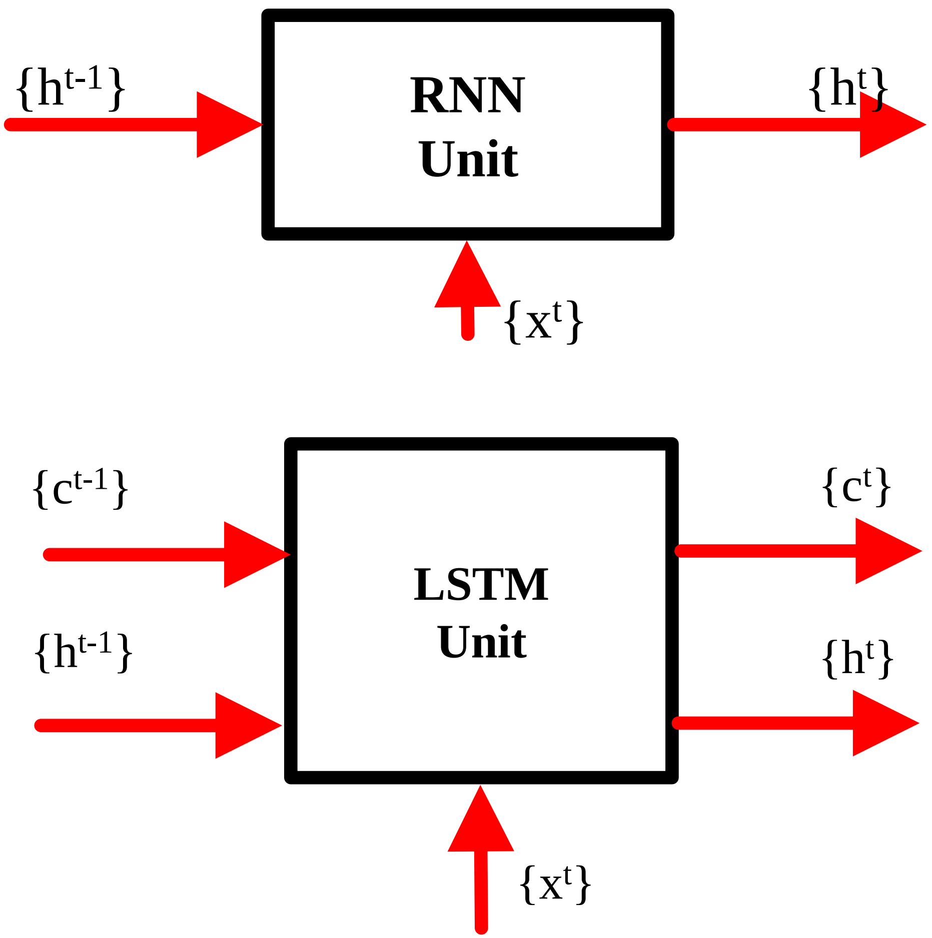
Case Study: Eye-diagram-metrics Prediction with DNN

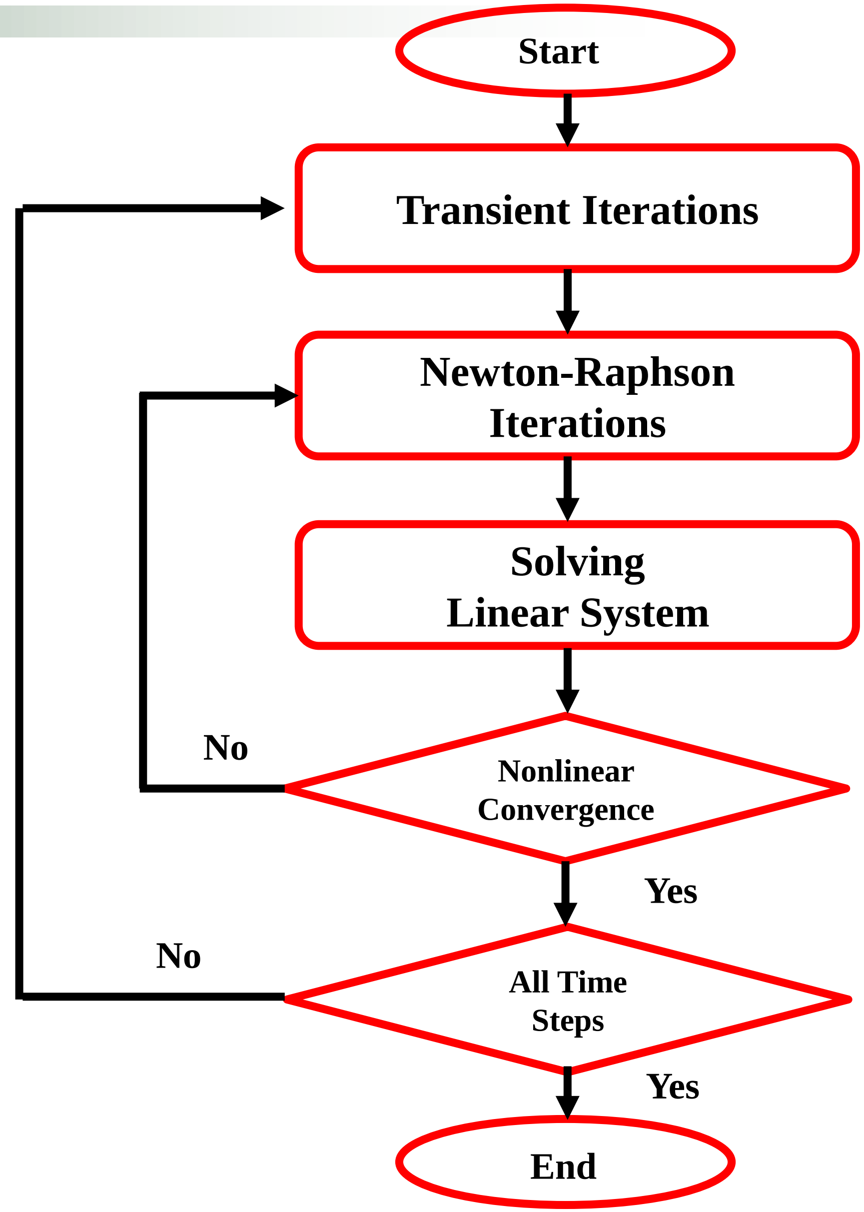


TensorFlow

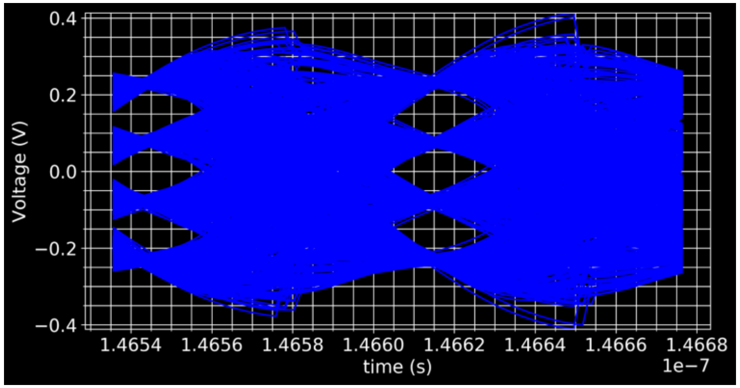
- Generator creates a set of input parameters for a high-speed channel, stored in $\{x\}$.
- Supervisor returns eye height or width y based on $\{x\}$.
- The learning process is essentially the selection of the right regression function $f(\{x\},\{\theta\})$ where $\{\theta\}$ contains the parameters to be learned, such that the prediction made by $f(\{x\},\{\theta\})$ approximates the value returned by the supervisor uniformly over all possible input $\{x\}$.
- Regression method in this work includes linear, support vector, and DNN regressions.

Case Study: Eye-diagram-metrics Prediction with RNN

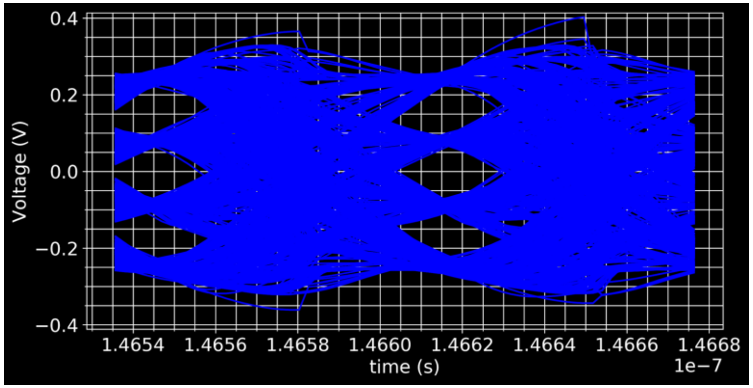




Eye Diagram Generation with a PAM4 Example



Circuit Simulator



LSTM Network

T. Nguyen, T. Lu, K. Wu, J. Schutt-Aine, "Transient simulations of high-speed channels with recurrent neural network," *in IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems.*

IBIS + AI/ML for SIPI Design and Simulations

- **IBIS keywords** are very useful as AI/ML input parameters

- This is an active research field and here are some publications:

  - Comparison of Machine Learning Techniques for Predictive Modeling of High-Speed Links, Hanzhi Ma; Er-Ping Li;Andreas C. Cangellaris;Xu Chen, 2019 IEEE 28th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
  - PAM-4 Behavioral Modeling using Machine Learning via Laguerre-Volterra Expansion, Xinying Wang; Thong Nguyen; Jose E. Schutt-Aine, 2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS)
  - Self-Evolution Cascade Deep Learning Model for High-Speed Receiver Adaptation, Bowen Li; Brandon Jiao; Chih-Hsun Chou; Romi Mayder; Paul Franzon, IEEE Transactions on Components, Packaging and Manufacturing Technology, Year: 2020 | Volume: 10, Issue: 6

Use AI/ML to generate more accurate IBIS models

- This is a relatively new research field, and it belongs to **generative AI.**

- Presentation from Prof Huang at the Hybrid IBIS Summit at 2023 IEEE Symposium on EMC+SIPI

USB3.0 IBIS-AMI Model Construction based on Measurement and Neural Network
Jiahuan Huang (Missouri S&T EMC Lab, USA)
Junho Joo (Missouri S&T EMC Lab, USA)
Hank Lin (ASUS, Taiwan)
Bin-Chyi Tseng (ASUS, Taiwan)
Will Chan (ASUS, Taiwan)
Chulsoon Hwang (Missouri S&T EMC Lab, USA)
[Presented by Jiahuan Huang]

THANK YOU!
&
QUESTIONS?

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Abbreviations

- GA: Genetic Algorithm
- ANN: Artificial Neural Network
- CNN: Convolutional Neural Network
- RNN: Recurrent Neural Network
- DNN: Deep Neural Networks
- LSTM: Long Short-Term Memory

Publications

[A] Stefano Piersanti, Riccardo Cecchetti, Carlo Olivieri; Francesco de Paulis; Antonio Orlandi; Markus Bueker, **Decoupling Capacitors Placement at Board Level Adopting a Nature-Inspired Algorithm**, in Electronics 2019, Volume 8, Issue 7, October 2019, available online: https://www.mdpi.com/2079-9292/8/7/737/pdf

[B] Francesco de Paulis; Riccardo Cecchetti; Carlo Olivieri; Stefano Piersanti; Antonio Orlandi; Markus Bueker, **Efficient Iterative Process based on an Improved Genetic Algorithm for Decoupling Capacitor Placement at Board Level**, in Electronics 2019, Volume 8, Issue 11, available online: https://www.mdpi.com/2079-9292/8/11/1219/pdf

[C] R. Cecchetti, F. de Paulis, C. Olivieri, A. Orlandi, M. Buecker, "**Effective PCB Decoupling Optimization by Combining an Iterative Genetic Algorithm and Machine Learning**" in Electronics 2020, Volume. 9, Issue 8, August 2020, available online: https://www.mdpi.com/2079-9292/9/8/1243

[D] F. de Paulis, R. Cecchetti, C. Olivieri and M. Buecker, "**Genetic Algorithm PDN Optimization based on Minimum Number of Decoupling Capacitors Applied to Arbitrary Target Impedance**," 2020 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), Reno, NV, USA, 2020, pp. 428-433, doi: 10.1109/EMCSI38923.2020.9191458. "**Best SIPI Symposium Paper Award**"

[E] Lu, Tianjian, Ju Sun, Ken Wu, and Zhiping Yang. "**High-speed channel modeling with machine learning methods for signal integrity analysis**." IEEE Transactions on Electromagnetic Compatibility 60, no. 6 (2018): 1957-1964.

[F] Nguyen, Thong, Tianjian Lu, Ju Sun, Quang Le, Ken We, and Jose Schut-Aine. "T**ransient simulation for high-speed channels with recurrent neural network**." In 2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), pp. 303-305. IEEE, 2018.

[G] L. Zhang, J. Juang, Z. Kiguradze, B. Pu, S. Jin, S. Wu, Z. Yang, and C. Hwang, "**Fast PDN Impedance Prediction using Deep Learning**", submitted to International Journal of Numerical Modeling: Electronic Networks, Devices and Fields.

[H] J. Juang, L. Zhang, Z. Kiguradze, B. Pu, S. Jin, S. Wu, Z. Yang, and C. Hwang, "**A Modified Genetic Algorithm for the Selection of Decoupling Capacitors in PDN Design**", accepted to IEEE EMC+ SIPI 2021.

[I] L. Zhang, J. Juang, Z. Kiguradze, B. Pu, S. Jin, S. Wu, Z. Yang, and C. Hwang, "**Efficient DC and AC Impedance Calculation for Arbitrary-shape and Multi-layer PDN Using Boundary Integration**," IEEE Trans. Electromagn. Compat., to be submitted.

[J] L. Zhang, J. Juang, Z. Kiguradze, S. Jin, S. Wu, Z. Yang, J. Fan, C. Hwang, **"PCB-Level Decap Placement Using Deep Reinforcement Learning**", IEEE Trans Microw Theory Tech., to be submitted.