IBIS Model Validation Report

Asian IBIS Summit, Shanghai China
October 27, 2006

**Zheng Qi**
Qzheng@fiberhome.com.cn

WRI

■ **IBIS Models have played an important role in signal integrity analysis**

- Access Buffer Characteristics
  - Buffer's transition time
  - driver output impedance
- Critical Net Quality Check
  - Incident Voltage
  - Monotonic
- Timing Analysis
  - Flight Time Calculating
- Power Integrity Analysis

overview

■ Before playing with IBIS we have to know

- behavioral model concept

overview
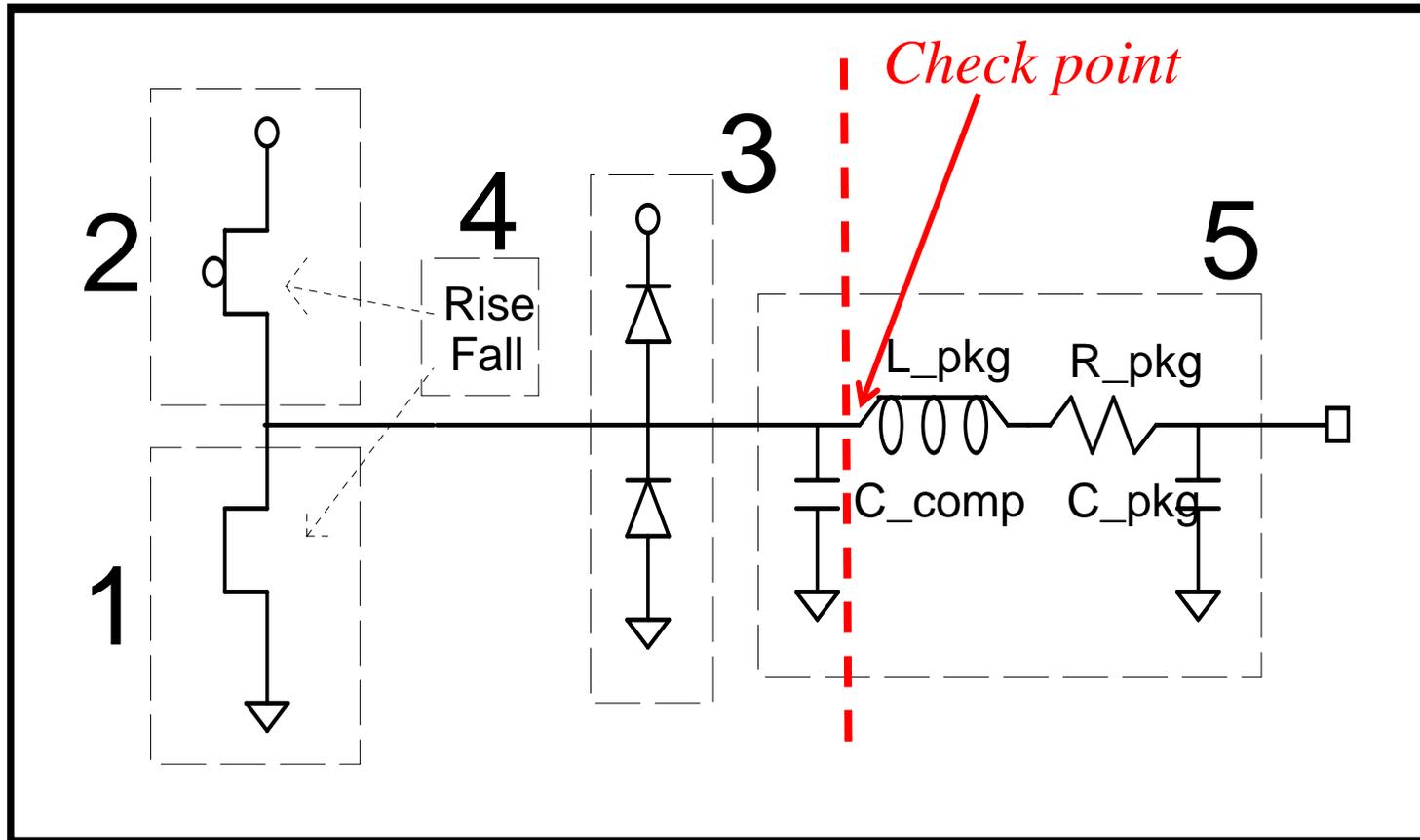
- **Model Validation (Comparison)**
  - With & without Package parameter
  - Spice model Vs IBIS model
  - R-fixture comparison
- **Test fixture**
  - 50 Ω Resistor Load to GND
  - 10pf Capacitor load to GND
- **Model (original model from *A* company)**
  - Push-pull clock buffer
  - 1R+1F
  - R_fixture = 0.50k Ω

Spice model simulation

■ Removing package parameter first

Sub-Title

10pf load

Package parameter comparison

Spice model Vs IBIS model
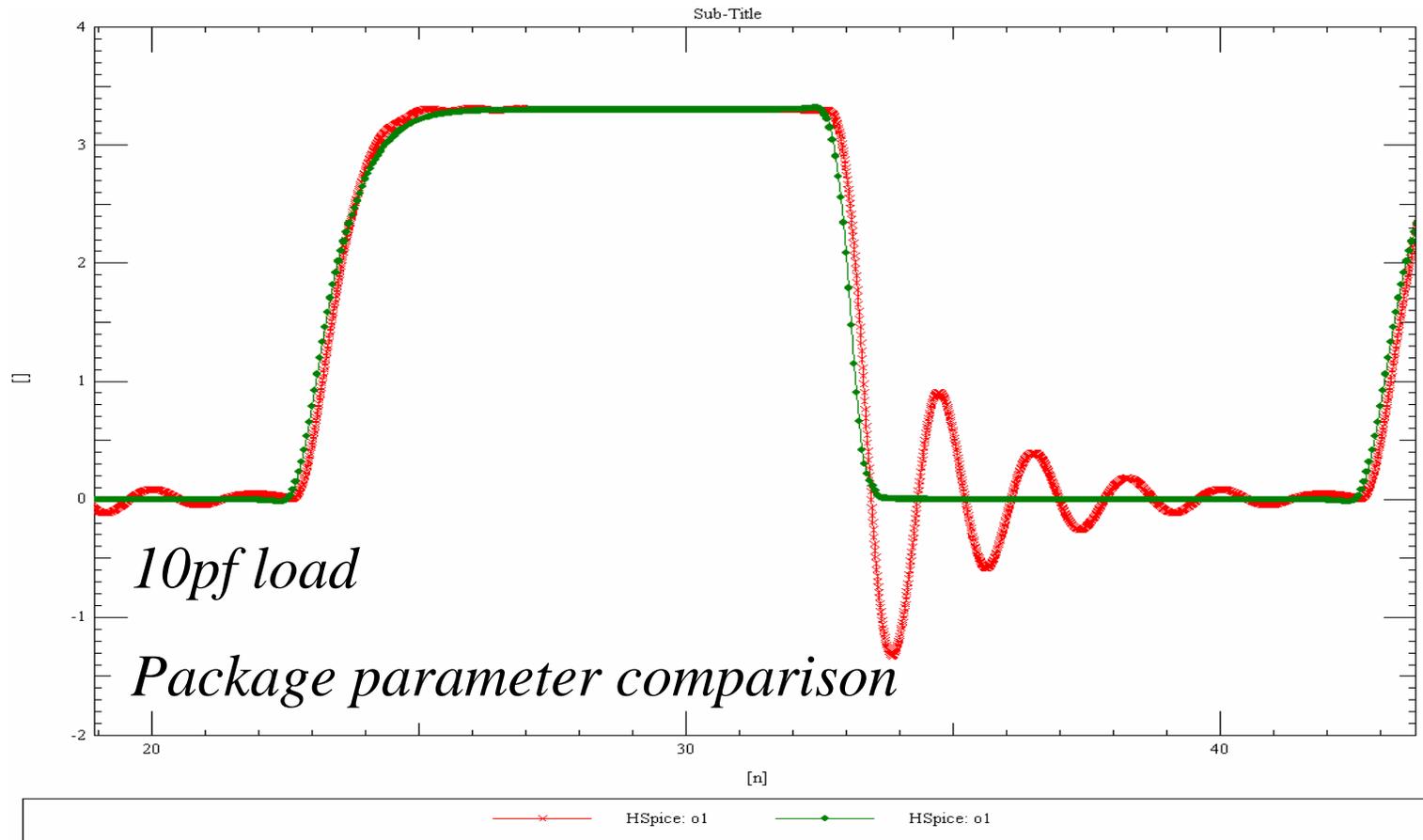
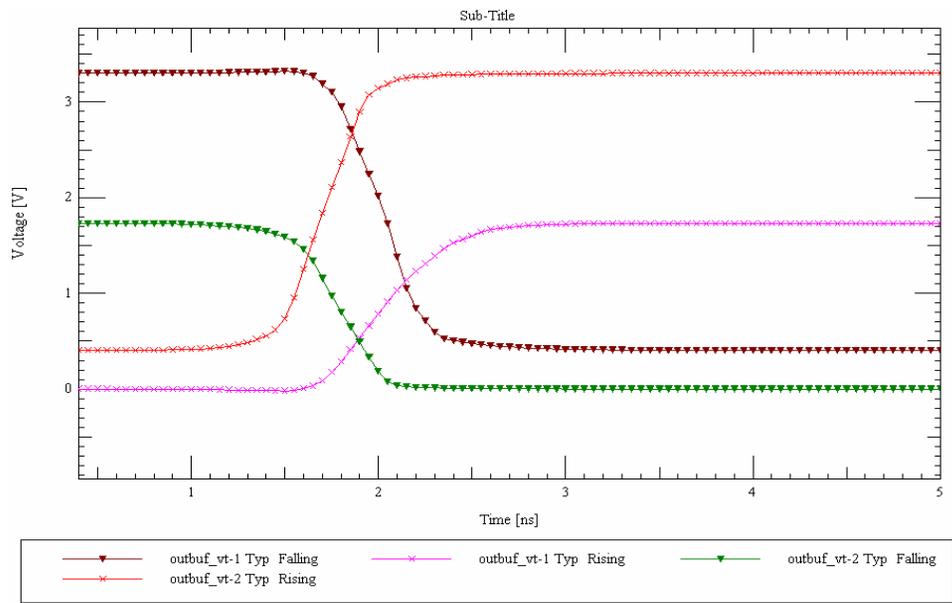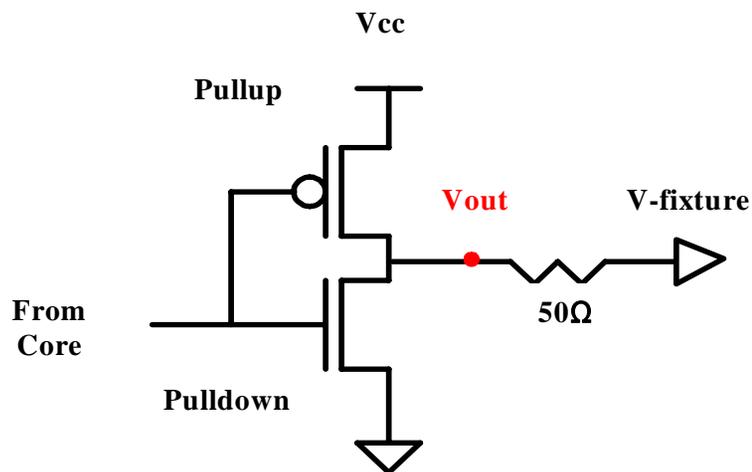- **Original IBIS model**
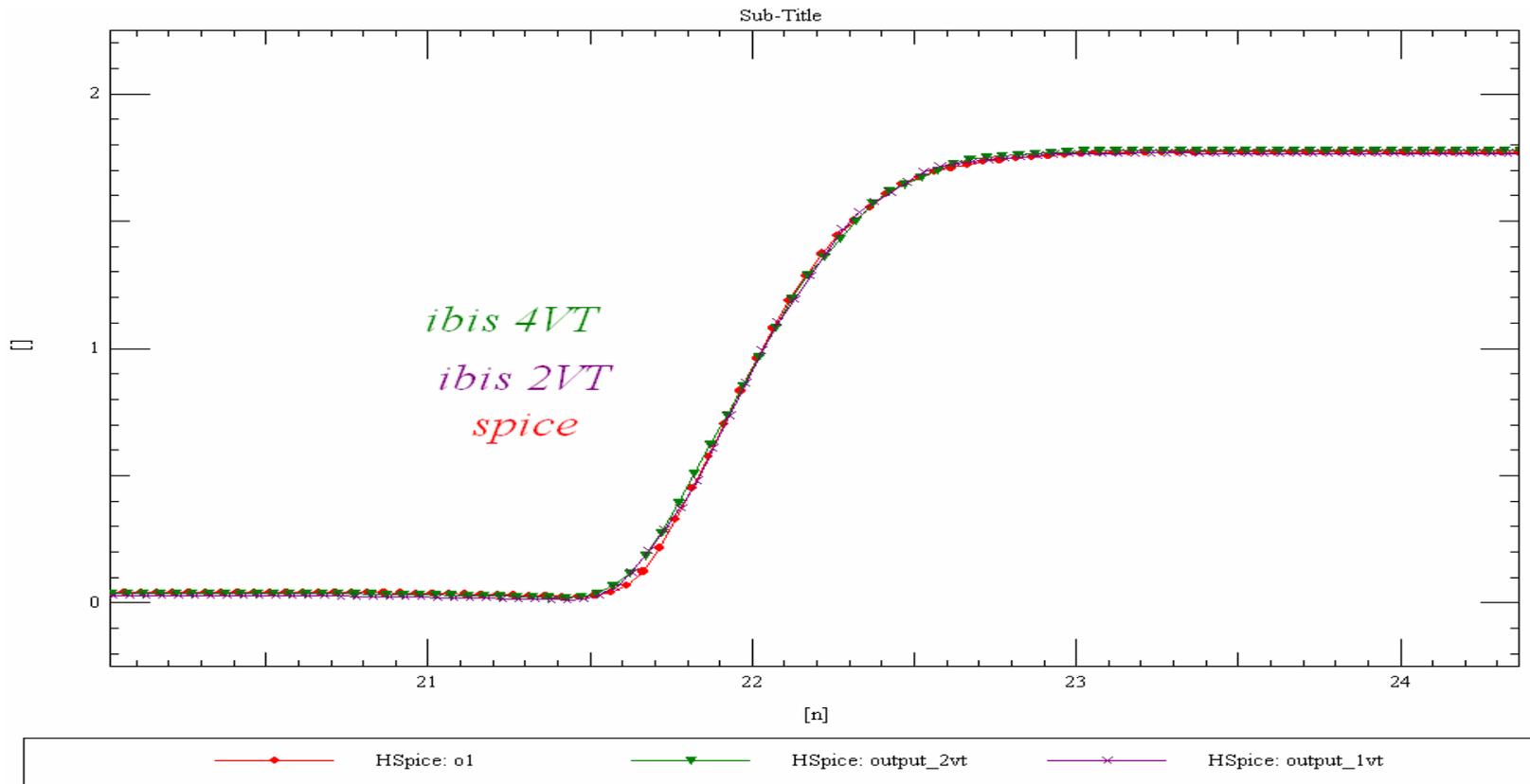 - 1R+1F & R_fixture = 0.50K Ω
  - Using 50 Ω load for test
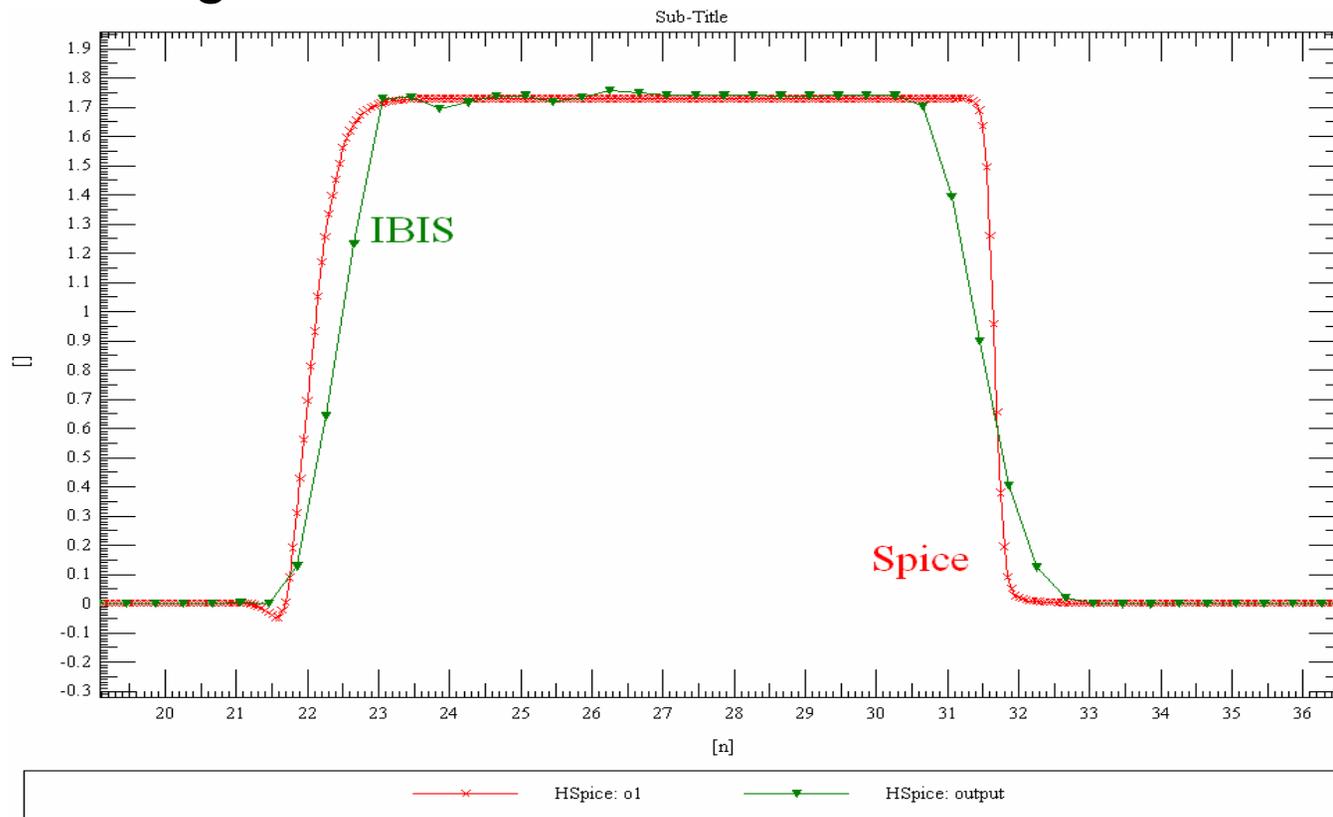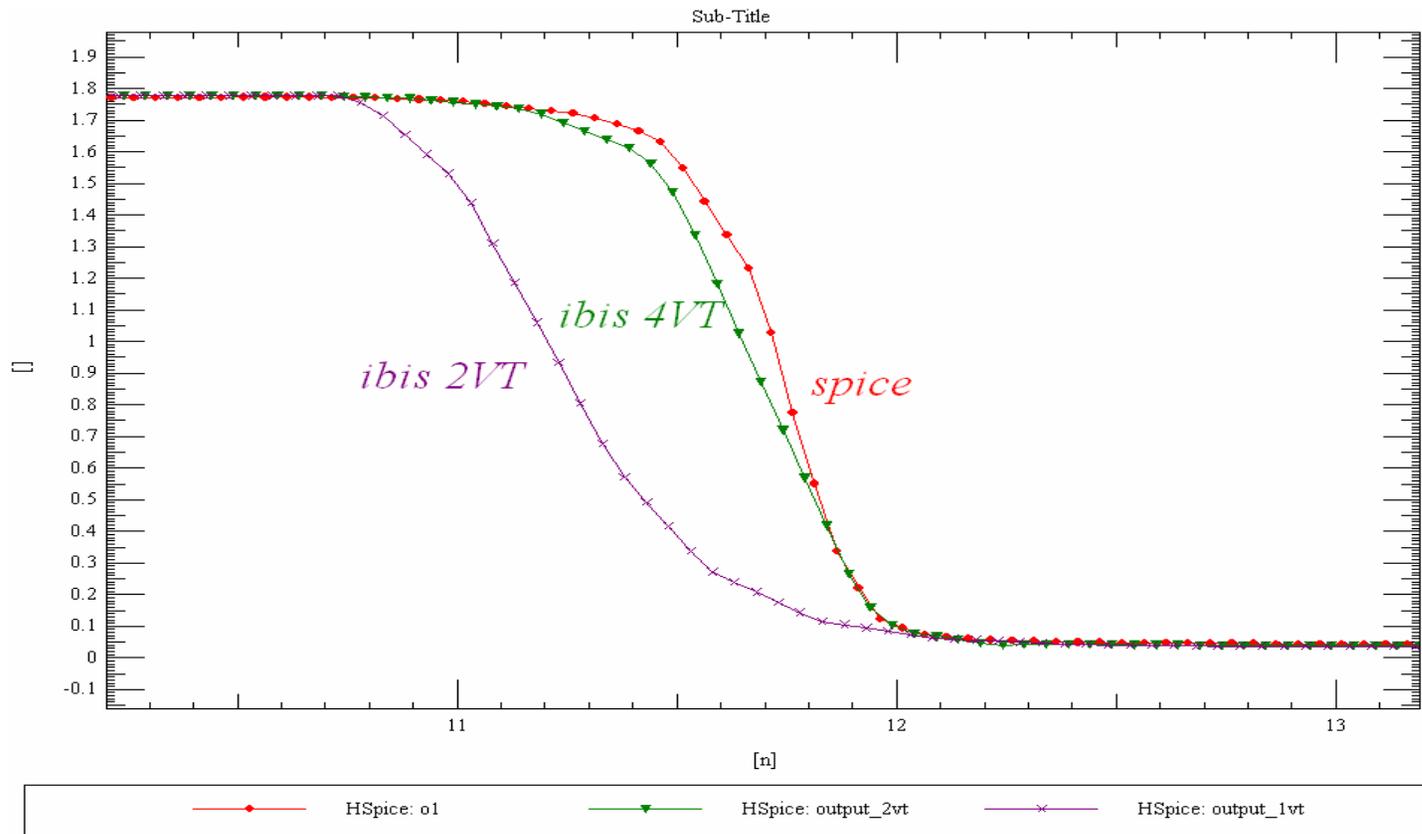
Model adjusting

- Add two V-T curves（2R + 2F）
- R-fixture changed to 50 Ω
- Add More points on V-T curves (lower timestep)

Model test

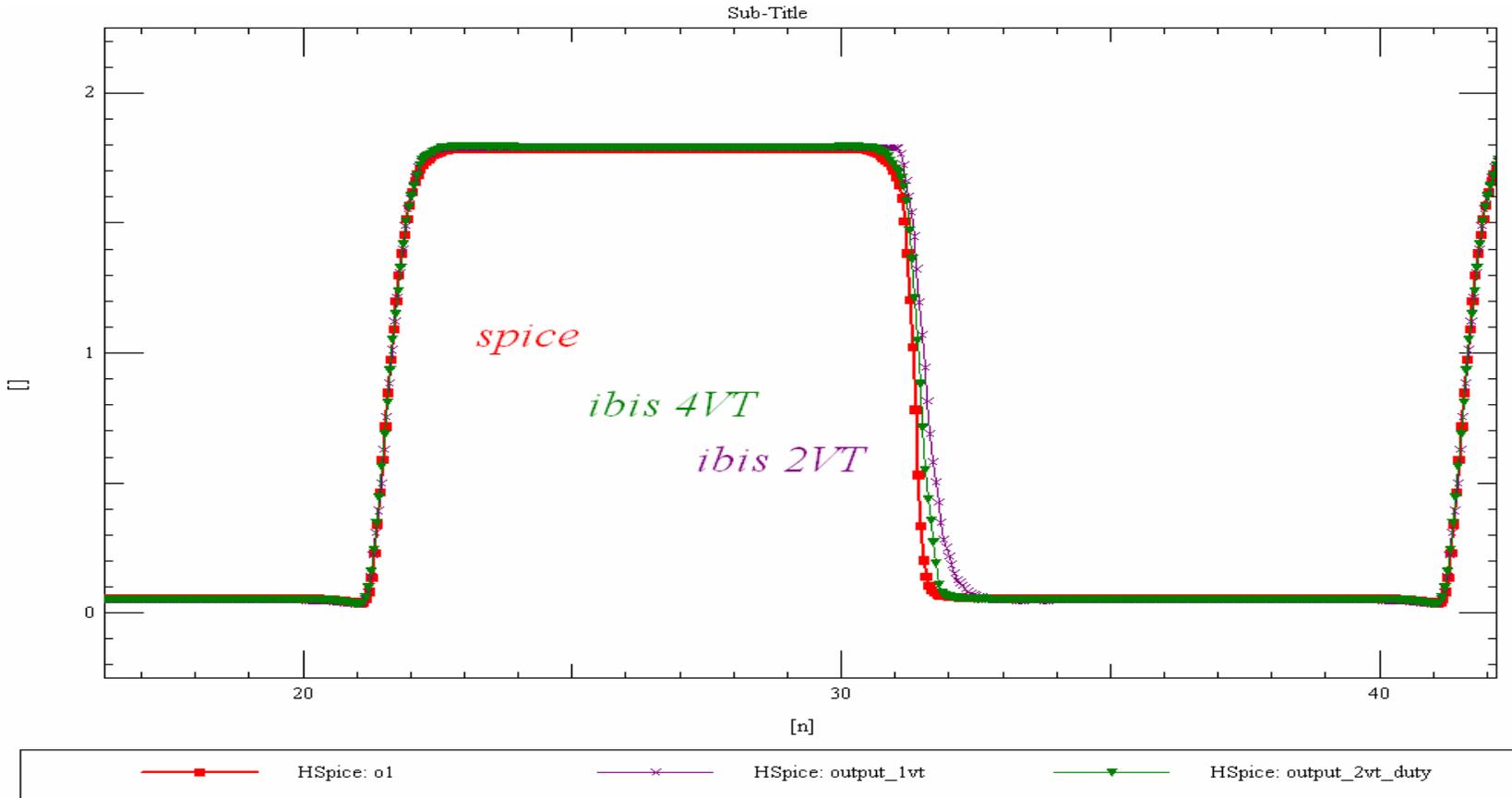- ■ Rising edge matched very well ☺
- ■ No different between 2VT and 4VT

- 4VT Falling edge match good
- 2VT Falling time degrading (460ps → 750ps)

Model test
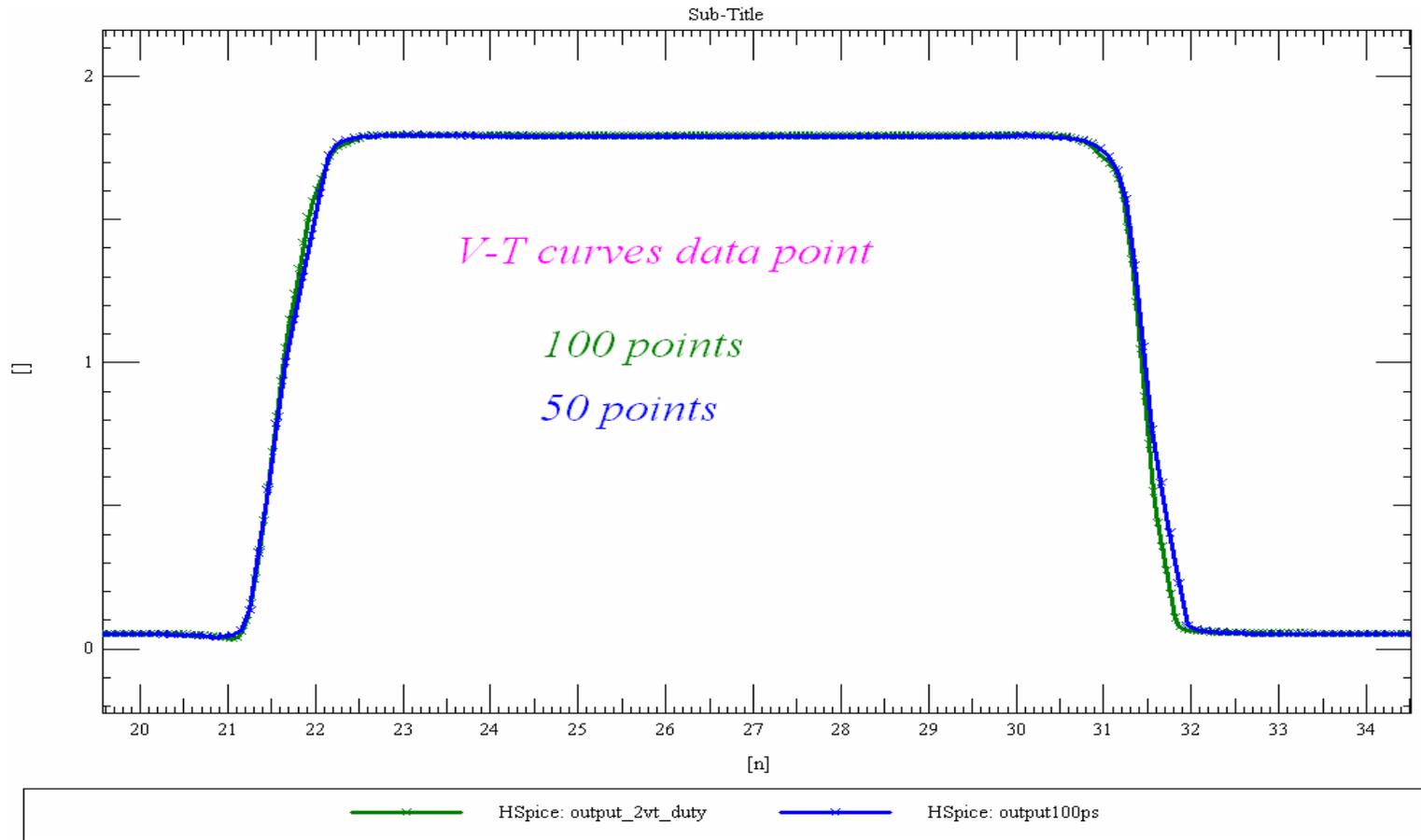
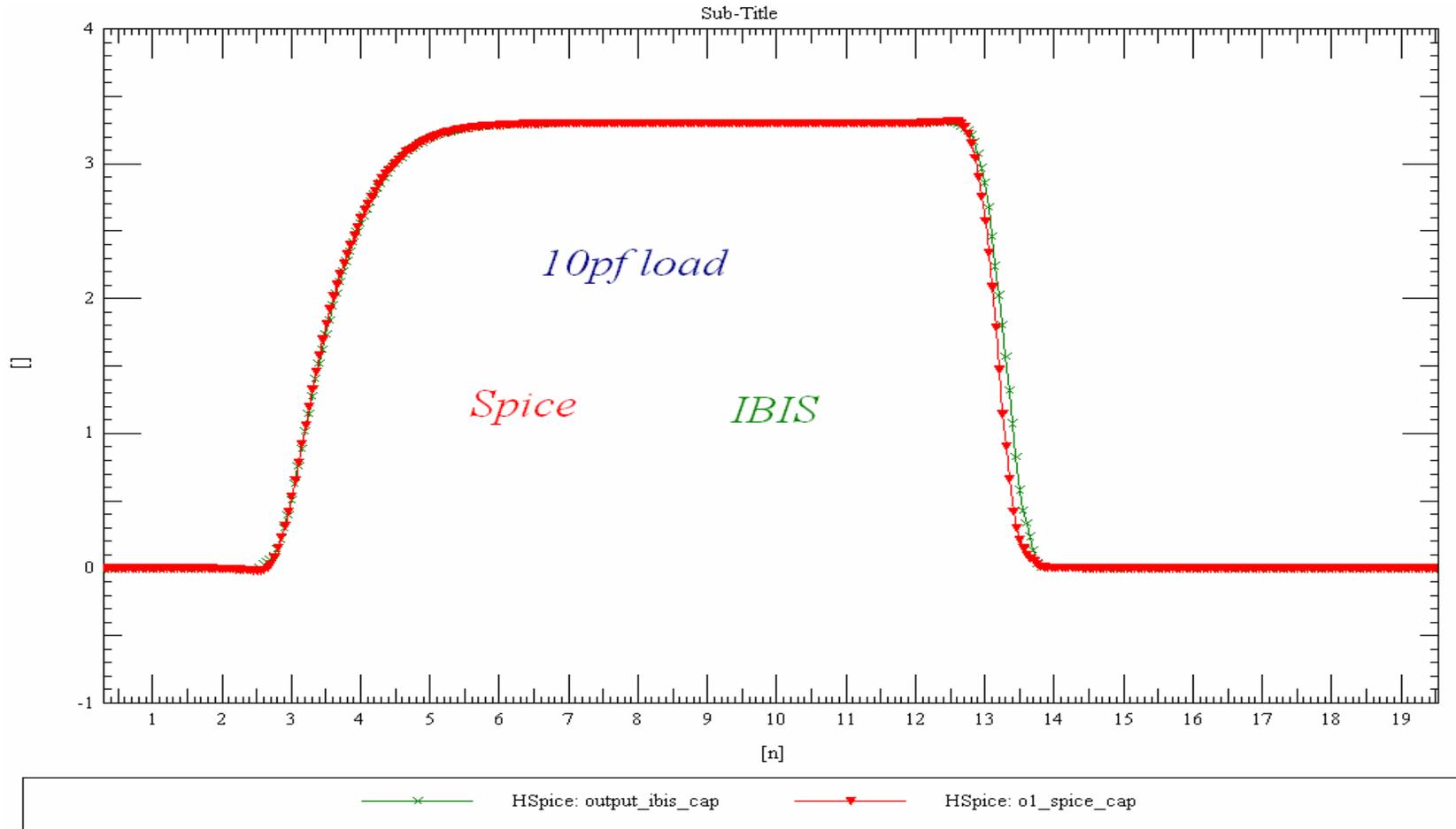## ■ Using 4VT and 2VT tables

Model test

■ **Different V-T data points**

Model test

- ## Capacitor load (using modified model)

Sub-Title

10pf load

Spice   IBIS

HSpice: output_ibis_cap   HSpice: o1_spice_cap

Good model

WRI

■ B model comparison (good model)👍

Conclusion
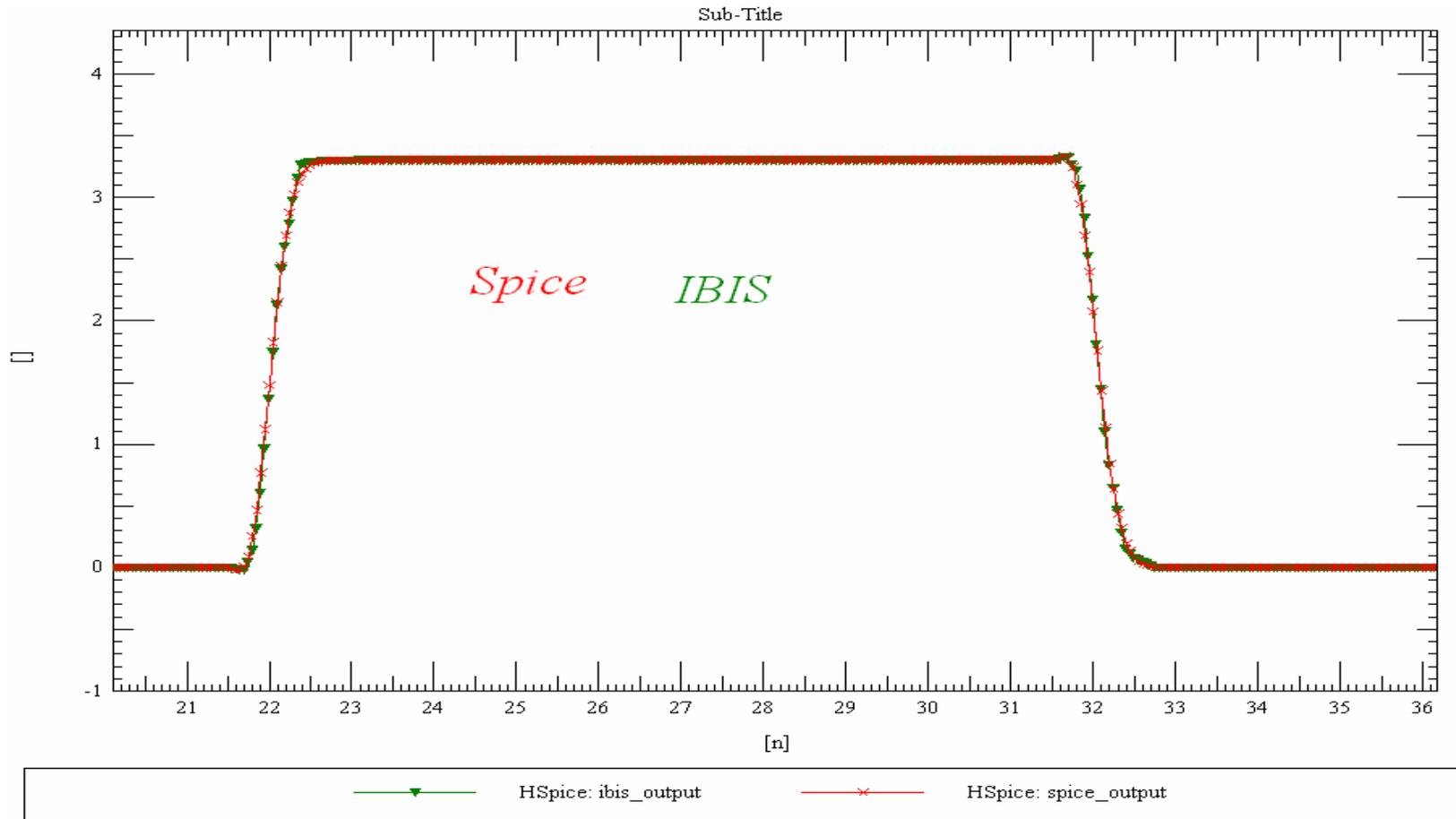
- The waveform shape (edge and DC Level) are very close between IBIS and Spice simulation when the model is correctly generated

- Downloaded models always need careful checking

- Package parameters have great impact on waveform quality

- Power pin's package parameters need more attention