



IBIS Open Forum Minutes

Meeting Date: **October 28, 2015**

Meeting Location: **EPEPS IBIS Summit, San Jose, CA, USA**

VOTING MEMBERS AND 2015 PARTICIPANTS

Altera	[David Banas], Masashi Shimanouchi*, Hsinho Wu*
ANSYS	(Steve Pytel), Curtis Clark
Applied Simulation Technology	Fred Balistreri, Norio Matsui
Avago Technologies	Minh Quach, Leif Zweidinger
Cadence Design Systems	Brad Brim, Joshua Luo, Ken Willis, Joy Li, Ambrish Varma
Cisco Systems	David Siadat, Rockwell Hsu, Bidyut Sen
CST	Stefan Paret, Matthias Troescher
Ericsson	Anders Ekholm
Huawei Technologies	Xiaoqing Dong
IBM	Adge Hawes, Luis Armenta, Dale Becker*
Infineon Technologies AG	Christian Sporrer
Intel Corporation	Michael Mirmak*, Todd Bermensolo, Nhan Phan Gianni Signorini, Chunlei Guo*, Shaowu Huang*
IO Methodology	Lance Wang
Keysight Technologies	Radek Biernacki*, Pegah Alavi*, Colin Warwick Jian Yang, Nicholas Tzou, Heidi Barnes*, Dave Larson Kyla Thomas, Fangyi Rao*
Maxim Integrated Products	Mahbul Bari, Don Greer, Joe Engert, Joe Rayhawk Yan Liang
Mentor Graphics	Arpad Muranyi*, Ed Bartlett, Vladimir Dmitriev-Zdorov*
Micron Technology	Randy Wolff
Signal Integrity Software	Mike LaBonte, Walter Katz*, Todd Westerhoff Mike Steinberger
Synopsys	Ted Mido*, Rita Horner, William Lau, Scott Wedge Michael Zieglmeier, Joerg Schweden
Teraspeed Labs	Bob Ross*, Tom Dagostino
Toshiba	(Yasumasa Kondo)
Xilinx	(Raymond Anderson)
ZTE Corporation	(Min Huang), Tao Guo
Zuken	Michael Schaefer, Markus Buecker, Griff Derryberry Ralf Bruening

OTHER PARTICIPANTS IN 2015

Advanced Semiconductor Engineering	Jane Yan*
Avago Technologies	David Carkeek*, James Church*
Bayside Design	Elliot Nahas
Ciena	Kaisheng Hu*

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eASIC	David Banas*
Freescale	Jon Burnett
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Independent	Tim Wang Lee
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KEI Systems	Shinichi Maeda
Lattice Semiconductor	Xu Jiang
Leading Edge	Pietro Vergine
Microchip Technology	Jeffrey Chou*
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Politecnico di Torino	Stefano Grivet-Talocia*
Qualcomm	Senthil Nagarathinam, Kevin Roselle*
Rambus	John Yan*, Joohee Kim*, Sujit Kumar* Wendem Beyene*
Raytheon	Joseph Aday
SAE International	Chris Denham*, Logen Johnson*
Siemens AG	Boris Kogan, Michael Flint
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Technische Universität Hamburg-Harburg	Jan Preibisch
University of Illinois	Jose Schutt-Aine*
Vitesse	Siris Tsang
ZI Consulting	Iliya Zamek*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 9, 2015	Asian IBIS Summit Shanghai – no teleconference	
November 13, 2015	Asian IBIS Summit Taipei – no teleconference	
November 16, 2015	Asian IBIS Summit Tokyo – no teleconference	
November 20, 2015	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

<https://ciscosales.webex.com/ciscosales/j.php?J=205475958>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in San Jose, California at the DoubleTree by Hilton Hotel following the 2015 EPEPS conference. About 34 people representing 20 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/oct15/>

Michael Mirmak opened the Summit on behalf of Mike LaBonte and the IBIS Open Forum board. After some brief announcements, each of the attendees introduced themselves. Michael thanked the sponsors EPEPS, Keysight Technologies, Mentor Graphics Corporation, and Synopsys for their support.

Bob Ross presented Chris Denham of SAE with a recognition gift (an IBIS mug) in honor of his upcoming retirement and 13 years of service to IBIS as the liaison with GEIA and SAE.

IBIS CHAIR'S REPORT

Mike LaBonte, SiSoft

Michael Mirmak presented. He provided an overview of the history of IBIS, including both the IBIS specifications and major features of each version. He also summarized the other specifications (ICM, IBIS-ISS, Touchstone) issued by IBIS as an organization. The new [ibis.org](http://www.ibis.org) website was announced, and the progress made by IBIS task groups toward supporting new features was presented. No questions were asked.

SPI2016 20TH IEEE WORKSHOP ON SIGNAL AND POWER INTEGRITY

Stefano Grivet-Talocia, Politecnico di Torino, Italy

Stefano Grivet-Talocia presented on the plans and venue for the 2016 SPI IEEE Workshop. He provided a quick summary of the SPI location, Torino (Turin), including arrangements for accommodations and transportation. He also covered the technical program schedule for the

week. The event takes place from May 8 through May 11, 2016 (Sunday through Wednesday), with the IBIS Summit taking place on Wednesday.

New features include an Industry Forum, to "present problems, not solutions." EDA vendors and academic representatives will be excluded, but other industry participants will be invited; the EDA and academic communities will be involved after the summary issues have been assembled. No papers for the forum will be required. The submission deadline is January 31, 2016 with notification of acceptance by February 28, 2016.

TURIN AND ITS PROVINCE (MOVIE)

Stefano Grivet-Talocia, Politecnico di Torino, Italy

Stefano Grivet-Talocia showed a brief video showcasing Torino as the location for the 2016 SPI IEEE Workshop.

SAE, ITC, AND IBIS

Logen Johnson, SAE International

Logen Johnson provided a brief overview of SAE and the SAC ITC. SAE maintains offices in Warrendale, PA (headquarters) as well as Shanghai and London. SAE was formed in 1905 as the Society of Automotive Engineers, but included aerospace in 1916 and more recently rebranded as "SAE".

SAE has two affiliate organizations: Performance Review Institute and SAE ITC (Industry Technologies Consortia), the latter of which can act more as a trade consortium/group. ITC can take advantage of SAE International's Legal, Financial, Publication, etc. resources.

Michael Mirmak asked about individual versus entity-based membership and SAE versus SAE ITC membership. Logen confirmed that ITC is based on entities, while SAE is based on individual membership.

ENHANCED MACROMODELS FOR I/O BUFFERS

Gianni Signorini*, Claudio Siviero**, Igor Simone Stievano**, and Stefano Grivet-Talocia**, *Intel Corporation and University of Pisa, ** Politecnico di Torino

Stefano Grivet-Talocia presented on behalf of Gianni Signorini, pointing out that the presentation is "not against IBIS" but a proposal to improve it, particularly the traditional IBIS treatment of power delivery effects.

The proposed macromodeling approach involves both the PDN and V_{dd} , and I_{dd} with respect to time, as well as the V_{out} and I_{out} behaviors of single-ended buffers. The input to the buffer can be a voltage or some more abstract data (e.g., event-driven simulator). The macromodel represents currents i_{out} and i_{dd} with respect to time as functions of input, v_{out} and v_{dd} , all with respect to time. Objectives include being SPICE-compatible and fast. i_{out} and i_{dd} are weighted sums of high and low logic state currents; the weights represent the switching, while the

currents cover events while not switching. i_{dd} must include currents from v_{dd} and the sink/reference that do not involve the output.

David Banas asked about why i_{dH} and i_{dL} are required if δ_i is also there. Stefano answered that δ_i represents the current (potentially crowbar) due to mismatches between H (high) and L (low) timing.

Today's IBIS is static, while the proposal covers more dynamic behaviors. Noisy supply rails can be inaccurately captured by IBIS 5.0 power aware keywords in its static assumptions. A 3D surface is proposed, to cover the relationship of currents between I_{dd} and output, with high and low states. An attendee suggested that the PDN was mainly inductive. Stefano suggested it was low-frequency inductive, but is otherwise "a mess". To compress the matrix data from sweeping, using SVD (singular value decomposition) is proposed to compact/truncate the incoming data. Dynamic effects are included using an assumed-linear rational approximation, in the time domain. Non-linearities will be captured by the 3D matrix. MISO (multi-input, single-output) computed/fitted models are used. Typical devices need 3-4 poles, instead of the single pole represented by C_{comp} . V_{dd} increasing will shorten the switching delay, which is not captured in IBIS today, but can be captured if the weighting functions include both time and v_{dd} as inputs.

Implementation is in an MPILOG model, which can be implemented using Verilog-A, SPICE, or [External Model] in IBIS. IBIS Version 5.1/6.0 compliance directly can be assured by using only a row and column of the original data. Transistor-level vs. IBIS speed up is 1500x, but MPILOG is 350x. Examples were shown where IBIS timing and power representation falls behind the MPILOG representation. Differential buffers may be linear today, but may not be in the future, due to the way the buffer is being stimulated. Differential adds a four-dimensional surface.

An example of a low voltage mode buffer showed the major impact of power supply modulation on output signaling.

ACCURATE STATISTICAL ANALYSIS OF HIGH-SPEED LINKS WITH PAM-4 MODULATION

Vladimir Dmitriev-Zdorov, Mentor Graphics

Vladimir Dmitriev-Zdorov summarized the initial portion of his slides, as the material was presented earlier during EPEPS, and many of the attendees were also at the Summit. He presented how step response samples can include effects such as jitter (variations at each sample point), and can be summed in a single equation that represents the eye diagram. Irregular sampling can be used in the presence of deterministic Tx jitter. All of this can be done to simulate statistically the behavior of the entire system. Effects that can be covered include random TX and RX jitter, deterministic jitter, and edge rate variations (asymmetry for PAM-2 or different edges in the 6 possible for PAM-4). Data-dependent jitter can also be included. Vladimir showed the state variations possible for PAM-4 modulation, which is 4^N .

Peak distortion can be used to determine the vertical (voltage) PDFs at the various levels, without jitter. They must be linear in equalization, without crosstalk (or at least not correlated with the input pattern). Optimum sampling is, in essence, a function of horizontal position (finding the peak).

For IBIS-AMI, statistical analysis requires LTI assumptions from impulse response, but for non-LTI channels, we can build a vertical histogram (p. 17). Sufficient bits -- 2000 to 4000 -- can be generated and used via sampling to generate a vertical histogram to create a PAM-4 set of thresholds.

Statistical analysis can be used to generate SER and BER. SER is the symbol error ratio and can be combined with Gray code mapping to convert to BER. An equation for PAM-4 SER calculation was provided.

Michael Mirmak asked about "non-LTI channels." Vladimir responded that the driver was intended here as the source of the non-LTI-ness. Bob Ross asked about page 9, where he suggested 64 transitions should be allowed. Vladimir stated these were mathematical transitions, but only 32 are unique if statistical symmetry is assumed.

Another question was asked about eye diagrams using bit-by-bit analysis: what effects are not captured in a statistical eye versus bit-by-bit? Vladimir suggested that unbounded jitter could be generated as part of linearization of jitter assumptions when a statistical process is used.

IBIS INTERCONNECT BIRD UPDATE

Walter Katz, SiSoft

Walter Katz opened his presentation by noting that current package/interconnect modeling in IBIS is only lumped coupled RLC or lossless uncoupled distributed models, neither of which is particularly useful today. IBIS-ISS was developed to address interconnect using generic SPICE (donated by Synopsys) without transistor models. A question was raised about solvers which may not support SPICE or HSPICE. EDA vendors, according to Walter, agreed that the IBIS-ISS format is indeed common between them. A key concept involved today is that on-die signal, package, and supply interconnects can be separated.

The fundamental assumption is that the package or interconnect vendors will not change how they model these structures; the requirement is only that they include explicit descriptions of the terminals. Pins and pads, in response to a question, were clarified to cover device to board and buffer to device connections, respectively.

A question was asked about modeling interposers (e.g., a mezzanine). Walter prefers to think of these as modules. Arpad Muranyi pointed out that IBIS-ISS allows nesting of subcircuits, so interposers can be incorporated at multiple levels within the circuit description. Walter provided several examples showing the terminal assignments, where power or signal groups can be modeled, or both. Touchstone can be used to express the circuits, but the reference must be made explicit.

A question was asked if one can pass parameters other than length. Walter responded that yes, anything that can be supported by SPICE parameter passing can be passed into a model, including text strings.

SOME RESULTS FOR GENERAL K-TABLE EXTRACTION PROPOSAL USING SPICE

Bob Ross*, Xuefeng Chen**, *Teraspeed Labs, **Synopsys

Bob Ross' presentation provides a simplified alternative to Stefano Grivet-Talocia's approach to generating prototype IBIS K-table data. This is based on the standard push-pull IBIS model approach, where power is fixed, not variable. The approach assumes fixed C_comp and known pin R, L, and C information. The approach also assumes iterative or looped feedback to convergence. This requires SPICE features that are not universal (not part of IBIS-ISS), such as tables and feedback loops. Source code for SPICE was shown, including transmission line loads and pulse (step) stimulus patterns.

Bob noted that generalized C_comp can be supported, but any series R must be de-embedded. A K-amplifier will adjust to zero out the difference between the load and the voltage at the sense point. An alternative is to derive an IBIS model at the C_comp subcircuit terminal with appropriate K-tables.

Stefano asked about stability issues with the feedback loop. Bob showed several examples, including the standard IBIS ideal ramp, and reactive fixtures (L, C). The unstable case involves a package subcircuit alone, with no C_comp model but Lpkg and Cpkg defined and non-zero. The voltage out requires a discontinuity to cover the continuous slope and both reactive elements. S-parameter testing did in fact work, but only for delay-less structures. Feedback multiplier values did not have an impact. Having large L and C values are unlikely to generate smooth transitions in any case; the test may be unrealistic. The entire scheme fails for t-line models due to delays in the feedback loops.

David Banas asked about future plans. Bob plans on trying more complex C_comp models with 3-4 poles and more extreme values. Walter Katz suggested the V-t tables that are being matched must include the C_comp that is being extracted.

A question was asked about complex packages and including them in the channel: is there anything wrong with this methodology? Bob suggested that deriving the IBIS model without the package model is ideal.

IBIS-AMI MODELLING OF HIGH-SPEED MEMORY INTERFACES

John Yan, Arash Zargaran-Yazd, Rambus

John Yan presented. For today's high-speed memory, equalization is needed (in addition to ODT), similar to SerDes link generation, with fairly stagnant channels. There are VGA, CTLE, and AFE (analog front end) elements. Speeds of 2.4 and 6.4 Gbps will be demonstrated. Multi-drop environments are atypical of IBIS-AMI usage. Higher speeds lead to less capacity per channel, getting closer to point-to-point topology; higher capacities actually constrain the speeds in a non-linear fashion.

To represent a two-RX load system within IBIS-AMI, the channel using a passive load and ODT can be combined with the rest of the (active) channel. An encapsulated channel approach can be shown to provide the same pulse response as the full multi-drop channel.

System identification can be used to model the AFE from SPICE simulations, extracting the

transfer function. DDR4 with CTLE at the RX example was shown compared to SPICE simulations. There was a 1000x speed improvement, with ~5% or less difference in results for 2.4 Gbps. For 6.4 Gbps, DFE at the RX and de-emphasis at the TX may be needed (beyond DDR4).

Walter Katz asked if a future JEDEC standard would incorporate equalization at the memory device side, as opposed to the controller side (where it already exists). John responded that he was not in a position to speak specifically to standardization.

Arpad Muranyi asked if for multi-drop, would AMI models only be at one RX, both, or at the TX. John responded that encapsulation captures the effects, but multi-ranks would use ODTs for the ternary receivers.

Walter asked whether scrambling is assumed. Clock forwarded or DQS may not be enough or may be needed per channel. There was some discussion of whether scrambling assures suitable density for CDR.

Michael Mirmak asked about encapsulation assuming LTI for superposition, particularly on the secondary channel.

A question was asked if tool vendors are automating multi-drop AMI modeling. John responded yes, though JEDEC support is expected/needed according to Walter. David Banas suggested support required combing IBIS and IBIS-AMI in tools. John replied that he would expect tool vendors to provide this kind of multi-drop support in the future.

IBISAMI – AN OPEN SOURCE, PUBLIC DOMAIN IBIS-AMI MODEL CREATION INFRASTRUCTURE

David Banas, eASIC

David Banas pointed out that his presentation has nothing to do with eASIC. IBIS generation is boring today. Either the tools handle it, or it's represented as best practices. How do the model makers show how clever they are in such an environment? Competitive differentiation can be enabled through a common resource, in this case, the ibisami package. Common code across many vendors requires redundant maintenance. Exceptions include adaptive CDRs and DFEs.

A common approach today uses machinery that generates source code using architecture. Here, the approach is different - everything is parameterized (e.g., Tx FIR pre-emphasis template). A Rx CTLE template uses peak locations/magnitudes, but this may be insufficient. DFE is also supported. A single makefile can be used for three OSes.

Limitations of the approach include that it is statistical only (no GetWave); there is no time-domain adaptation for CDR or DFE; there is a fixed number of CTLE poles/zeros. No non-linear behavior (e.g., Tx output driver saturation) is included. David requested that contributions fork rather than copy code, to help with integrating improvements.

David's examples include coverage of different samples/bit settings, to avoid a common problem in today's models in the industry. No variation was seen. A separate package was

used to test IBIS-AMI models. DFE does not use GetWave; it works by sending in zeros and then seeing what DFE values are needed to bring it to the target value.

A question was asked if this approach requires clock steps. David answered no, as this is Init only. The overall approach is based on a 2008 paper from DesignCon by SiSoft.

Michael Mirmak asked whether the DFE adaptation was also called "zero-forcing" in the industry. Some attendees confirmed this. Arpad Muranyi asked about CTLE modeling. David noted that the CTLE has one zero and two poles, but TX is arbitrary. The DFE must be linear.

David noted that his project had no other participants yet as developers.

INTRODUCING IBIS VERSION 6.1

Michael Mirmak, Intel Corporation

Michael Mirmak gave a brief overview of the major changes in IBIS Version 6.1, covering both the AMI and traditional IBIS portions. For the IBIS-AMI areas, model dependencies are supported, PAM-4 is included, and bi-directionality is explicitly included. For traditional IBIS, initial delays are explicitly defined to assist with overclocking, and clarifications are made to package diagonals and package pin assignments for power delivery.

David Banas asked whether duobinary was specifically excluded and whether any demands had been made on the IBIS Open Forum to include support. Michael and the other participants confirmed that no requests had so far been made, but that a similar approach as used for PAM-4 could be enabled. David also asked whether any support for trailing delay removal is planned, as this might be more important to provide than initial delay support for overclocking. In general, the participants agreed that this would be less of interest as most tools can handle automatic removal of settled V-t data.

CLOSING REMARKS

To close the summit, Michael Mirmak reminded the participants about the upcoming IBIS Open Forum teleconference on November 20. He again thanked the co-sponsors EPEPS, Keysight Technologies, Mentor Graphics Corporation and Synopsys.

Bob Ross moved to adjourn. Radek Biernacki seconded. The meeting was adjourned at approximately 5:45 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held November 20, 2015. The following IBIS Open Forum teleconference meeting will be held December 18, 2015. The Asian IBIS Summit in Shanghai will be held November 9, 2015. The Asian IBIS Summit in Taipei will be held November 13, 2015. The Asian IBIS Summit in Tokyo will be held November 16, 2015. No teleconferences will be available for the Summit meetings.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to ibis-info@freelists.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: `ibischk6`, `tschk2`, `icmchk1`, `s2ibis`, `s2ibis2` and `s2iplt`.

The BUG Report Form for `ibischk` resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>
<http://www.ibis.org/bugs/ibischk/bugform.txt>

The BUG Report Form for `tschk2` resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for `icmchk` resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report `s2ibis`, `s2ibis2` and `s2iplt` bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>
<http://www.ibis.org/bugs/s2iplt/bugsplt.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on [ibis.org](http://www.ibis.org) for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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IBIS – SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	September	October 2,	October	October 28,
			11, 2015	2015	23, 2015	2015
Altera	Producer	Active	X	X	X	X
ANSYS	User	Active	X	X	X	-
Applied Simulation Technology	User	Inactive	-	-	-	-
Avago Technologies	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	-	X	-
Cisco Systems	User	Inactive	-	-	-	-
CST	User	Inactive	-	X	-	-
Ericsson	Producer	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	-
IBM	Producer	Inactive	X	-	-	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Inactive	X	-	-	X
IO Methodology	User	Active	X	X	X	-
Keysight Technologies	User	Active	X	X	X	X
Maxim Integrated Products	Producer	Active	X	X	X	-
Mentor Graphics	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	-
Signal Integrity Software	User	Active	X	X	X	X
Synopsys	User	Active	-	X	X	X
Teraspeed Labs	General Interest	Active	X	X	X	X
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	-

I/O Buffer Information Specification Committee (IBIS)

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH SAE BALLOT VOTING ARE:

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