

Current Status - IBIS 4.1 Macro Library for Simulator Independent Modeling

presented by
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IBIS-Macro Working Group

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Agenda

- **Origins of IBIS-Macro**
- **IBIS-Macro concept**
- **Status at last meeting**
- **Recent activities**
- **Current issues**
- **Next steps**

Origins

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- **IBIS hasn't kept up with new I/O technologies**
 - SPICE use for SI is steadily increasing
- **IBIS 4.1 supports AMS, but adoption has been slow**
 - AMS is powerful, but also complex
- **Macro modeling proposed as alternative to full AMS implementations**
 - Proposed by Donald Telian of Cadence, Jan 2005
 - Original proposal used Berkeley SPICE extensions
- **Study group formed in Mar 2005 to explore macro modeling concept in IBIS**

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Vendor / Tool / Language Survey

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Tool #	Verilog-A	Verilog-AMS	VHDL-AMS
1	✓		
2			
3			
4			✓
5	✓		
6	✓	✓	✓
7	✓	✓	✓
8	✓	✓	✓
9			
10			
11	✓		
12	✓		

- **Current status of 12 popular "SI" tools and their -AMS language support**
- **Goal: develop a strategy that supports advanced modeling across all these combinations**

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IBIS-Macro Goals

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- **Drive IBIS to support advanced technologies**
- **Multi-simulator support**
 - Same as original IBIS, tool-independent models
- **Speed EDA/semiconductor adoption of advanced behavioral modeling techniques**
- **Leverage existing skills**
 - Most model developers are familiar with Spice-style macro modeling

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Macro Models

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- **Instantiate blocks with pre-defined functions and behaviors**
- **Parameterize those blocks by passing values into the elements**
- **Interconnect blocks using a netlist-type syntax**
- **Define external ports to the model using the netlist syntax**

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IBIS-Macro Concept

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- Library of AMS “elements” instantiated and interconnected to create complex buffer models
- AMS elements modeled after sources and elements found in popular SPICE tools
- Ensure elements can be implemented by substitution in SPICE-only engines
- Standardize AMS element library across semiconductor model providers
- Collection of reference “templates” instantiate AMS elements to address common modeling issues (e.g. pre-emphasis buffer)

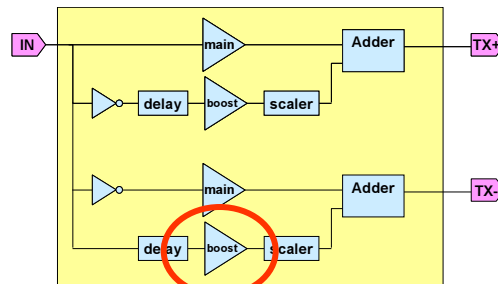
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IBIS-Macro Element Mapping

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Verilog-AMS Simulator

```
'include ".Macro_lib\No_ODT_OUTPUT_data.dat"
IBIS_OUTPUT #( "OUTPUT_data",
               .Max_dt(Max_dt_val),
               .Vth_R(Vth_R_val),
               .Vth_F(Vth_F_val)) \
B1 (Power, Ground, Pad, In_D, Power, Ground);
```

VHDL-AMS Simulator

```
IBIS_OUTPUT1 : entity MacroLib.IBIS_OUTPUT(IBIS_2EQ2UK)
generic map ( DataFile => ".\Macro_lib\No_ODT_IO_data.txt" )
port map ( PU_ref => Power,
          PD_ref => Ground,
          Pad => Output,
          In_D => Input,
          PC_ref => Power,
          GC_ref => Ground );
```

SPICE Simulator

```
b_io PUFrefB PDrefB IoB InB En PCrefB GCrefB
+ file='mybuf.ibs' model='mybuf' +power=on buffer=2
```

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Status at Last Meeting

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- **Preliminary library in place**
- **Recruiting semiconductor vendors to test library**
- **Looking for additional model templates**
 - Initial set contributed by Cadence
- **Looking for resources to help with automated model translation / reformatting**

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Recent Activities

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- **Ongoing weekly meetings**
- **Final coding / testing of element library**
- **Driving EDA tool compatibility**
- **BIRD100.2 accepted**
- **Recruited Paul Fernando (NCSU) to help with model translation issues**
- **Released library versions 1.0 (Verilog-A and VHDL-AMS)**
 - www.eda.org/pub/ibis/macromodel_wip/

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Tool Development

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Documentation Tool

```
~/IBIS/macromodel/macromodel_wip/tools/macro_lib.doc
~/IBIS/macromodel/macromodel_wip/tools/macro
$ perl moduledoc.pl IBIS_macro_library.xml IBIS_macro_library.vhd
Reading XML file IBIS_macro_library.xml
File IBIS_macro_library.vhd moved to IBIS_macro_library.1.vhd for
Annotating VHD file IBIS_macro_library.vhd
55 modules annotated
=====moduledoc=====
--
-- MODULE:      IBIS_R (p, n)
--
-- DESCRIPTION:
--   A simple resistor. The resistance value is calc
--   R = Rval * Scale
--
-- TERMINALS:
--   p          positive resistor terminal
--   n          negative resistor terminal
--
-- PARAMETERS:
--   Rval       Resistance value
--              DEFAULT Rval = '1.0'
--   Scale      Scaling factor for calculating resistance value
--              DEFAULT Scale = '1.0'
```

Model Data Extraction Tool

```
~/IBIS/macromodel/macromodel_wip/work/paulfer/paulfer
~/IBIS/macromodel/macromodel_wip/work/paulfer
$ perl conv.pl lab_1.ibs io50v
No process corner selected. Defaulting to typical.
Typical: t Min=n Max=x
// Generated on: Time: 8:54:17 Date: 2/1, 2006
// Verilog-A primitive: IBIS_INPUT
define ibis_params \
.C_comp(O), \
.Vinh(2.000), \
.Vinl(800.000E-3), \
define IV_data \
.IVpc_length(100) \
.IVpc(17.05273790E+0, 6.19755316E+0, 6.17265699E+0, 5.44273139E
1, 5.37641265E+0, 4.73848157E+0, 4.69708416E+0, 4.65569034E+0, 4
4352596E+0, 4.00219833E+0, 3.50668107E+0, 3.45717593E+0, 3.4159
90E+0, 2.92976715E+0, 2.88861979E+0, 2.51053701E+0, 2.46129230E
2, 2.08441639E+0, 2.04332838E+0, 2.01083906E+0, 1.70904725E+0,
6022958E+0, 1.38440932E+0, 1.36014901E+0, 1.35206540E+0, 1.1023
71E+0, 1.08633599E+0, 870.87825200E-3, 855.01209670E-3, 775.920
81500E-3, 689.44963020E-3, 658.16726690E-3, 642.56231960E-3, 61
2.67390930E-3, 549.5129110E-3, 534.11418370E-3, 495.77687350E-3,
3.465.28787620E-3, 427.43371130E-3, 412.38094520E-3, 389.90712
820E-3, 316.07214230E-3, 301.54151470E-3, 265.63929580E-3, 258.
46978750E-3, 244.43078790E-3, 223.51351340E-3, 216.61282330E-3,
189.41631990E-3, 169.50520180E-3, 156.50043060E-3, 143.7393486
0E-3, 121.35026220E-3, 110.06516230E-3, 107.23320160E-3, 95.72
```

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Current Issues

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- **Significant compatibility issues identified with AMS implementations in different EDA tools**
 - Understandable, considering relative age of –AMS language and EDA implementations
- **Discussions on best way to proceed**
 - Discard macro modeling, rely on native AMS
 - Document needed AMS language subsets in Verilog and VHDL
 - Proceed as planned, using macro library as *de facto* subset documentation and test case
 - Proceed as planned, have macro library explicitly defined as compliance test suite

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Next Steps

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- **Continue analog-only vs. full-AMS discussion**
- **Drive EDA tool improvements for language support**
- **Seek additional semiconductor and EDA vendor participation**
- **Create additional templates, determine if additional building blocks are needed**

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For More Information

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- **IBIS-Macro Website**
 - www.eda.org/pub/ibis/macromodel_wip/
- **IBIS-Macro mail reflector**
 - Mail to: ibis-macro-request@freelists.org
 - Subject: **subscribe**
- **IBIS-Macro mail archives**
 - www.freelists.org/archives/ibis-macro

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