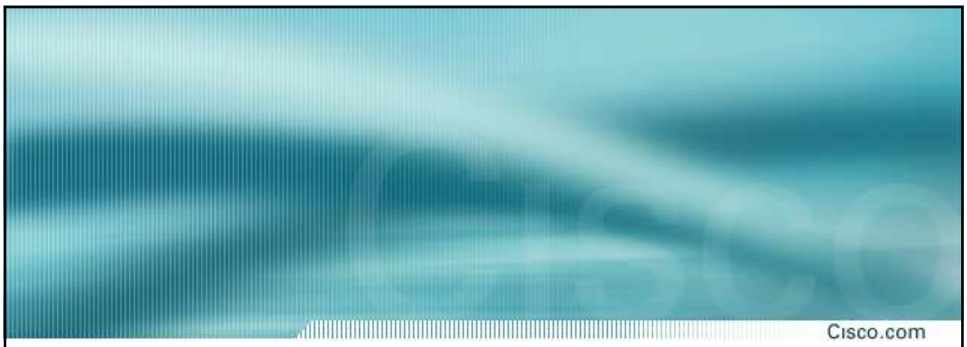

Current Status - IBIS 4.1 Macro Library for Simulator Independent Modeling

presented by
Todd Westerhoff, Cisco Systems

IBIS-Macro Working Group

Intel - Arpad Muranyi	Cadence - Ken Willis
Cisco - Mike LaBonte, Todd Westerhoff	Mentor Graphics - Ian Dodd
NC State University - Paul Fernando	Sigrity - Sam Chitwood
SiSoft - Barry Katz, Walter Katz	Teraspeed - Scott McMorrow, Bob Ross

Agenda

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- Origins of IBIS-Macro
- IBIS-Macro concept
- Status at last meeting
- Recent activities
- Current issues
- Next steps

Origins

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- IBIS hasn't kept up with new I/O technologies
  - SPICE use for SI is steadily increasing
- IBIS 4.1 supports AMS, but adoption has been slow
  - AMS is powerful, but also complex
- Macro modeling proposed as alternative to full AMS implementations
  - Proposed by Donald Telian of Cadence, Jan 2005
  - Original proposal used Berkeley SPICE extensions
- Study group formed in Mar 2005 to explore macro modeling concept in IBIS

Vendor / Tool / Language Survey

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Tool #	Verilog-A	Verilog-AMS	VHDL-AMS
1	✓		
2			
3			
4			✓
5	✓		
6	✓	✓	✓
7	✓	✓	✓
8	✓	✓	✓
9			
10			
11	✓		
12	✓		

- Current status of 12 popular "SI" tools and their –AMS language support
- Goal: develop a strategy that supports advanced modeling across all these combinations

IBIS-Macro Goals

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- Drive IBIS to support advanced technologies
- Multi-simulator support
  - Same as original IBIS, tool-independent models
- Speed EDA/semiconductor adoption of advanced behavioral modeling techniques
- Leverage existing skills
  - Most model developers are familiar with Spice-style macro modeling

Macro Models

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- Instantiate blocks with pre-defined functions and behaviors
- Parameterize those blocks by passing values into the elements
- Interconnect blocks using a netlist-type syntax
- Define external ports to the model using the netlist syntax

IBIS-Macro Concept

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- Library of AMS “elements” instantiated and interconnected to create complex buffer models
- AMS elements modeled after sources and elements found in popular SPICE tools
- Ensure elements can be implemented by substitution in SPICE-only engines
- Standardize AMS element library across semiconductor model providers
- Collection of reference “templates” instantiate AMS elements to address common modeling issues (e.g. pre-emphasis buffer)

IBIS-Macro Element Mapping

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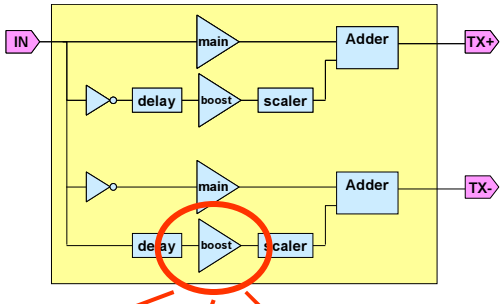

Verilog-AMS Simulator

```
`include ".\Macro_lib\No_ODT_OUTPUT_data.dat"
IBIS_OUTPUT  #(`OUTPUT_data,
                .Max_dt(Max_dt_val),
                .Vth_R(Vth_R_val),
                .Vth_F(Vth_F_val)) \
   B1  (Power, Ground, Pad, In_D, Power, Ground);
```

VHDL-AMS Simulator

```
IBIS_OUTPUT1 : entity MacroLib.IBIS_OUTPUT(IBIS_2EQ2UK)
    generic map ( DataFile => ".\Macro_lib\No_ODT_IO_data.txt" )
    port map ( PU_ref   => Power,
               PD_ref   => Ground,
               Pad      => Output,
               In_D     => Input,
               PC_ref   => Power,
               GC_ref   => Ground );
```

SPICE Simulator

```
b_io PUrefB PDrefB IoB InB En PCrefB GCrefB
+ file='mybuf.ibs' model='mybuf' +power=on buffer=2
```

Status at Last Meeting

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- Preliminary library in place
- Recruiting semiconductor vendors to test library
- Looking for additional model templates
  - Initial set contributed by Cadence
- Looking for resources to help with automated model translation / reformatting

Recent Activities

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- Ongoing weekly meetings
- Final coding / testing of element library
- Driving EDA tool compatibility
- BIRD100.2 accepted
- Recruited Paul Fernando (NCSU) to help with model translation issues
- Released library versions 1.0 (Verilog-A and VHDL-AMS)
  - www.eda.org/pub/ibis/macromodel_wip/

Tool Development

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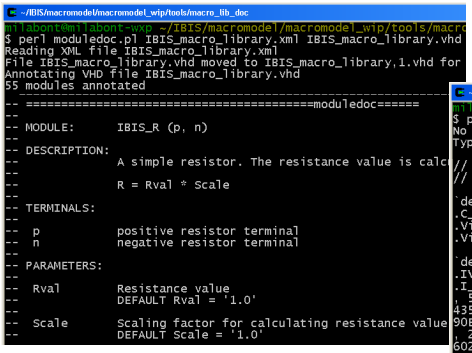
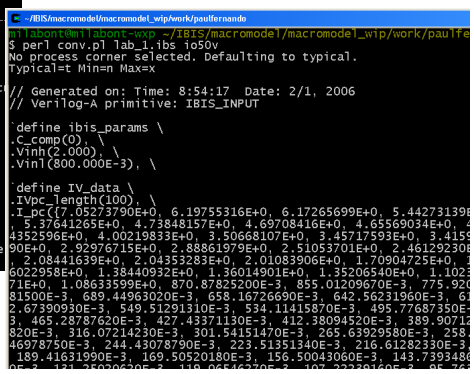
Documentation Tool



Model Data Extraction Tool



Current Issues

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- **Significant compatibility issues identified with AMS implementations in different EDA tools**
  - **Understandable, considering relative age of –AMS language and EDA implementations**
- **Discussions on best way to proceed**
  - **Discard macro modeling, rely on native AMS**
  - **Document needed AMS language subsets in Verilog and VHDL**
  - **Proceed as planned, using macro library as *de facto* subset documentation and test case**
  - **Proceed as planned, have macro library explicitly defined as compliance test suite**

Next Steps

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- Continue analog-only vs. full-AMS discussion
- Drive EDA tool improvements for language support
- Seek additional semiconductor and EDA vendor participation
- Create additional templates, determine if additional building blocks are needed

For More Information

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- IBIS-Macro Website
  - www.eda.org/pub/ibis/macromodel_wip/
- IBIS-Macro mail reflector
  - Mail to: ibis-macro-request@freelists.org
  - Subject: subscribe
- IBIS-Macro mail archives
  - www.freelists.org/archives/ibis-macro