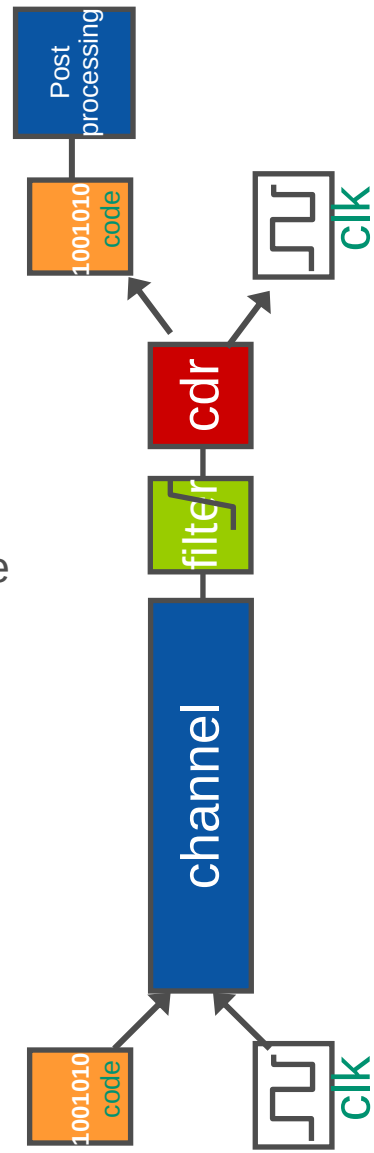
AMI Proposal Background
Cadence

C. Kumar, Architect, Cadence Design Systems, Inc.

Oct 10, 2006

Advanced Serdes Modeling Challenges

- For 5+Gbps Serdes devices, complex signal processing ***algorithms*** often need to be represented, like:
  - FFE/DFE tap coefficient optimization (with/without crosstalk)
  - CDR algorithms
  - proprietary noise cancellation techniques
  - proprietary post-processing of data
- Architectural level exploration required
  - Algorithms are easy to represent and already exist at design level
  - They are typically modeled in higher level programming languages like C or Matlab
- These algorithms are very difficult to represent with traditional device modeling techniques
  - Long run times even if you can create them
- There is currently no industry-standard way to represent algorithms
  - IP suppliers have developed & distributed their own proprietary tools, increasing their support costs
  - No interoperability for systems company users

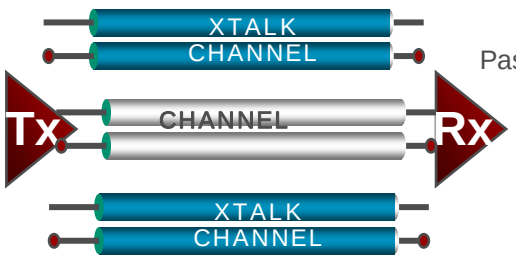


Simple API

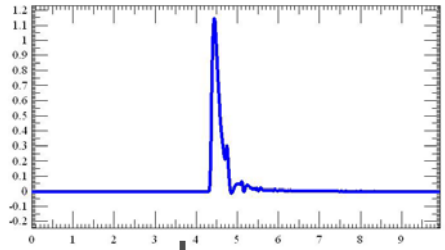
- Init
  - Initialize and optimize channel with Tx / Rx Model
  - This is where the IC DSP decides how to drive the system: e.g., filter coefficients, channel compensation, …
  - Input: Channel Characterization, system and dll specific parameters from config file
    - bit period, sampling intervals, # of forward/backward coefficients, …
  - Output: Modified Channel Characterization, status
- GetWave
  - Modify continuous time domain waveform [CDR, Post Processing]
  - Input: Voltage at Rx input at specific times
  - Output: Modified Voltage, Clock tics, status
- Close
  - Clean up, exit

Parameters passed by the system simulation platform are in red

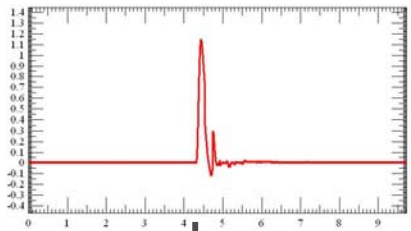
Rx_init



Pass characterization in matrix ‘a’



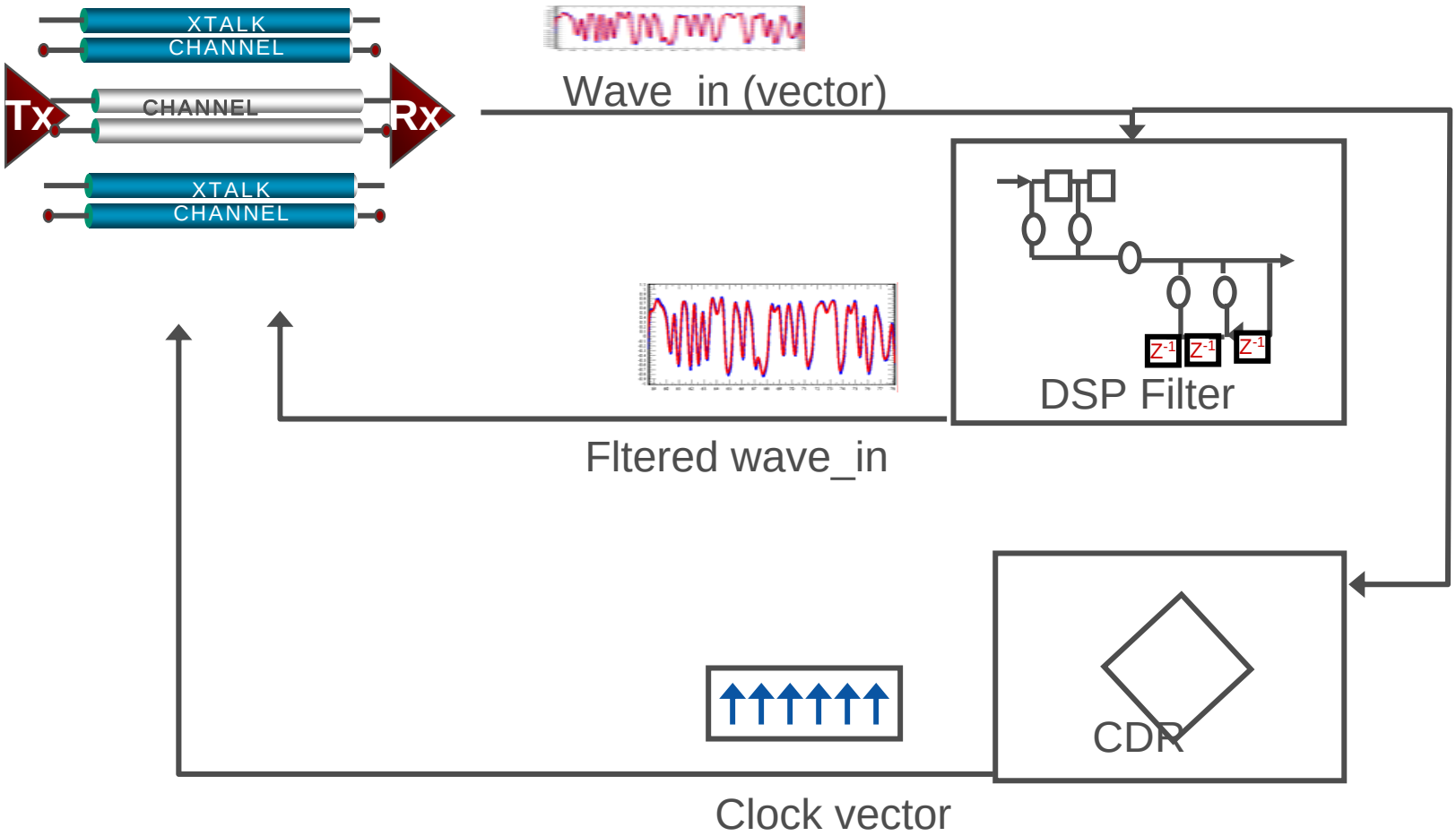
Dsp algorithms , modify characterization



Send modified char back (modify matrix ‘a’)

Internal storage

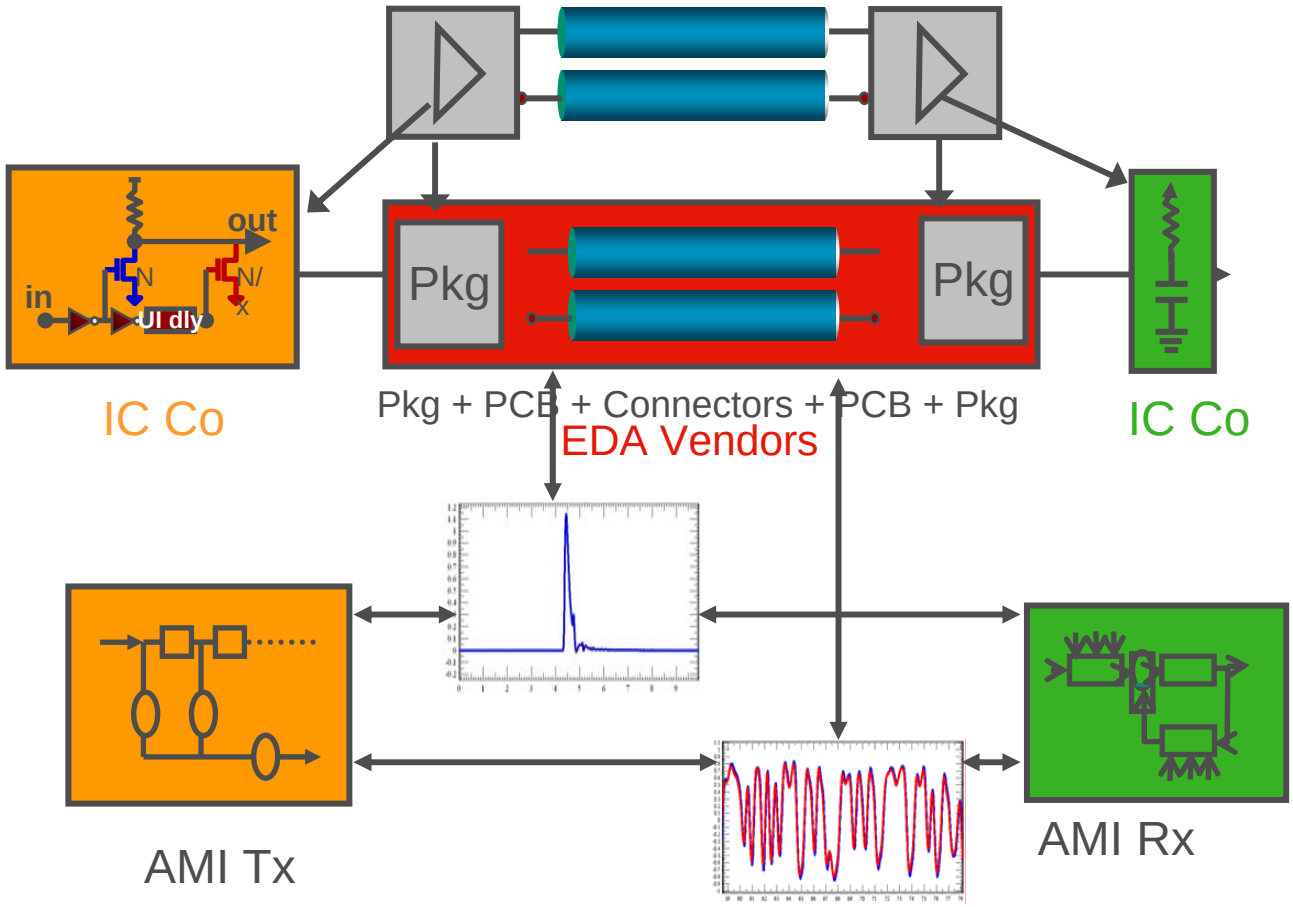
Rx_getwave


XTALK
CHANNEL
CHANNEL
XTALK
CHANNEL
Tx
Rx
Wave_in (vector)
DSP Filter
Z-1
Z-1
Z-1
Fltered wave_in
CDR
Clock vector

Proposal is evolutionary

- Leverages existing infrastructure
- Tx front end + channel + rx front end impulse characterization can be done using existing infrastructure

Evolutionary platform



Multiple Scenerios

- Only Rx model is algorithm base
- Both Tx and Rx are algorithm base