Electrical Module Description
EMD
Review

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Module Interconnect Modeling Requirements

- Signal Interconnect Modeling
- Signal Coupling (crosstalk)
- Power Distribution
  - Rail voltage AC coupling
  - DC drop
    - Bed Spring Model
    - Voids, cutouts, islands in planes
- Coupling between Signal Interconnects and Power Distribution (SSO)

EMD Solution

- Contains the following sections
  - [mPins]
    - Pins on the “periphery” of the module
  - [Components]
    - IBIS Component
    - EMD
  - [Extended Nets]
    - Connects between mPins and Components Pins
  - [Interconnect Subckts]
    - Ports are mPins and/or Pins

Subckts

- “Interconnect Nodal Netlist Format”
- It is expected that translators will be required for each target simulator
- Model only interconnect
- Assume LTI
- Parameters

Subckt “Views”

- A package has both a 1 GHz parallel interface and a 7GHz SerDes interface.
- Require RLGC models for the parallel interface.
- Require S Parameter models for the SerDes interface.

Decisions

- EMD Components
  - SDRAM sdram.ibs sdram U1 U2
- EMD Netlist
  - Net ADDR7 J1.7 U1.B24 U2.B24
- Subckt Blocks
  - Tline, RLGC, S-Parameter, Brad Element, …
- Subckt Netlist Between Blocks
  - Block J1.7 Tee RLGCTable=W50ohm.rlgc Len=.04
  - Block Tee U1.B24 TouchstoneFile=50ohm.s2p
  - Block Tee U2.B24 Model=Tline Zo=50 Td=200ps

Subckt Elements

- Resistor
- Inductor
- Capacitor
- Conductance
- Coupling Element
- Tline
- RLGC
- S-Parameter
- Impulse Response
- Controlled Sources
- Poles and Zeros
- Subckt of Above

- Miscellaneous
  - .Parameter
- Corner
  - Slow/Typ/Fast
  - Min/Max Noise
  - Min/Max CrossTalk