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BIRD ID#: ???
ISSUE TITLE: Analog Model Boundary Definition
REQUESTER: Arpad Muranyi, Mentor Graphics
DATE SUBMITTED: ???
DATE REVISED: ???
DATE ACCEPTED BY IBIS OPEN FORUM:

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STATEMENT OF THE ISSUE:

The IBIS specification does not explicitly describe the boundary conditions of analog models contained in [External Model]s or [External Circuit]s which can lead to serious modeling problems if the assumptions of the model maker and the EDA tool vendor are different.

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STATEMENT OF THE RESOLVED SPECIFICATIONS:

On pg. 104 of the IBIS v5.0 specification, below this paragraph:

| SPICE, VHDL-A(MS), Verilog-A(MS) cannot process digital signals. All SPICE, VHDL-A(MS), Verilog-A(MS) input and output signals must be in analog format. Consequently, IBIS multi-lingual models using SPICE, VHDL-A(MS) or Verilog-A(MS) require analog-to-digital (A_to_D) and/or digital-to-analog (D_to_A) converters to be provided by the EDA tool. The converter subparameters are declared by the user, as part of the [External Model] or [External Circuit] syntax, with user-defined names for the ports which connect the converters to the analog ports of the SPICE, VHDL-A(MS), or Verilog-A(MS) model. The details behind these declarations are explained in the keyword definitions below.

add these words:

| The electrical output characteristics of D_to_A converters are equivalent to ideal voltage sources having a zero Ohm drive impedance, and the electrical input characteristics of A_to_D converters are equivalent to ideal voltage probes, having an infinite input impedance.
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ANALYSIS PATH/DATA THAT LED TO SPECIFICATION

A long series of email and teleconference discussions in the IBIS Advanced Technology Modeling Task Group resulted in a decision that defining the D_to_A and A_to_D converters as ideal voltage sources and ideal voltage probes should be sufficient to avoid any ambiguities in the IBIS

specification regarding analog models instantiated in [External Model]s
and [External Circuit]s, including proper boundary condition definitions
for S-parameter models and Touchstone files.

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ANY OTHER BACKGROUND INFORMATION:

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