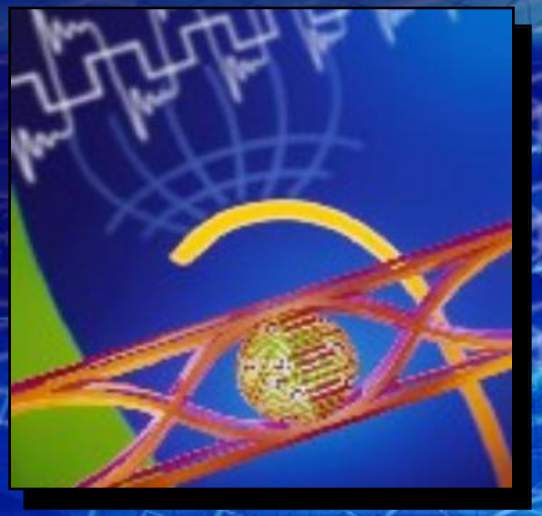
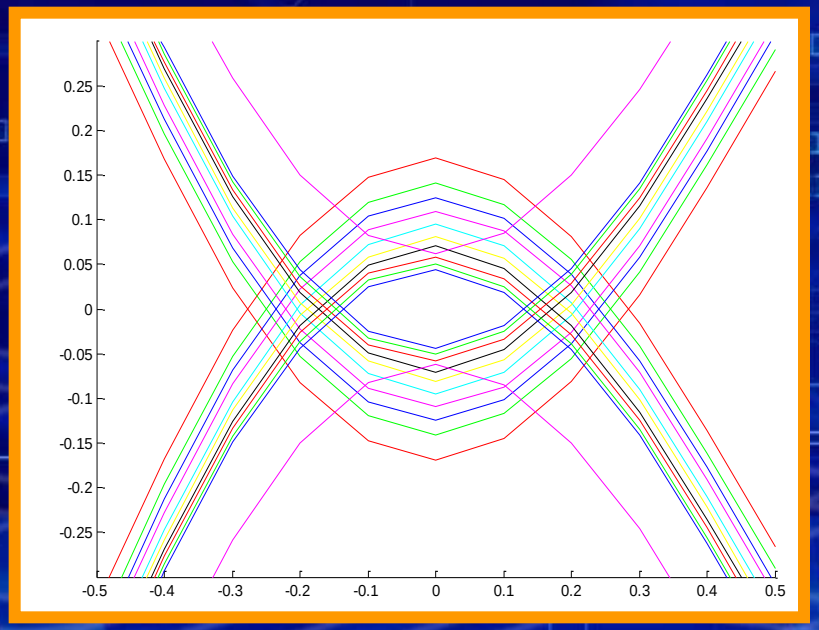
IBIS-AMI Analog Modeling



IBIS ATM Discussions
June 2012



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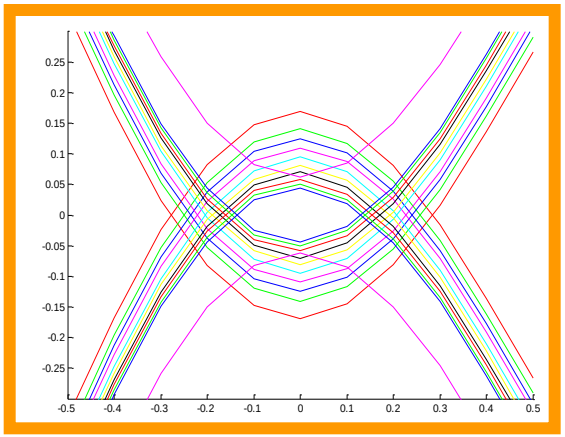
IBIS-AMI Analog Modeling



IBIS ATM Discussions
June 2012

1. IBIS-AMI analog model examples with IBIS-ISS
2. Package modeling in legacy IBIS
3. Package modeling with BIRD 125 and IBIS-ISS
4. More details for the Figure 12 example
5. A fundamental problem in legacy IBIS
6. A solution using existing BIRDs

The current state of buffer modeling using BIRDs 116-118

S-parameter Tx model with [External Model] & IBIS-ISS

Legacy IBIS file:

```
|------------------------------------------------------------
| Example of an analog AMI Tx model using [External Model] and
| an IBIS-ISS S-parameter:
|------------------------------------------------------------
[Model] ISS_Diff_Tx
Model_type Output_diff
Rref_diff = 100
|
[Voltage Range] 1.0   NA   NA
|
[Ramp]
dV/dt_r   0.6/40p   NA   NA
dV/dt_f   0.6/40p   NA   NA
|
[External Model]
Language ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner     Typ          AMIdriver.cir    AMI_Sdrv
|
| List of parameters
Parameters  TSFile = Tx.par(Tstonefile)
|
| List of converter parameters
Converter_Parameters  VloP =  Tx.par(Vol)
Converter_Parameters  VhiP =  Tx.par(Voh)
Converter_Parameters  VloN =  Tx.par(Voh)
Converter_Parameters  VhiN =  Tx.par(Vol)
Converter_Parameters  Tfa  =  Tx.par(Trf)
Converter_Parameters  Tri  =  Tx.par(Trf)
|
| Ports List of port names (in same order as in SPICE)
Ports  A_signal_pos  A_signal_neg  my_driveP  my_driveN  A_gnd
|
| D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name
D_to_A  D_drive  my_driveP  my_ref  VloP  VhiP  Tfa  Tri  Typ
D_to_A  D_drive  my_driveN  my_ref  VloN  VhiN  Tfa  Tri  Typ
|
[End External Model]
|
[Algorithmic Model]
Executable  Windows_VisualStudio_32  MentorTx.dll  MentorTx.ami
[End Algorithmic Model]
```

Tx.par file:

```
(Tstonefile (Usage Info)(Type String)
   (Corner "NC.s4p" "WC.s4p" "BC.s4p")
   (Description "Driver on-die S-parameter file")
)
(Voh (Usage Info)(Value 0.9)(Type Float)
   (Description "Output open circuit high voltage")
)
(Vol (Usage Info)(Value 0.0)(Type Float)
   (Description "Output open circuit low voltage")
)
(Trf (Usage Info)(Value 40e-12)(Type Float)
   (Description "20%-80% output rise time")
)
```

EDA tool GUI lets user select "one of many". Dependency Table may also affect what this GUI does.

AMIdriver.cir file:

```
*******************************************************************************
.SUBCKT  AMI_Sdrv  A_signal_pos  A_signal_neg  my_driveP  my_driveN  my_ref
+ TSFile="TouchstoneFileName.s4p"

Sdriver  my_driveP  A_signal_pos  my_driveN  A_signal_neg  my_ref
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]

*******************************************************************************
.ends
```

RC Rx model with [External Model] & IBIS-ISS

Legacy IBIS file:

```
|------------------------------------------------------------
| Example of an analog AMI Rx model using [External Model] and
| an IBIS-ISS circuit:
|------------------------------------------------------------
[Model] ISS_Diff_Rx
Model_type Input_diff
|
[Voltage Range] 1.0   NA   NA
|
[External Model]
Language ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner     Typ          AMIreceiver.cir    AMI_RCrcv
|
| List of parameters
Parameters   Rt_H  Rt_L    = Rx.par(Rt)
Parameters   Rd            = Rx.par(Rd)
Parameters   Cc_H  Cc_L    = Rx.par(Cc)
Parameters   Cd  Vt
|
| List of converter parameters
Converter_Parameters  Vlo = -0.05
Converter_Parameters  Vhi =  0.05
|
| Ports List of port names (in same order as in SPICE)
Ports  A_signal_pos  A_signal_neg  my_rcv_H  my_rcv_L  A_gnd
|
| D_to_A d_port port1 port2 vlow vhigh corner_name
A_to_D  D_receive  my_rcv_H      my_rcv_L      Vlo  Vhi  Typ
|A_to_D  D_receive  A_signal_pos  A_signal_neg  Vlo  Vhi  Typ
|
[End External Model]
|
[Algorithmic Model]
Executable  Windows_VisualStudio_32  MentorTx.dll  MentorRx.ami
[End Algorithmic Model]
|
```

Rx.par file:

```
(Rt  (Usage Info)(Value 47.75)(Type Float)
   (Description "Single-ended termination resistance")
)
(Rd  (Usage Info)(Value 99.75)(Type Float)
   (Description "Differential termination resistance")
)
(Cc  (Usage Info)(Value 0.5e-12)(Type Float)(Default 0.5e-12)
   (Description "Input Capacitance")
)
```

AMIreceiver.cir file:

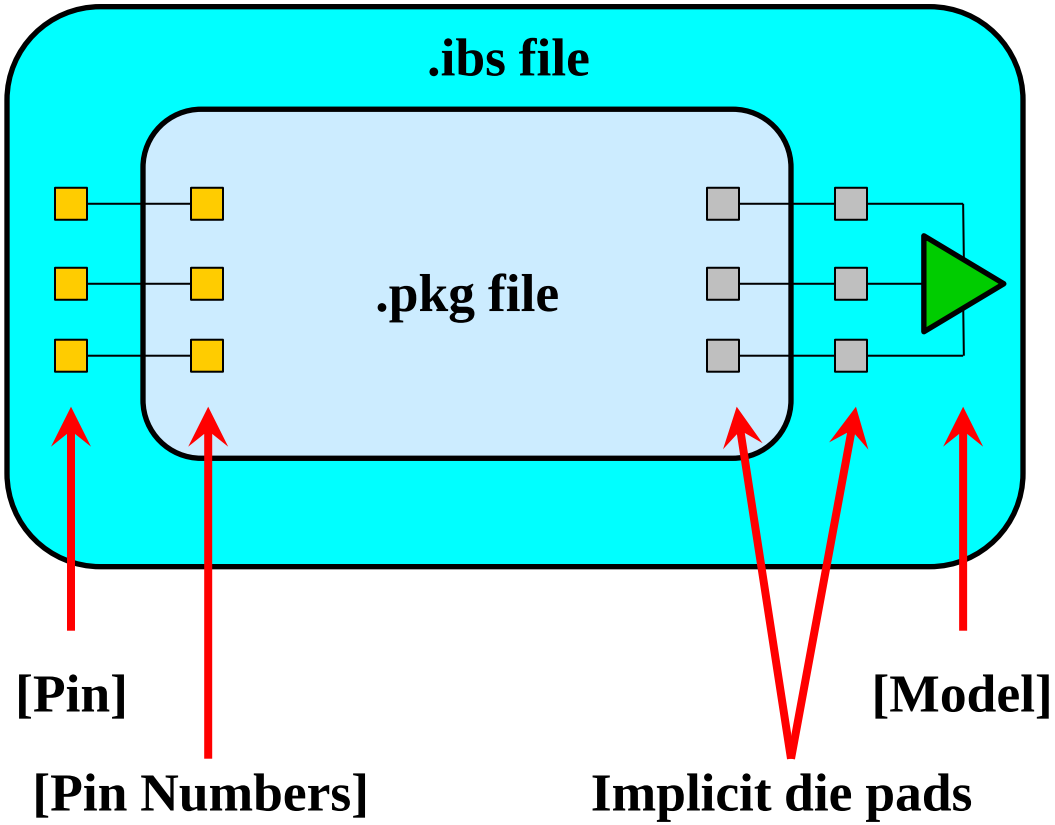
```
*******************************************************************************
.SUBCKT  AMI_RCrcv  A_signal_pos  A_signal_neg  my_rcv_H  my_rcv_L  my_ref
+ Rt_H   = 1e+6
+ Rt_L   = 1e+6
+ Rd     = 1e+6
+ Cc_H   = 0
+ Cc_L   = 0
+ Cd     = 0
+ Vt     = 0

Cc_H  A_signal_pos  my_ref         C=Cc_H
Cc_L  A_signal_neg  my_ref         C=Cc_L
Cd    A_signal_pos  A_signal_neg   C=Cd
Rt_H  A_signal_pos  my_vtt         R=Rt_H
Rt_L  A_signal_neg  my_vtt         R=Rt_L
Rd    A_signal_pos  A_signal_neg   R=Rd

Vvtt    my_vtt    my_ref  DC=Vt
E_H     my_rcv_H  my_ref  VCVS  A_signal_pos  my_ref  1
E_L     my_rcv_L  my_ref  VCVS  A_signal_neg  my_ref  1
*******************************************************************************
.ends
```

Legacy IBIS package modeling overview

Package modeling in legacy IBIS



Package modeling in legacy IBIS

```
[Pin] signal_name  model_name
 A1   Vcc1         POWER
 B2   DQ_signal    DQ_model
 C3   GND1         GND
|
[Package Model]  A_pkg_model
|…
[Model] DQ_model
Model_type I/O
|…
```

```
[Define Package Model]  A_pkg_model
[Manufacturer]          Noname Company, Inc.
[OEM]                   Noname Company, Inc.
[Description]           Illustration model
[Number Of Pins]  3
|
[Pin Numbers]
 A1
 B2
 C3
|…
[Model Data]
|…
```

- The .ibs file does not declare the pads on the die
- It assumes ***one*** corresponding "implicit" pad for each pin
- The [Pin] list is repeated in the package model as [Pin Numbers]
- The package model is placed between the pin and this implicit pad

The current state of package modeling using BIRD 125

Package modeling with BIRD 125

```
[Pin] signal_name  model_name
 A1   Vcc1         POWER
 B2   DQ_signal    DQ_model
 C3   GND1         GND
|
[Package Model]  A_pkg_model
|…
[Model] DQ_model
Model_type I/O
|…
[Node Declarations]
Pad_2
```

```
[Define Package Model]  A_pkg_model
[Manufacturer]          Noname Company, Inc.
[OEM]                   Noname Company, Inc.
[Description]           Illustration model
[Number Of Pins]  3
|
[Pin Numbers]
 A1  DiePortName = IDP_A1
 B2  DiePortName = Pad_2
 C3  DiePortName = IDP_C3
|…
[Package Circuit]
Language IBIS-ISS
|…
```

- The new 2nd column of [Pin Numbers] declares
  - Implicit on-die nodes (pads)
  - Explicit on-die nodes (pads)
- IBIS-ISS models can be placed between pins and pads
- This supports arbitrary mapping between pins and pads

A simple package model with IBIS-ISS

Legacy IBIS file:

```
|------------------------------------------------------------
| Example of an IBIS model using an IBIS-ISS package model
|------------------------------------------------------------
|
[Pin] signal_name  model_name
  1   …            …
  2   …            …
  3   …            …
  4   …            …
  5   Channel_1P   ISS_Diff_Tx
  6   Channel_1N   ISS_Diff_Tx
  7   Channel_2P   ISS_Diff_Tx
  8   Channel_2N   ISS_Diff_Tx
  9   …            …
 10   …            …
|
[Package Model]  A_4_pin_pkg_model
|…
|…
```

Matched by name

PackageModel.cir file:

```
**************************************************************
.SUBCKT  S_pkg  P1  P2  P3  P4  P5  P6  P7  P8
+ TSFile="TouchstoneFileName.s8p"

Sdriver  P1  P2  P3  P4  P5  P6  P7  P8
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]

**************************************************************
.ends
```

Matched by position

IBIS .pkg file:

```
|------------------------------------------------------------
| This example implements a package model using an IBIS-ISS
| subcircuit.
|------------------------------------------------------------
|
[Define Package Model]  A_4_pin_pkg_model
[Manufacturer]          Noname Company, Inc.
[OEM]                   Another Noname Package Company, Inc.
[Description]           4-pin
[Number Of Pins]  4
|
[Pin Numbers]
  5   DiePortName = IDP_5
  6   DiePortName = IDP_6
  7   DiePortName = IDP_7
  8   DiePortName = IDP_8
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  PackageModel.cir  S_pkg
|
| Parameters List of parameters
Parameters  TSFile = "My_TstoneFile.s8p"
|
| Ports are in same order as defined in SPICE
Ports  5      6      7      8
Ports  IDP_8  IDP_7  IDP_6  IDP_5
|
[End Package Circuit]
[End Package Model]
```

Declaration of Implicit die ports

Matched by name

Figure 12 (pg. 136) in IBIS v5.0

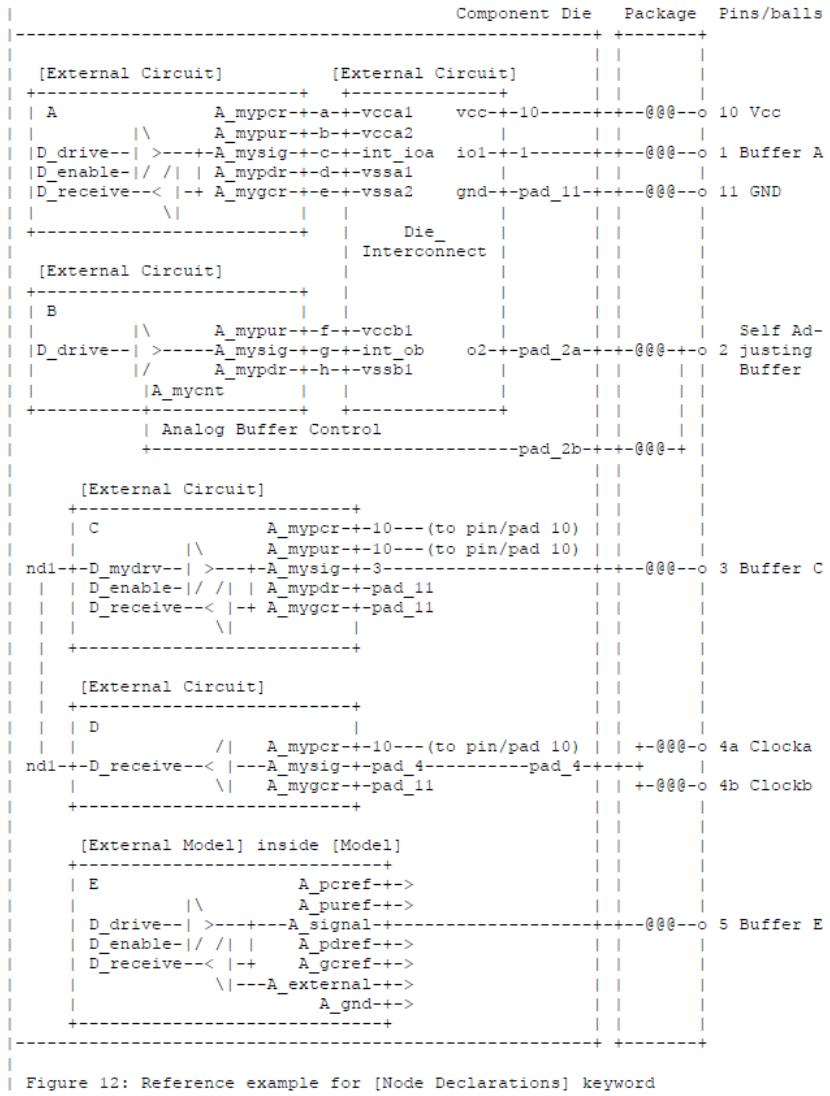


Figure 12 implemented with IBIS-ISS

Legacy IBIS file:

```
|-------------------------------------------------------------
| Example of an IBIS model using an IBIS-ISS package model.
| This example implements a package call for the drawing in
| Fig. 12 on pg. 136 of the IBIS v5.0 specification.
|-------------------------------------------------------------
|
[Pin] signal_name  model_name
 10   Vcc          POWER
  1   A0           CIRCUITCALL
 11   GND          GND
  2   CAS0         CIRCUITCALL
  3   A1           CIRCUITCALL
  4a  Clk_A        CIRCUITCALL
  4b  Clk_B        CIRCUITCALL
  5   A2           Buffer_E
|
[Node Declarations]
| Die nodes:
a  b  c  d  e  f  g  h  nd1    | List of die nodes
|
| Die pads:
pad_2a  pad_2b  pad_4  pad_11  | List of die pads
|
[End Node Declarations]
|
[Package Model]  QS-SMT-cer-8-pin-pkgs
|…
```

PackageModel.cir file:

```
**********************************************************
.SUBCKT  S_pkg  P1  P2   P3   P4   P5   P6   P7   P8
+               P9  P10  P11  P12  P13  P14  P15  P16
+ TSFile="TouchstoneFileName.s16p"

Sdriver  P1  P2   P3   P4   P5   P6   P7   P8
+        P9  P10  P11  P12  P13  P14  P15  P16
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]

**********************************************************
.ends
```

IBIS .pkg file:

```
|-------------------------------------------------------------
| This example implements a package model using an IBIS-ISS
| subcircuit for the drawing in Fig. 12 on pg. 136 of the
| IBIS v5.0 specification.
|-------------------------------------------------------------
|
[Define Package Model]  QS-SMT-cer-8-pin-pkgs
[Manufacturer]          Quality Semiconductors Ltd.
[OEM]                   Acme Package Co.
[Description]           8-Pin ceramic SMT package
[Number Of Pins]  8
|
[Pin Numbers]
 10   DiePort = IDP_10
  1   DiePort = IDP_1
 11   DiePort = pad_11
  2   DiePort = pad_2a
  2   DiePort = pad_2b
  3   DiePort = IDP_3
  4a  DiePort = pad_4
  4b  DiePort = pad_4
  5   DiePort = IDP_5
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  PackageModel.cir  S_pkg
|
| Parameters List of parameters
Parameters  TSFile = "My_TstoneFile.s16p"
|
| Ports are in same order as defined in SPICE
Ports  10  1  11  2  3  4a  4b  5
Ports  IDP_5  pad_4  IDP_3  pad_2b
Ports  pad_2a  pad_11  IDP_1  IDP_10
|
[End Package Circuit]
[End Package Model]
```

Matched by name

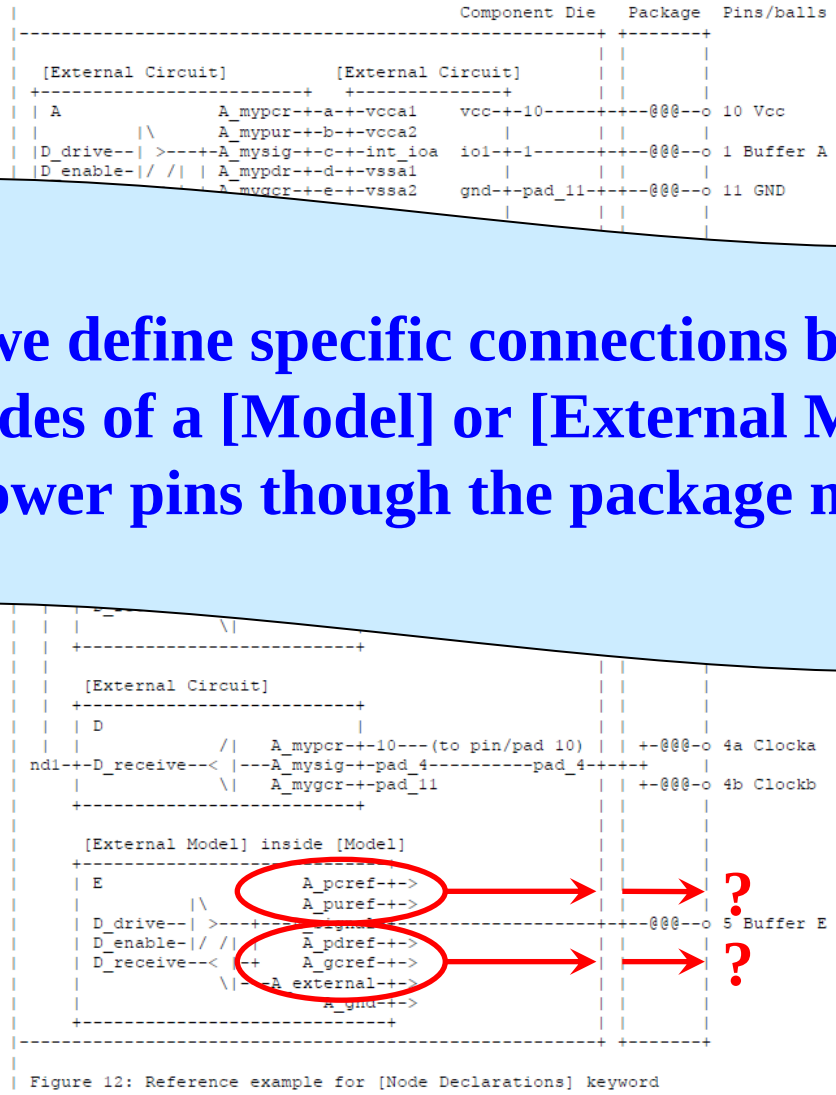
Implicit die ports (in blue)

Explicit die ports (in red) are declared under [Node Declarations]

Matched by position

Matched by name

A missing detail in the previous example for Figure 12



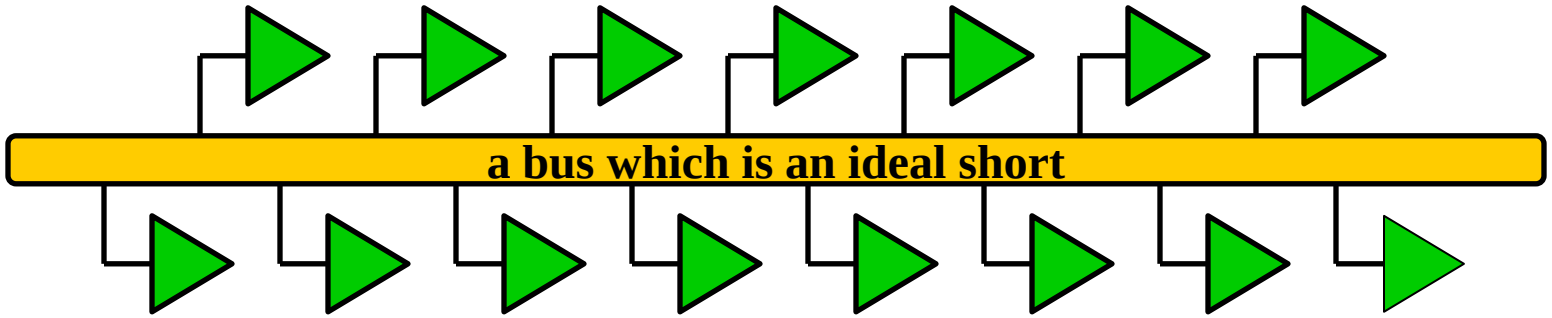
How can we define specific connections between the supply nodes of a [Model] or [External Model] and the power pins though the package model?

Use [Pin Mapping] to declare supply die pads

```
[Pin]  signal_name  model_name  R_pin  L_pin  C_pin
|
Vcc1   Supply1      POWER
Vcc2   Supply2      POWER
Vcc11  Supply11     POWER
Vcc12  Supply12     POWER
GND1   Ground1      GND
GND11  Ground11     GND
Ref1   Reference1   POWER
Ref11  Reference11  POWER
|
5      Data5        EM5
15     Data15       EM15
|
|
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
|
Vcc1          NC           PCref_EM5
Vcc2          NC           PUref_EM5
Vcc11         NC           PCref_EM15
Vcc12         NC           PUref_EM15
GND1          Ground_EM5   NC
GND11         Ground_EM15  NC
Ref1          NC           EXref_EM5
Ref11         NC           EXref_EM15
|
5             Ground_EM5   PUref_EM5  Ground_EM5    PCref_EM5       EXref_EM5
15            Ground_EM15  PUref_EM15 Ground_EM15   PCref_EM15      EXref_EM15
```

These are called “bus names” by the specification, and are defined to be ideal shorts. Functionally they are the same thing as “die nodes” or “die pads”.

If a bus is an ideal short, it is a node



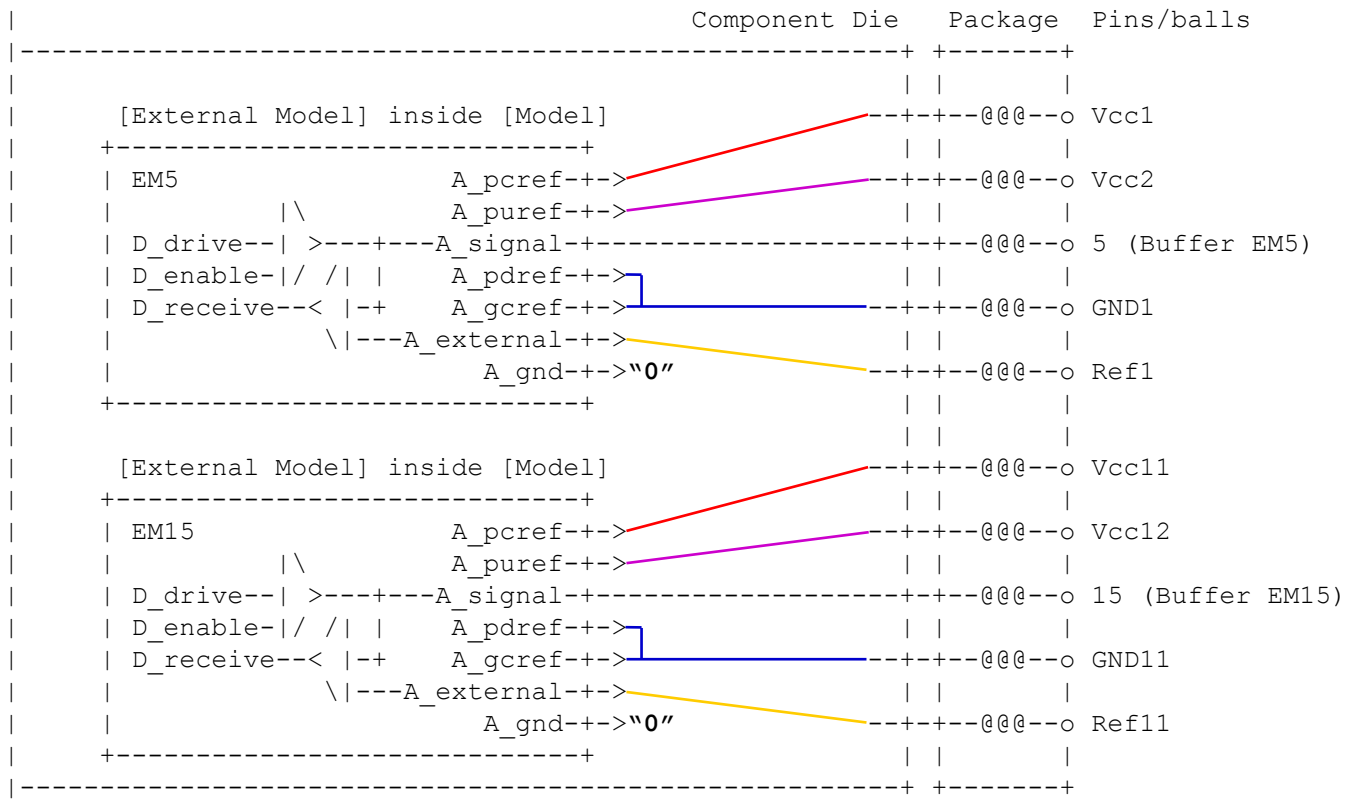
If the "bus" is an ideal short, each receiver sees exactly the same signal, i.e. the bus is just a node

The number of connections made to the "bus" doesn't make a difference, if it is ideal, it is till just a "node"…

[Pin Mapping] = [Node Declarations] + Netlisting

- **The [Pin Mapping] keyword serves three functions**
  - **declares die nodes (ideal short die buses)**
  - **associates (i.e. connects) die nodes with the reserved analog supply node names of [Model] or [External Model]**
    - `A_pdref, A_pdref, A_gcref, A_pcref, A_extref`
    - signal nodes are NOT included
  - **associates the named die nodes (pads) with pin names**
    - eliminates the need for implicit die pad names (derived from pin names)
- **This provides a mechanism to connect the supply nodes of [Model] and [External Model] to specific pins through an accurate package model (IBIS-ISS)**
  - **multiple pin to single pad *is* possible**
  - **multiple pad from different [Model]s to single pin *not* possible**
- **This works with IBIS 5.0 and BIRD 125.1**
  - **slight modifications to [Pin Mapping] could provide on die interconnect modeling capabilities also**

Modified Figure 12 to illustrate supply connections



Modified Figure 12 using BIRD 125.1 syntax

Legacy IBIS file:

```
|-------------------------------------------------------------
| Example of an IBIS model using an IBIS-ISS package model.
|-------------------------------------------------------------
|
Vcc1    Supply1       POWER
Vcc2    Supply2       POWER
Vcc11   Supply11      POWER
Vcc12   Supply12      POWER
GND1    Ground1       GND
GND11   Ground11      GND
Ref1    Reference1    POWER
Ref11   Reference11   POWER
|
5       Data5         EM5
15      Data15        EM15
|
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
|
Vcc1            NC            PCref_EM5
Vcc2            NC            PUref_EM5
Vcc11           NC            PCref_EM15
Vcc12           NC            PUref_EM15
GND1            Ground_EM5    NC
GND11           Ground_EM15   NC
Ref1            NC            EXref_EM5
Ref11           NC            EXref_EM15
|
5               Ground_EM5    PUref_EM5   Ground_EM5    PCref_EM5       EXref_EM5
15              Ground_EM15   PUref_EM15  Ground_EM15   PCref_EM15      EXref_EM15
|
[Package Model]  QS-SMT-cer-10-pin-pkgs
|…
```

IBIS .pkg file:

```
|-------------------------------------------------------------
| This example implements a package model using an IBIS-ISS
| subcircuit.
|-------------------------------------------------------------
|
[Define Package Model]  QS-SMT-cer-10-pin-pkgs
[Manufacturer]          Quality Semiconductors Ltd.
[OEM]                   Acme Package Co.
[Description]           10-Pin ceramic SMT package
[Number Of Pins]  10
|
|
[Pin Numbers]
Vcc1    DiePort = PCref_EM5
Vcc2    DiePort = PUref_EM5
Vcc11   DiePort = PCref_EM15
Vcc12   DiePort = PUref_EM15
GND1    DiePort = Ground_EM5
GND11   DiePort = Ground_EM15
Ref1    DiePort = EXref_EM5
Ref11   DiePort = EXref_EM15
|
5       DiePort = IDP_5
15      DiePort = IDP_15
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  PackageModel.cir  S_pkg
|
| Parameters List of parameters
Parameters  TSFile = "My_TstoneFile.s20p"
|
| Ports are in same order as defined in SPICE
Ports  Vcc1         Vcc2         Vcc11        Vcc12
Ports  PCref_EM5    PUref_EM5    PCref_EM15   PUref_EM15
Ports  GND1         GND11        Ref1         Ref11
Ports  Ground_EM5   Ground_M15   EXref_EM5    EXref_EM15
Ports  5            15
Ports  IDP_5        IDP_15
|
[End Package Circuit]
[End Package Model]
```

PackageModel.cir file:

```
**************************************************
.SUBCKT  S_pkg  P1  P2  P3  P4  P5  P6  P7  P8  P9  P10
+               P11 P12 P13 P14 P15 P16 P17 P18 P19 P20
+ TSFile="TouchstoneFileName.s20p"
Sdriver  P1  P2  P3  P4  P5  P6  P7  P8  P9  P10
+        P11 P12 P13 P14 P15 P16 P17 P18 P19 P20
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
**************************************************
.ends
```

Matched by name

Matched by position

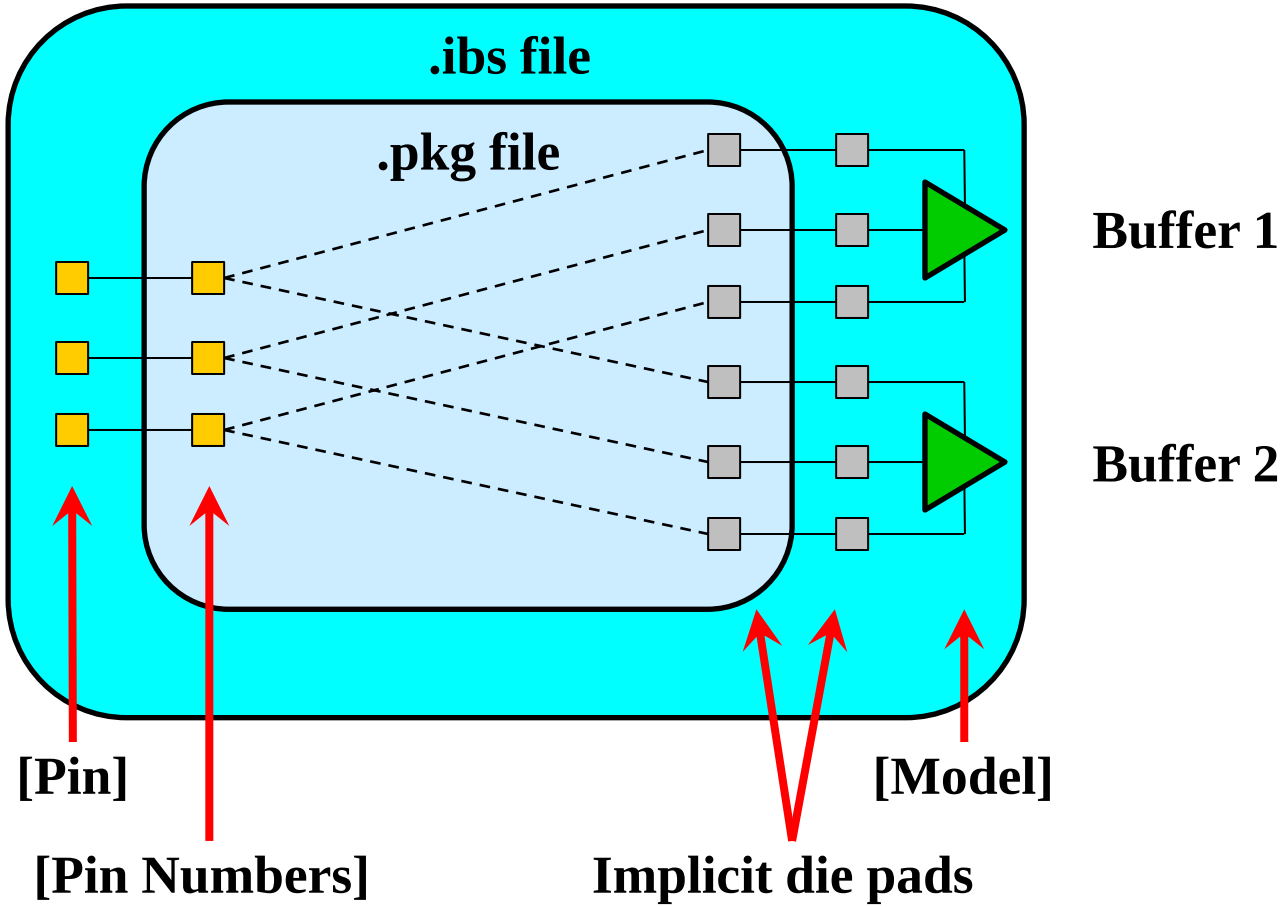
Matched by name

Explicit die ports (red) are declared under [Pin Mapping]

Implicit die ports (blue) are declared here

A fundamental problem in legacy IBIS

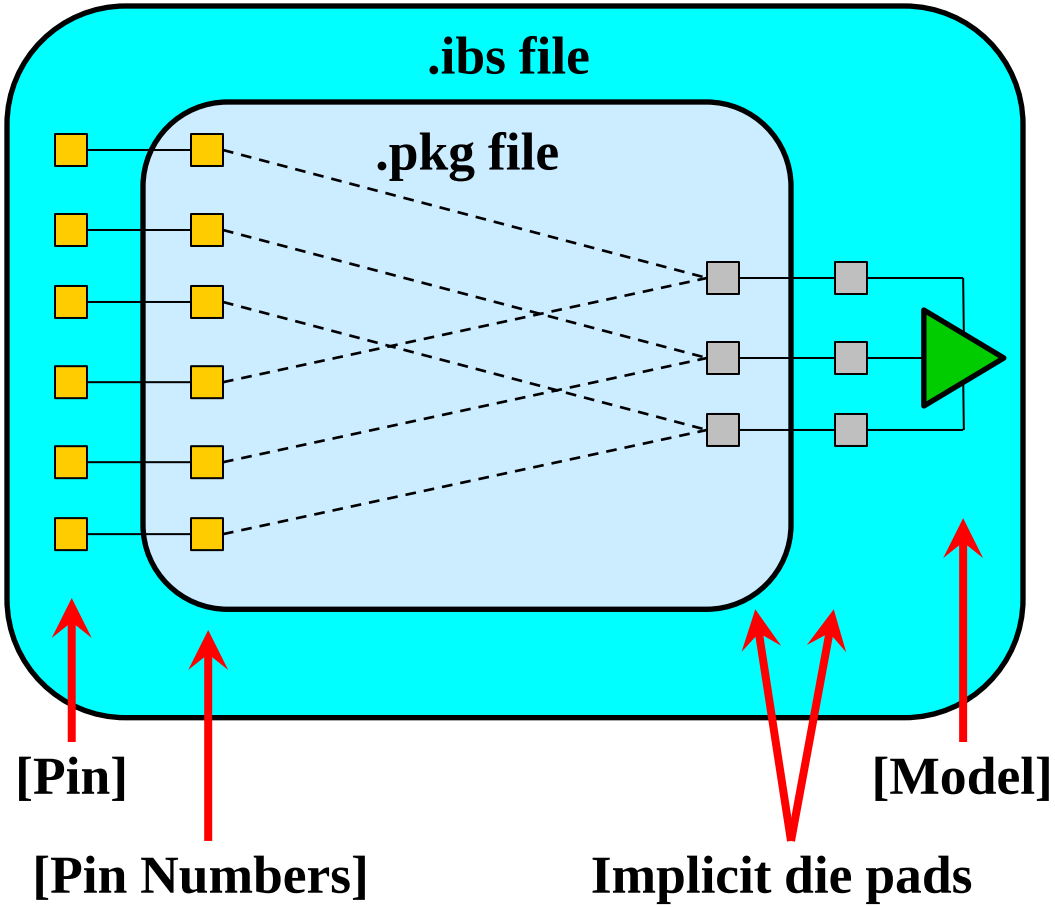
A fundamental problem in legacy IBIS



Buffers are "instantiated" by the 3rd column of the [Pin] keyword.

One pin can only instantiate one buffer in legacy IBIS.

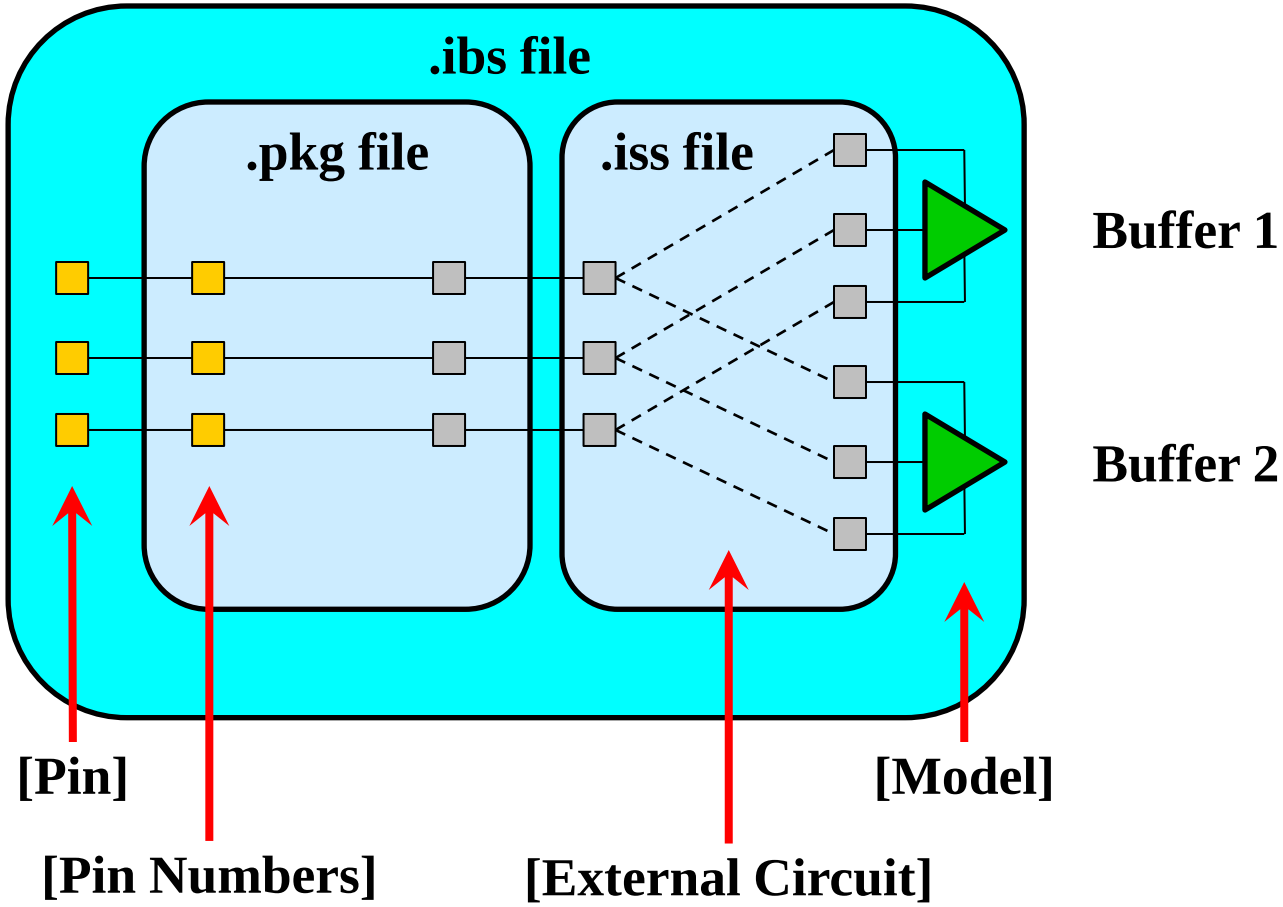
A fundamental problem in legacy IBIS



Which pin should instantiate this buffer?

An additional feature needed

We also need to be able to model on-die interconnects

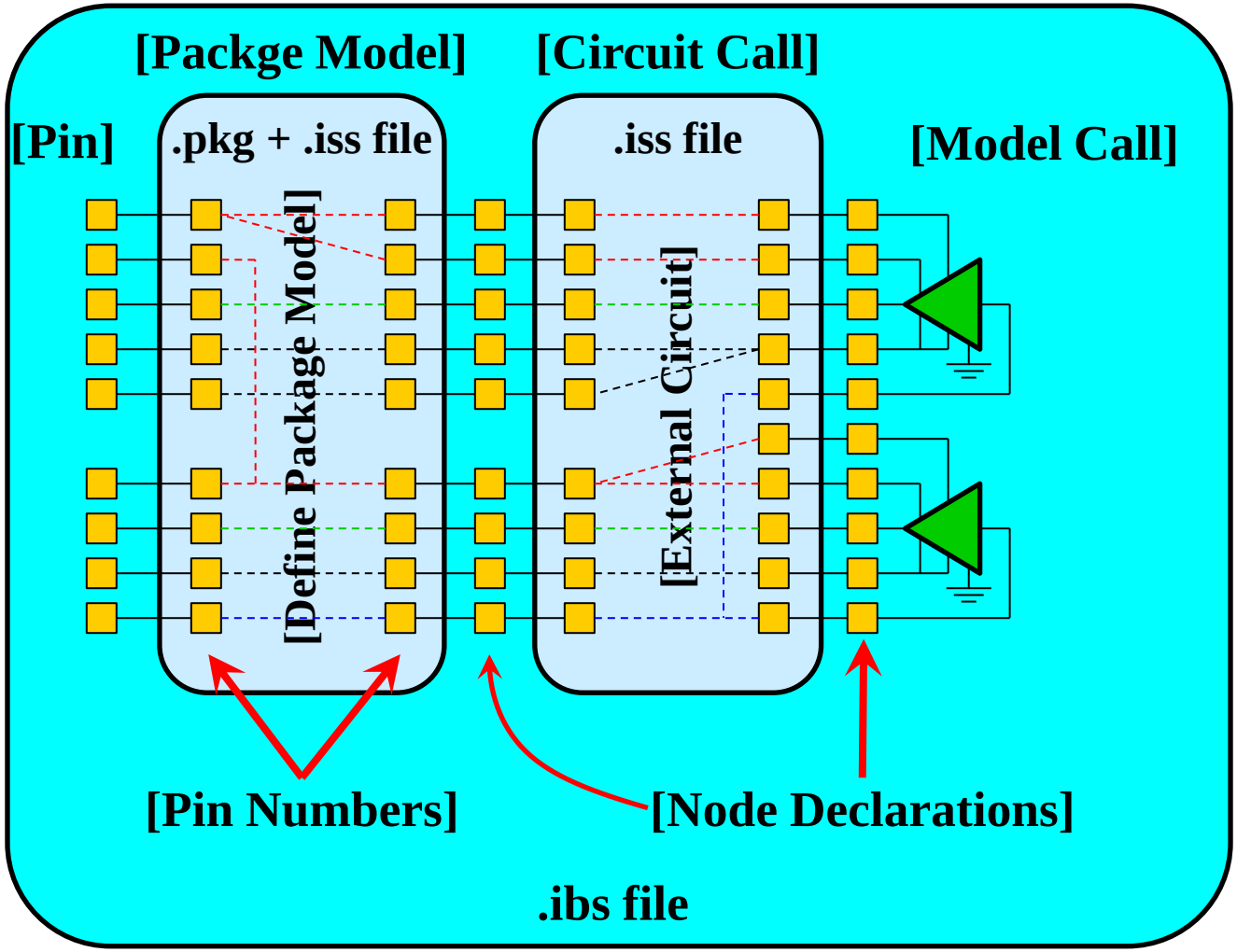


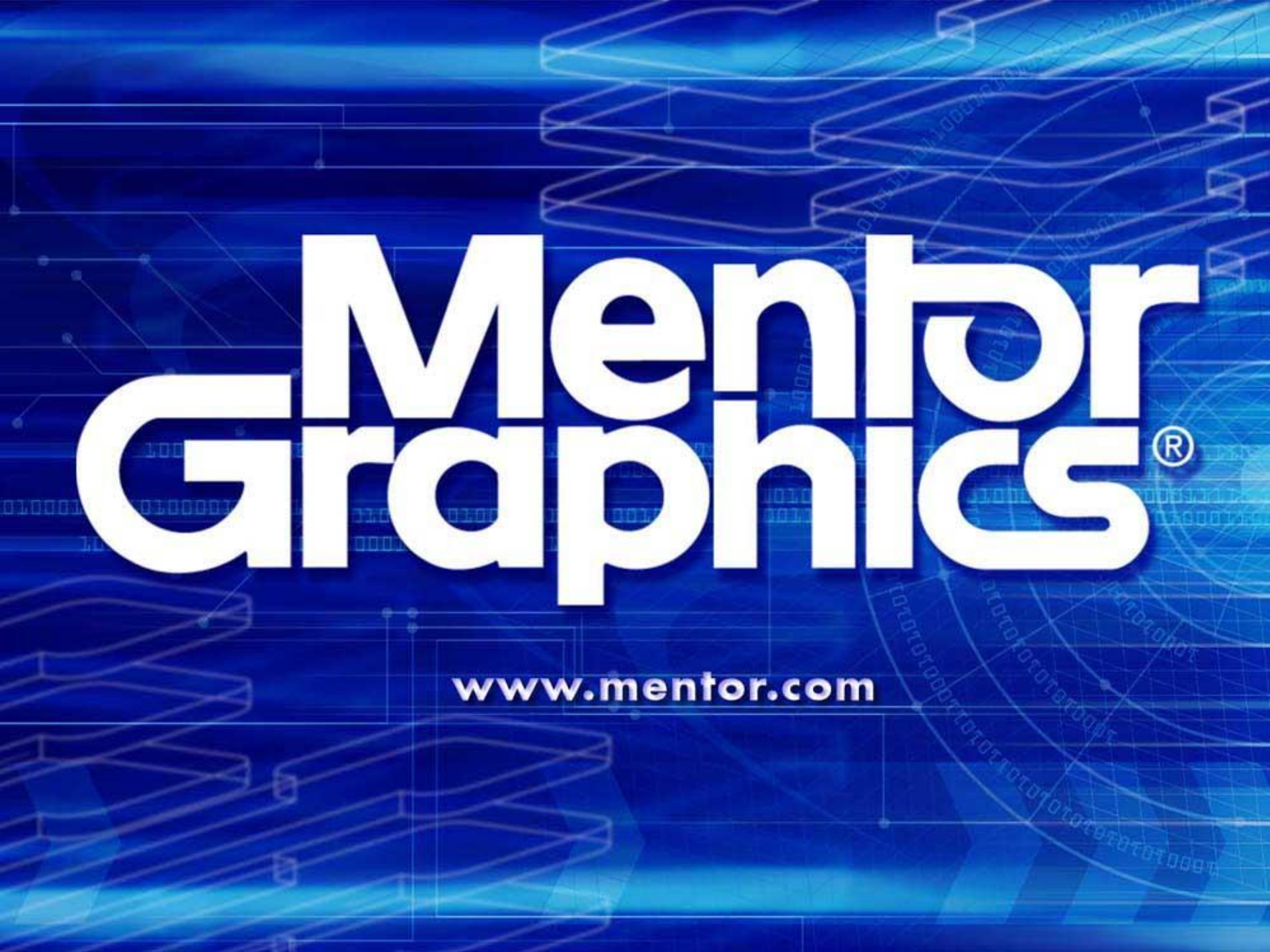
Buffers are "instantiated" by the 3rd column of the [Pin] keyword.
One pin can only instantiate one buffer in legacy IBIS.

A possible solution

- **It seems that the biggest problem is that [Model]s are instantiated from the [Pin] keyword**
  - **useful for PCB layout or IC footprint driven EDA tools to find the [Model] for a particular "net"**
  - **gets in the way of non 1 to 1 pin/ball to pad/bump mapping**
  - **gets in the way of on-die interconnect modeling**
- **The best solution seems to be to instantiate [Model]s the same way as [External Circuit]s, using [Model Call]**
  - **supports named [Model] terminals anywhere on the die**
    - **does not rely on the cumbersome [Pin Mapping] keyword to achieve this**
  - **supports named die pads/bumps**
  - **supports on-die interconnects using [External Circuit] and IBIS-ISS**
  - **supports package models with IBIS-ISS (BIRD 125)**
  - **supports arbitrary connections between buffer terminals and pads/bumps**
  - **supports arbitrary connections between pins/balls and pads/bumps**
  - **this is proposed by BIRD 145**

Illustration using BIRD 116, 125, 145

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