# IBISx

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IBIS-ATM
August 28, 2012

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# Overview

- Legacy IBIS combines package interconnect, on-die interconnect and buffer models in one file
- Idea is to put package and package interconnect into an EMD file and die, on-die interconnect and buffer models into an IBISx (.ibsx) file
- EMD (.emd files)
  - .ibs packages
  - .ebd “Board” modules
  - Multi Chip Modules (MCM)
  - Connectors
  - Cables (electrical and Optical)
- IBISx (.ibsx files)
  - Bare Die
  - Single Silicon (GaAs …) Chip

# Examples

- legacy.ibs
- package.emd
- die.ibsx
- die.ibsx with separate Buffer list

# legacy.ibs

([IBIS_Ver 5.0]
[File_Name legacy.ibs
[Component] legacy
[Pins]
|Pin_Name Signal_name Model
A1 DQ1 DQ
A2 DQ2 DQ
A3 DQ3 DQ
V1 VDD Power
G1 VSS GND
[Model] DQ
…
[End]

# package.emd

```
(package   (IBIS_Ver  6.0)   (Description "…")
      (File_Rev "…")  (Copyright "…")  (Notes "…")  (Date "…")  (Disclaimer "…")  (Manufacturer "…")
      (File_Name            package.emd)
      (Module_Name        package)
      (Number_Of_Pins     5)
      (Pins    | "Balls" of BGA package
            (A1              (Signal_Name    DQ1) (Length=11)(Class=DQ))
            (A2              (Signal_Name    DQ2) (Bank=3))
            (A3              (Signal_Name    DQ3) (Interface=DDR3))
            (V1              (Power_Name   POWER))
            (G1              (Gnd_Name      GND)) )
      (Extended_Nets
            (DQ1 A1 U1.A1) (DQ2 A2 U1.A2)  (DQ3 A3 U1.A3)
            (POWER V2 U1.VDD1 U1.VDD2) (GND G1 U1.VSS1 U1.VSS2) )
      (Reference_Designator_Map
            (U1               (IBISx_File   die.ibsx)       (Component   die)) )
      (Interconnect  | Substrate, Connector, Cable
            (Full_Package
                  (Tstonefile full_package.s12p)
                  (Model_Ports
                        (1 A1)(2 A2)(3 A3) (4 U1.A1)(5 U1.A2)(6 U1.A3)
                        (7 V1)(8 G1)(9 U1.VDD1)(10 U1.VDD2)(11 U1.VSS1 )(12 U1.VSS2)))))
```

# die.ibsx

```
(die   (IBIS_Ver  6.0)   (Description "…")
       (File_Rev "…")  (Copyright "…")  (Notes "…")  (Date "…")  (Disclaimer "…")  (Manufacturer "…")
       (File_Name            die.ibsx)
       (Chip_Name            die)
       (Number_Of_Pins     7)
       (Pads    |  "Bump Pads" of flip chip IC
              (A1              (Signal_Name    DQ1) (Model DQ))
              (A2              (Signal_Name    DQ2) (Model DQ))
              (A3              (Signal_Name    DQ3) (Model DQ))
              (VDD1            (Power_Name   VDD))
              (VDD2            (Power_Name   VDD))
              (VSS1            (Gnd_Name      VSS))
              (VSS2            (Gnd_Name      VSS))
       )
       (Interconnect   | On-Die
              (Full_Die
                     (Tstonefile full_die.s16p)
                     (Model_Ports
                           (1 A1)(2 A2)(3 A3)(4 B.A1)(5 B.A2)(6 B.A3)
                           (7 VDD1) (8 VDD2)(9 VSS1)(10 VSS2)
                           (11 Pu.A1)(12 Pu.A2)(13 Pu.A3)
                           (14 Pd.A1)(15 Pd.A2)(16 Pd.A3)
                     )
              )
       )
```

# die.ibsx (Legacy IV/VT or IBIS-BSS)

```
(Models
    (DQ  (Supplies (PuRef VDD) (PdRef VSS))
        (Thresholds (Vinl .7) (Vinh .9) (Vmeas .8))
        (Voltage_Range 1.200V )
        (Legacy_IV/VT
            (C_comp (Corner 1pF 1.5pF .8pF))
            |    (C_comp (Range1pF .8pF 1.5pF))
            (Ramp (dV/dt_r 430.781mV/76.796ps) (dV/dt_f 426.037mV/71.420ps))
            (Pulldown …) (Pullup …) (GND_Clamp …)(Power_Clamp …)
            (Falling_Waveform …) (Rising_Waveform …)
            (Falling_Waveform …) (Rising_Waveform …))))
| OR
(Models
    (DQ  (Supplies (PuRef VDD) (PdRef VSS))
        (Thresholds (Vinl .7) (Vinh .9) (Vmeas .8))
        (Voltage_Range 1.200V )
        (IBIS-BSS
            (File_Name DQ.bss)
            (Circuit_Name DQ)
            (Stimulus (Trise 75ps)(Tfall 71ps)(Vlow 0)(Vhigh 1.2))
            (Enable 0 1.2)
            (Model_Ports
                (1 Drive)(2 Signal)(3 Enable)(4 PuRef)(5 PdRef))))))
```

# die.ibsx with separate Buffer list

```
(die   (IBIS_Ver  6.0)   (Description "…")
       (File_Rev "…")  (Copyright "…")  (Notes "…")  (Date "…")  (Disclaimer "…")  (Manufacturer "…")
       (File_Name            die.ibsx)
       (Chip_Name            die)
       (Number_Of_Pins     7)
       (Pads    |  "Bump Pads" of flip chip IC
              (A1              (Signal_Name    DQ1))
              (A2              (Signal_Name    DQ2))
              (A3              (Signal_Name    DQ3))
              (VDD1            (Power_Name   VDD))
              (VDD2            (Power_Name   VDD))
              (VSS1            (Gnd_Name       VSS))
              (VSS2            (Gnd_Name       VSS))
       )
       (Buffers    |  Buffers
              (B.A1            (Signal_Name    DQ1) (Model DQ))
              (B.A2            (Signal_Name    DQ2) (Model DQ))
              (B.A3            (Signal_Name    DQ3) (Model DQ))
       )
       (Extended_Nets
              (DQ1 A1 B.A1) (DQ2 A2 B.A2) (DQ3 A3 B.A3)
              (VDD VDD1 VDD2 B.A1.Pu B.A2.Pu B.A3.Pu)
              (VSS VSS1 VSS2 B.A1.Pd B.A2.Pd B.A3.Pd)
       )
```

# BIRD Status

| IBIS Version | BIRD No. | BIRD Name |
|---|---|---|
| Reject | 116 | Add IBIS-ISS to [External Model] and [External Circuit] as a Supported Language |
| Reject | 117.3 | Parameterize A_to_D and D_to_A Converters |
| Reject | 118.2 | Analog Parameter Assignments |
| IBIS 5.2 | 121.1 | IBIS-AMI New Reserved Parameters for Data Management |
| Reject | 122 | IBIS-AMI New Reserved Parameters for Analog Modeling |
| IBIS 5.2 | 123.2 | IBIS-AMI New Reserved Parameters for Jitter/Noise |
| Reject | 124 | IBIS-AMI New Reserved Parameters for Dependency Tables |
| Reject | 125.1 | Make IBIS-ISS Available for IBIS Package Modeling |
| IBIS 5.3 | 128 | Allow AMI_parameters_out to pass AMI_parameters_in data on calls to AMI_GetWave |
| Reject | 129 | Add "polarity" Argument to D_to_A Converters |
| IBIS 5.2 | 131 | IBIS-AMI Repeaters |
| Reject | 144.3 | Add TOUCHSTONE to [External Model] and [External Circuit] as a Supported Language |
| Reject | 145.2 | Instantiation of IBIS I/O buffers in an [External Circuit] using the [Model Call] keyword |
| IBIS 5.3 | 147 | Back-channel support |
| IBIS 5.2 | 150 | IBIS-AMI New Reserved Parameters for Dependency Tables |
| Reject | 152 | Analog Model Boundary Definition |
| IBIS 6.0 | | EMD - Supercede EBD, ICM, IBIS (Package) |
| IBIS 6.0 | | IBISx - Supercede IBIS (Die) |
| IBIS 6.0 | | IBIS-ISS Interconnect for EMD and IBISx |
| IBIS 6.0 | | IBIS-BSS Enhance IBIS-ISS with Macro Models (e.g. PWL Controlled Voltage and Current Sources) |