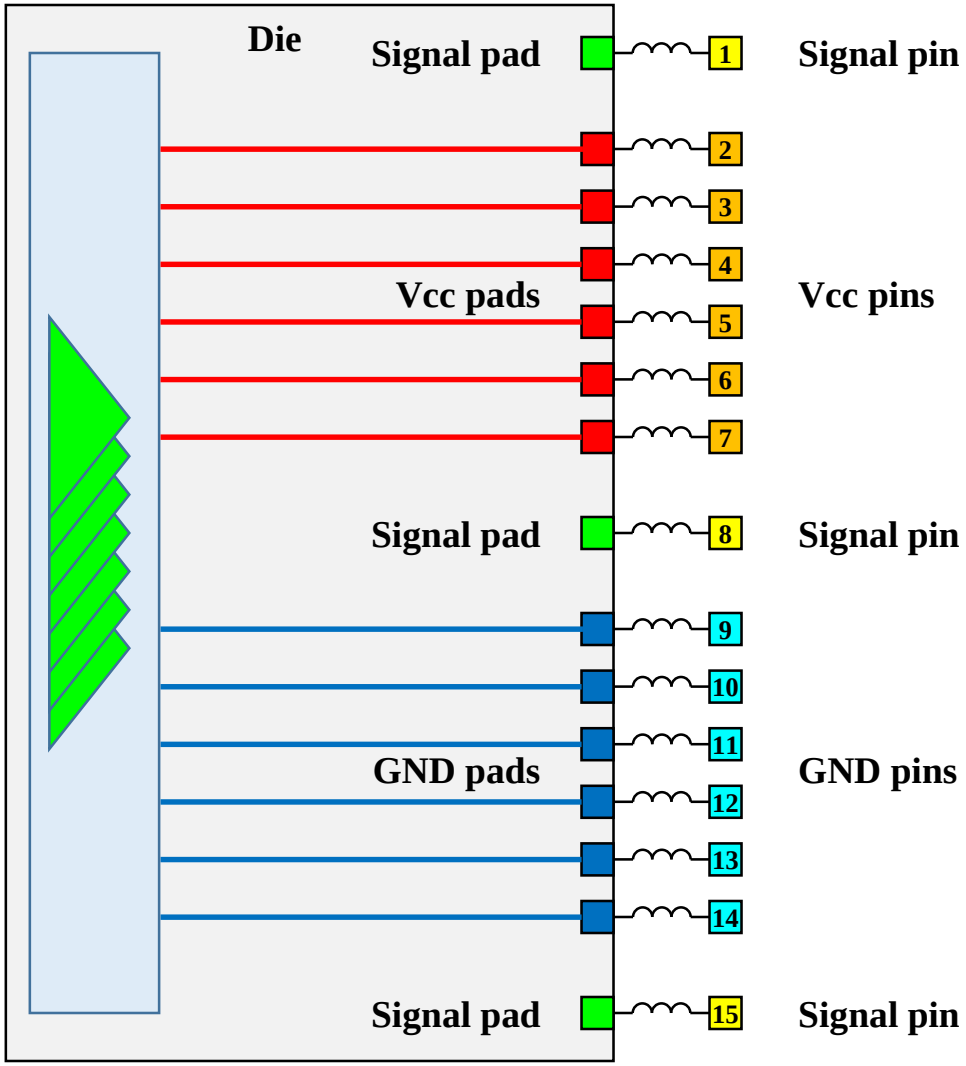
[Define Package Model] ambiguity in IBIS v6.0

Arpad Muranyi (Mentor Graphics)
Randy Wolff (Micron Technology)

IBIS-ATM teleconference

March 31, 2015

Without power or ground bus definitions (no [Pin Mapping] keyword)



Case 1:
[Package] keyword only
- **all pins get the [Package]/[Pin] RLC**

Case 2:
All pins are listed in [Define Package Model]
- **all pins get the model in [Define Package Model]**

Case 3:
If the [Define Package Model] is a partial model and lists only pins 1, 2, 14, 15
- **these pins get model from [Define Package Model]**

How should the rest of the pins be modeled?

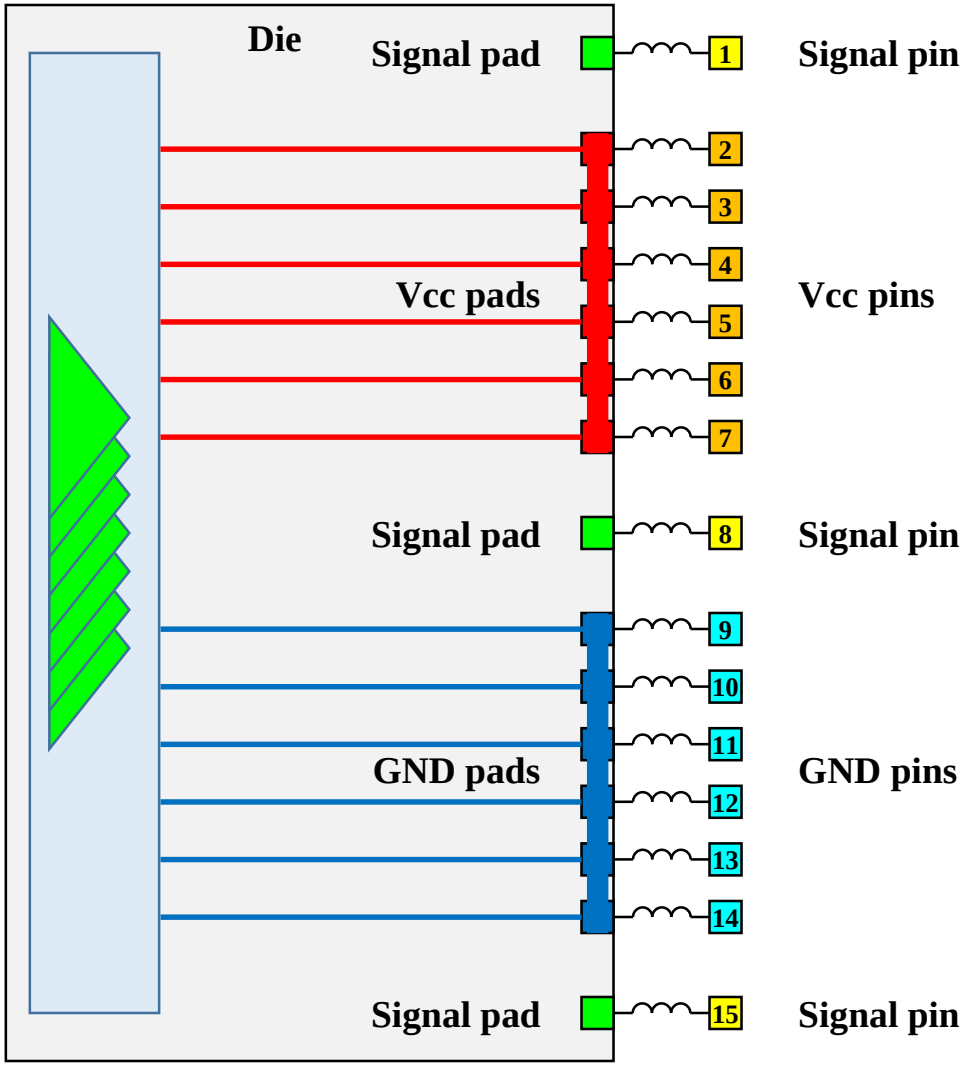
1) **use [Package] /[Pin] RLC?**
2) **use an open between pin and pad?**
3) **use a short between pin and pad?**

Note: None of these cases have information on how buffers and power/ground pins are connected, consequently the buffers can only be powered by ideal sources directly at their power terminals using the [Voltage Range] and related keywords.

Signal pins missing in [Define Package Model] should use the [Package]/[Pin] RLC values.

For these cases all power and ground package parasitics can be ignored

With power or ground bus definitions using [Pin Mapping]



Case 1:
[Package] keyword only

- all pins get the [Package]/[Pin] RLC
- using the information in [Pin Mapping], buffers can be associated with specific power/ground pins
- consequently buffers can be powered through the pins and the package model
- Note: Package parasitics may get "shunted" in parallel if pins are also shorted

Case 2:
All pins are listed in [Define Package Model]

- all pins get the model in [Define Package Model]
- using the information in [Pin Mapping], buffers can be associated with specific power/ground pins
- consequently buffers can be powered through the pins and the package model
- Note: Package parasitics may get "shunted" in parallel if pins are also shorted

Case 3:
If the [Define Package Model] is a partial model and lists only pins 1, 2, 14, 15

- these pins get model from [Define Package Model]

How should the rest of the pins be modeled?

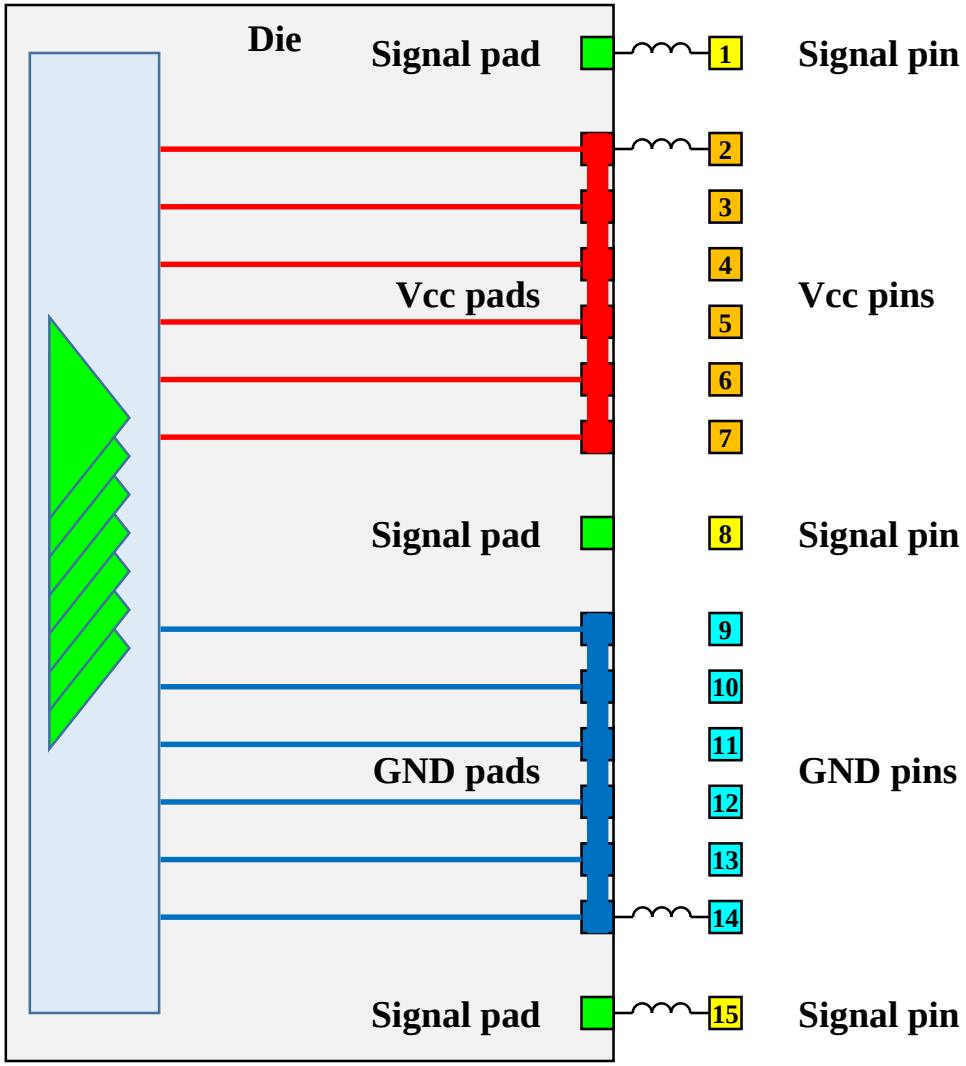
1) use [Package] /[Pin] RLC?
2) use an open between pin and pad?
3) use a short between pin and pad?

- missing signal pins should get [Package]/[Pin] RLC

What if the model maker wants to "merge" the power and/or ground parasitics into one corresponding pin, knowing that the bus defined in [Pin Mapping] is an ideal short at the pads?

The answer depends on the meaning of the model data!

What is the “expectation” with the following partial [Define Package Model]?



Signal pin:

Use [Package]/[Pin] RLC

- **this makes the most sense to me, because it includes whatever package model is available**

Use a short

- **possible, but doesn’t include package effects**

Use an open

- **makes no sense, buffer model is disconnected from the pin**

Power/ground pins:

Use [Package]/[Pin] RLC

- **this would be consistent with the signal pins**
- **but it does NOT include all coupling effects**

Use a short

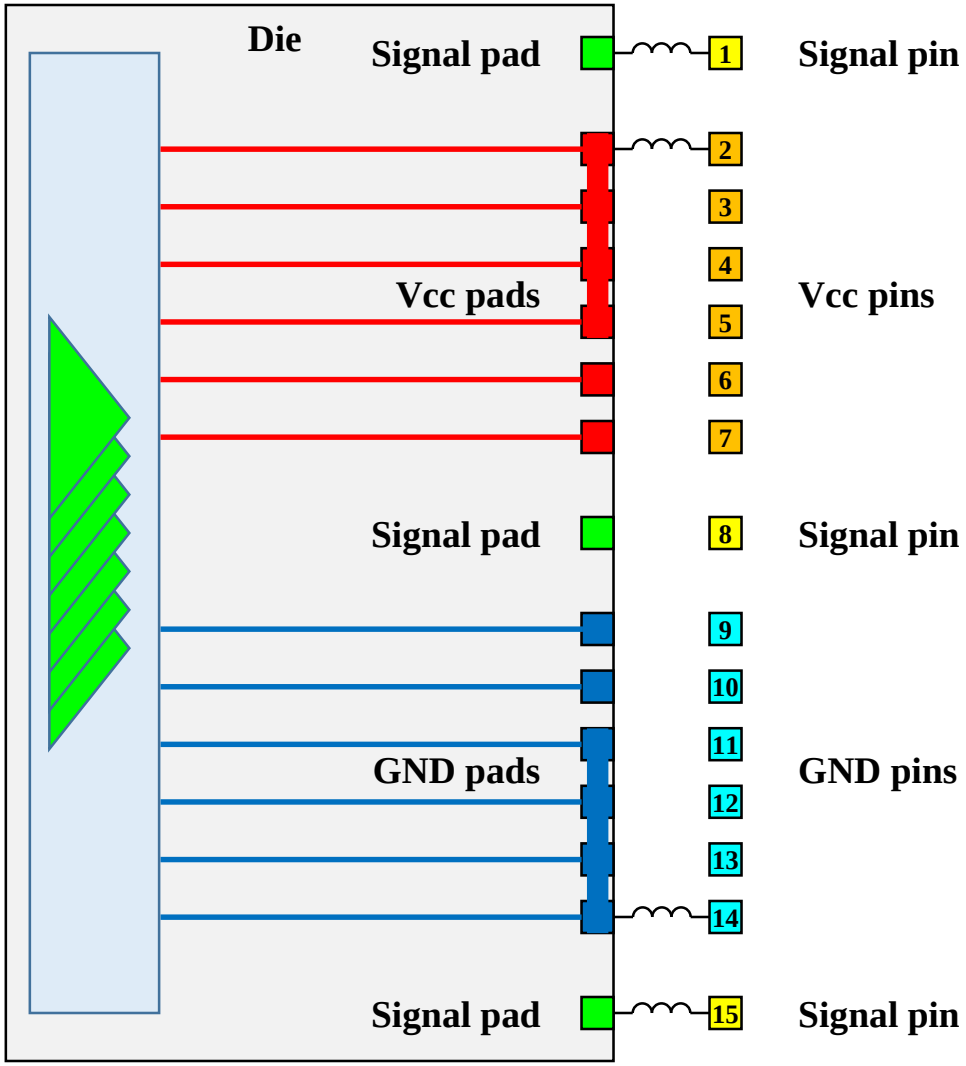
- **possible, but excludes any package effects for those pins which are not defined in [Define Package Model]**
- **it can short out the package parasitics for those pins which are defined in [Define Package Model] when the pins are shorted**

Use an open

- **possible, but assumes that missing package parasitics are merged into the defined pin’s package parasitics**

Using [Package]/[Pin] RLC would be consistent with pg. 20 in IBIS v6.0

What about this case (pins 6, 7, 9, 10 not defined in [Pin Mapping])?



Pins 6, 7, 9, 10:
Since these pins are not mentioned in the [Pin Mapping] keyword, they are not associated with any of the buffer models ([Model] keywords). For this reason these pins and their package parasitics may be ignored in all simulations.

There is no need for a package model of any sort between pins 6, 7, 9, 10 and their corresponding pads to provide power to a buffer [Model]s because no buffer [Model] can be associated with them.

Why model makers would want to use “merging”

R, L and C matrices must be the same size in IBIS. This makes it nearly impossible to take RLC data from any simulator and convert it into the IBIS matrix format. The C matrix will never have the same size as the R and L matrices unless there is never more than one pin connected to each power or ground path. The equivalent SPICE model would have only one C element but multiple RL elements. To generate a valid C matrix of the same size as the R and L matrices, model makers would have to post-process the simulation data and create multiple C values from a single C value. All mutual C values would have to be created properly as well.

Why model makers would not want to use [Package]/[Pin] RLC for power pins

Using the [Package]/[Pin] RLC data for signal pins not defined in [Define Package Model] is acceptable

However, the same rule is difficult at best to apply to power and ground pins and it seems that it is better not to use RLC data from the [Package]/[Pin] keywords for power and ground pins not defined in [Define Package Model]

- **For data in the [Pin] keyword, you run into the issues of representing the capacitance of a plane on multiple pins**
- **No ability to define critically important mutual L and C**
- **For data in the [Package] keyword, the problem is about the min/max values. People use the min/max values based on the signal parasitics, which is useless for the power/ground corner cases.**

Conclusions for the IBIS specification

- **It seems that the only way to provide valid RLC data for PI simulations is if the data is located in the [Define Package Model] keyword, and if multiple power/ground pins are merged into one pin while the remaining pins in the group are left undefined**

- **A simple update to IBIS could describe that when the [Pin Mapping] keyword defines power/ground buses that span over multiple power/ground pins (i.e. pads), the package parasitics of those power/ground pins should be merged into a single pin representation per group in the [Define Package Model] keyword and only one of the pin names for each of those groups should be present in the [Pin Numbers] keyword of the [Define Package Model] keyword**

- **Even though the new package/on-die interconnect specification proposal for IBIS is expected to resolve these problems, it might still be worth adding this change for the legacy package modeling syntax, since there may be numerous models which will never use the new package modeling syntax**