Are [Interconnect Model]s scoped by the [Interconnect Model Set], or do they appear in the top level in an IBIS file and just referenced by the [Interconnect Model Set]?

Every (almost every) component has either a pin 1 or a pin A1. It is only logical to identify [Interconnect Model]s by the pin(s) they connect. Putting [Interconnect Model]s at the top level and referencing them by name in the [Interconnect Model Set] will create colisions between the names of [Interconnect Model]s between different [Interconnect Model Set]s.

Must all [Interconnect Model]s in a single [Component] used in a single simulation be in a single [Interconnect Model Set], or can the be in multiple [Interconnect Model Set]s with in a single [Interconnect Model Set Selector]?

We have already discussed the advantages of partitioning the i=package interconnect into two or more [Interconnect Model Set]s (e.g. separate [Interconnect Model Set]s for DDR4, PCIe, SATA, … There are clear advantages for also having separate [Interconnect Model Set]s for Power Delivery Networks (PDN).

If we want to simulate both DDR4 and PCIe together, or DDR4 and PDN together, or PCIe and PDN together, it only makes sense for an EDA tool to allow the user to select more than one [Interconnect Model Set]s for a single simulation.

There are other alternatives to this capability, such as adding an [Include] capability to IBIS or just repeating the PDN [Interconnect Model] in both the DDR4 and PCIe [Interconnect Model Set]s.

Ar

```
[IBIS Ver]     7.0
[File Name]    interconnect_model_set.ibs
[Date]         07/25/2016
[File Rev]     1.0
[Source]       Walter Katz
|
|
[Component]      pkg1
[Interconnect Model Set Selector]
Interconnect_Model_Set pkg1_A pkg1_a.ims
Interconnect_Model_Set pkg1_B pkg1_b.ims
[End Interconnect Model Set Selector]
|
[Pin]    signal_name          model_name      R_pin     L_pin     C_pin
A1       A6                   DQ              200.0m    1.0nH 00  0.5pF
A2       A0                   DQ              200.0m    1.0nH 00  0.5pF
L7       A1                   ADDR            200.0m    1.0nH 00  0.5pF
L8       A5                   ADDR            200.0m    1.0nH 00  0.5pF
M1       VDD                  POWER
N1       VSS                  GND
|
[Component]      pkg2
[Interconnect Model Set Selector]
Interconnect_Model_Set pkg2 pkg2.ims
[End Interconnect Model Set Selector]
|
[Pin]    signal_name          model_name      R_pin     L_pin     C_pin
1        A6                   DQ              200.0m    1.0nH 00  0.5pF
2        A0                   DQ              200.0m    1.0nH 00  0.5pF
3        A1                   ADDR            200.0m    1.0nH 00  0.5pF
4        A5                   ADDR            200.0m    1.0nH 00  0.5pF
5        VDD                  POWER
6        VSS                  GND
|
[Component]      pkg3
[Interconnect Model Set Selector]
Interconnect_Model_Set pkg3_DQ   pkg3.ims
Interconnect_Model_Set pkg3_ADDR pkg3.ims
Interconnect_Model_Set pkg3_PDN  pkg3.ims
[End Interconnect Model Set Selector]
|
[Pin]    signal_name          model_name      R_pin     L_pin     C_pin
A1       A6                   DQ              200.0m    1.0nH 00  0.5pF
A2       A0                   DQ              200.0m    1.0nH 00  0.5pF
L7       A1                   ADDR            200.0m    1.0nH 00  0.5pF
L8       A5                   ADDR            200.0m    1.0nH 00  0.5pF
M1       VDD                  POWER
N1       VSS                  GND
[Model] DQ
[Model] ADDR
```

```
|
[End]
```

File pkg1_a.ims

```
[Interconnect Model Set] pkg1_A
Manufacturer Acme, Inc
|
[Interconnect Model] A1
File_IBIS-ISS     pkg1a.iss PATH
Param L Value .2
Number_of_terminals 3
1 Pin_I/O A1
2 Buf_I/O A1
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] A2
File_IBIS-ISS     pkg1a.iss PATH
Param L Value .25
Number_of_terminals 3
1 Pin_I/O A2
2 Buf_I/O A2
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] L7
File_IBIS-ISS     pkg1a.iss PATH
Param L Value .15
Number_of_terminals 3
1 Pin_I/O L7
2 Buf_I/O L7
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] L8
File_IBIS-ISS     pkg1a.iss PATH
Param L Value .3
Number_of_terminals 3
1 Pin_I/O L8
2 Buf_I/O L8
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] PDN
File_IBIS-ISS     pkg1a.iss PDN
Number_of_terminals 4
1 Pin_Rail VDD
2 Pin_Rail VSS
3 Buf_Rail VDD
4 Buf_Rail VSS
[End Interconnect Model]
[End Interconnect Model Set]
```

File pkg1_b.ims

```
[Interconnect Model Set] pkg1_B
Manufacturer Apex, Inc
|
[Interconnect Model] A1
File_IBIS-ISS     pkg1b.iss PATH
Param L Value .2
Number_of_terminals 3
1 Pin_I/O A1
2 Buf_I/O A1
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] A2
File_IBIS-ISS     pkg1b.iss PATH
Param L Value .25
Number_of_terminals 3
1 Pin_I/O A2
2 Buf_I/O A2
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] L7
File_IBIS-ISS     pkg1b.iss PATH
Param L Value .15
Number_of_terminals 3
1 Pin_I/O L7
2 Buf_I/O L7
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] L8
File_IBIS-ISS     pkg1b.iss PATH
Param L Value .3
Number_of_terminals 3
1 Pin_I/O L8
2 Buf_I/O L8
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] PDN
File_IBIS-ISS     pkg1b.iss PDN
Number_of_terminals 4
1 Pin_Rail VDD
2 Pin_Rail VSS
3 Buf_Rail VDD
4 Buf_Rail VSS
[End Interconnect Model]
[End Interconnect Model Set]
```

File pkg2.ims

```
[Interconnect Model Set] pkg2
Manufacturer Acme, Inc
|
[Interconnect Model] 1
File_IBIS-ISS     pkg2.iss PATH
Param L Value .2
Number_of_terminals 3
1 Pin_I/O  1
2 Buf_I/O  1
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] 2
File_IBIS-ISS     pkg2.iss PATH
Param L Value .25
Number_of_terminals 3
1 Pin_I/O 2
2 Buf_I/O 2
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] 3
File_IBIS-ISS     pkg2.iss PATH
Param L Value .15
Number_of_terminals 3
1 Pin_I/O 3
2 Buf_I/O 3
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] 4
File_IBIS-ISS     pkg2.iss PATH
Param L Value .3
Number_of_terminals 3
1 Pin_I/O 4
2 Buf_I/O 4
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] PDN
File_IBIS-ISS     pkg2.iss PDN
Number_of_terminals 4
1 Pin_Rail VDD
2 Pin_Rail VSS
3 Buf_Rail VDD
4 Buf_Rail VSS
[End Interconnect Model]
[End Interconnect Model Set]
```

File pkg3.ims

```
[Interconnect Model Set] pkg3_DQ
Manufacturer Apex, Inc
|
[Interconnect Model] A1
File_IBIS-ISS     pkg3.iss PATH
Param L Value .2
Number_of_terminals 3
1 Pin_I/O A1
2 Buf_I/O A1
3 Pin_Rail VSS
[End Interconnect Model]
|
[Interconnect Model] A2
File_IBIS-ISS     pkg3.iss PATH
Param L Value .25
Number_of_terminals 3
1 Pin_I/O A2
2 Buf_I/O A2
3 Pin_Rail VSS
[End Interconnect Model]
[End Interconnect Model Set]
|
|
[Interconnect Model Set] pkg3_ADDR
Manufacturer Apex, Inc
|
[Interconnect Model] L7
File_IBIS-ISS     pkg3.iss PATH
Param L Value .15
Number_of_terminals 3
1 Pin_I/O L7
2 Buf_I/O L7
3 Pin_Rail VSS
[End Interconnect Model]

[Interconnect Model] L8
File_IBIS-ISS     pkg3.iss PATH
Param L Value .3
Number_of_terminals 3
1 Pin_I/O L8
2 Buf_I/O L8
3 Pin_Rail VSS
[End Interconnect Model]
[End Interconnect Model Set]
|
[Interconnect Model Set] pkg3_PDN
[Interconnect Model] PDN
File_IBIS-ISS     pkg3.iss PDN
Number_of_terminals 4
1 Pin_Rail VDD
```

```
2 Pin_Rail VSS
3 Buf_Rail VDD
4 Buf_Rail VSS
[End Interconnect Model]
[End Interconnect Model Set]
```

Suppose we wanted to use PDN in both pkg3_DQ and pkg3_ADDR:

This can be handled three ways:

1. Add to IBIS a new keyword [Include]
    a. [Include] <FileName> {<Section>}
2. Allowing the user to select more than one [Interconnect Model Set]s
3. Use just copies the following into both pkg3_DQ and pkg3_ADDR:

[Interconnect Model] PDN
File_IBIS-ISS pkg3.iss PDN
Number_of_terminals 4
1 Pin_Rail VDD
2 Pin_Rail VSS
3 Buf_Rail VDD
4 Buf_Rail VSS
[End Interconnect Model]