Introduction to the IBIS Macro Model Library

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February 9, 2006

Contents of the library

- Three resistors
  - R, VCR, CCR
- Three capacitors
  - C, VCC, CCC
- Four inductors
  - L, VCL, CCL, K
- 22 voltage and 22 current sources, including
  - Delay, Min, Max, Abs, Sum, Mult, Div, PWL
- An ideal T-line
- Eight IBIS buffers
  - Input, Output, IO, 3-state, Opensource, IO_opensource, Opensink, IO_opensink

Philosophy of examples

- Assumption:
  - HSPICE with Verilog-A option installed, and/or
  - SMASH installed (for the VHDL-A(MS) examples)
- All examples are ready to go
  - No editing is necessary, just simulate and look at the waveforms
  - The examples are simple, just enough to show the concept
  - No attempt was made to show all possibilities
  - The data files contain very short data tables so the waveforms may not all be smooth and rounded
  - Some lines are commented out in the VHDL-A(MS) building blocks to allow them work in the evaluation version of SMASH (Seduction)
- A PERL script has been developed to extract and reformat the data from IBIS files so that the library building blocks can read it

Test suite architecture

- Top level SPICE files
  - Include the simulation control statements
  - Contain simple stimulus source(s), load(s) and a call to the macro model netlist (i.e. template)
  - Equivalent of the SI simulator tool’s IBIS environment with an IBIS file using an [External Model] or [External Circuit] statement
- “Macro model template”-s
  - Contain Verilog-A(MS) or VHDL-A(MS) netlists to instantiate the building blocks from the library
  - Show how to pass parameter values into the instances
  - Equivalent of a “complicated buffer’s” macro model
- Model library file
  - Contains the various building blocks of “primitives”

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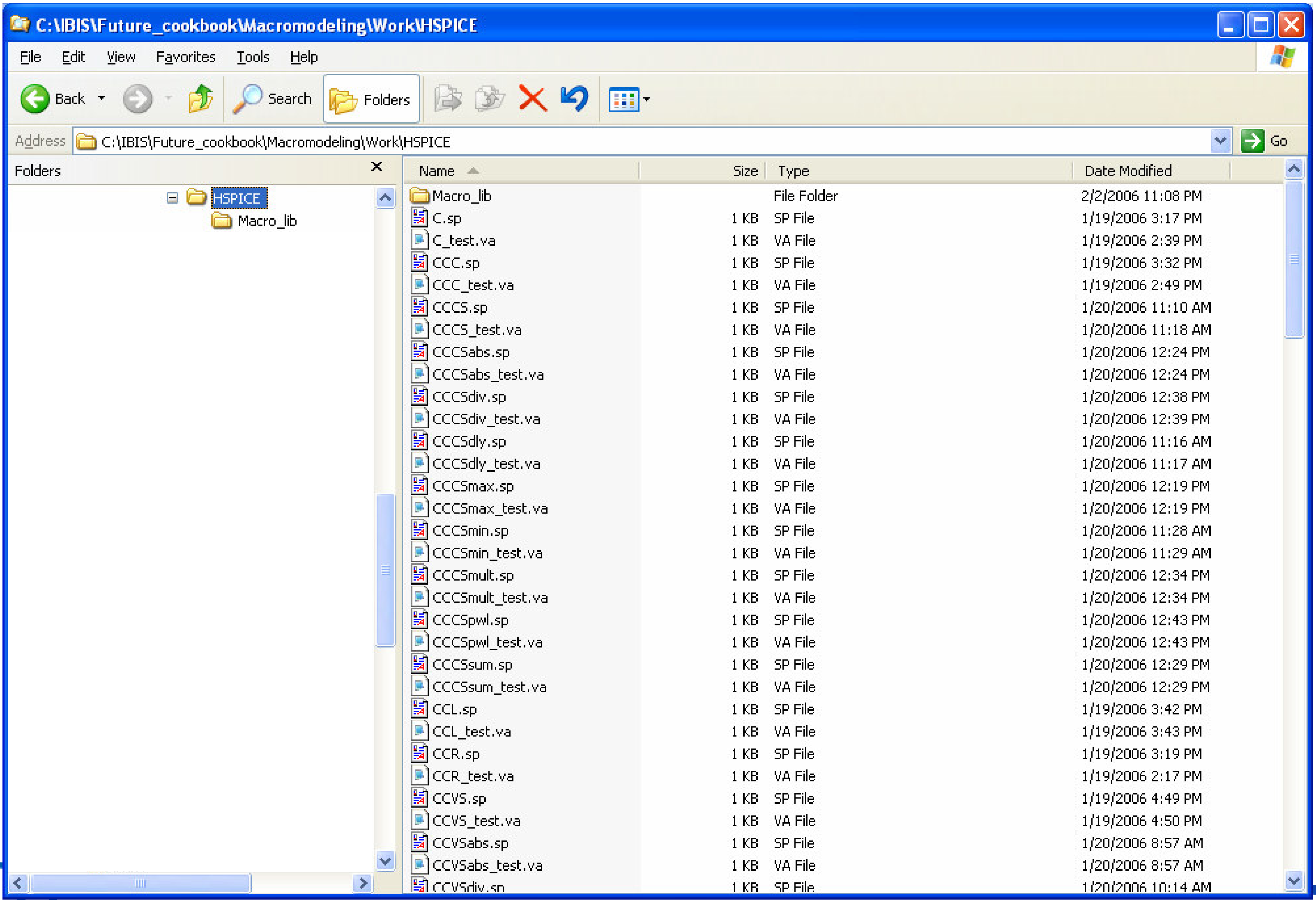
File system of the Verilog-A(MS) distribution for HSPICE

- Installation directory of your choice
  - One .sp and .va file per library building block
  - The .sp file contains the simulation control and stimulus statements and the call to the .va netlist (or the “template” file)
- Macro_lib subdirectory
  - Contains two mandatory files and the library file
    - constants.vams
    - disciplines.vams
    - IBIS_macro_library.va
  - plus a small collection of parameter data files (*.dat)
    - these files contain IBIS buffer parameters, such as C_comp, I-V and V-t tables, or
    - appropriate data tables for the PWL sources

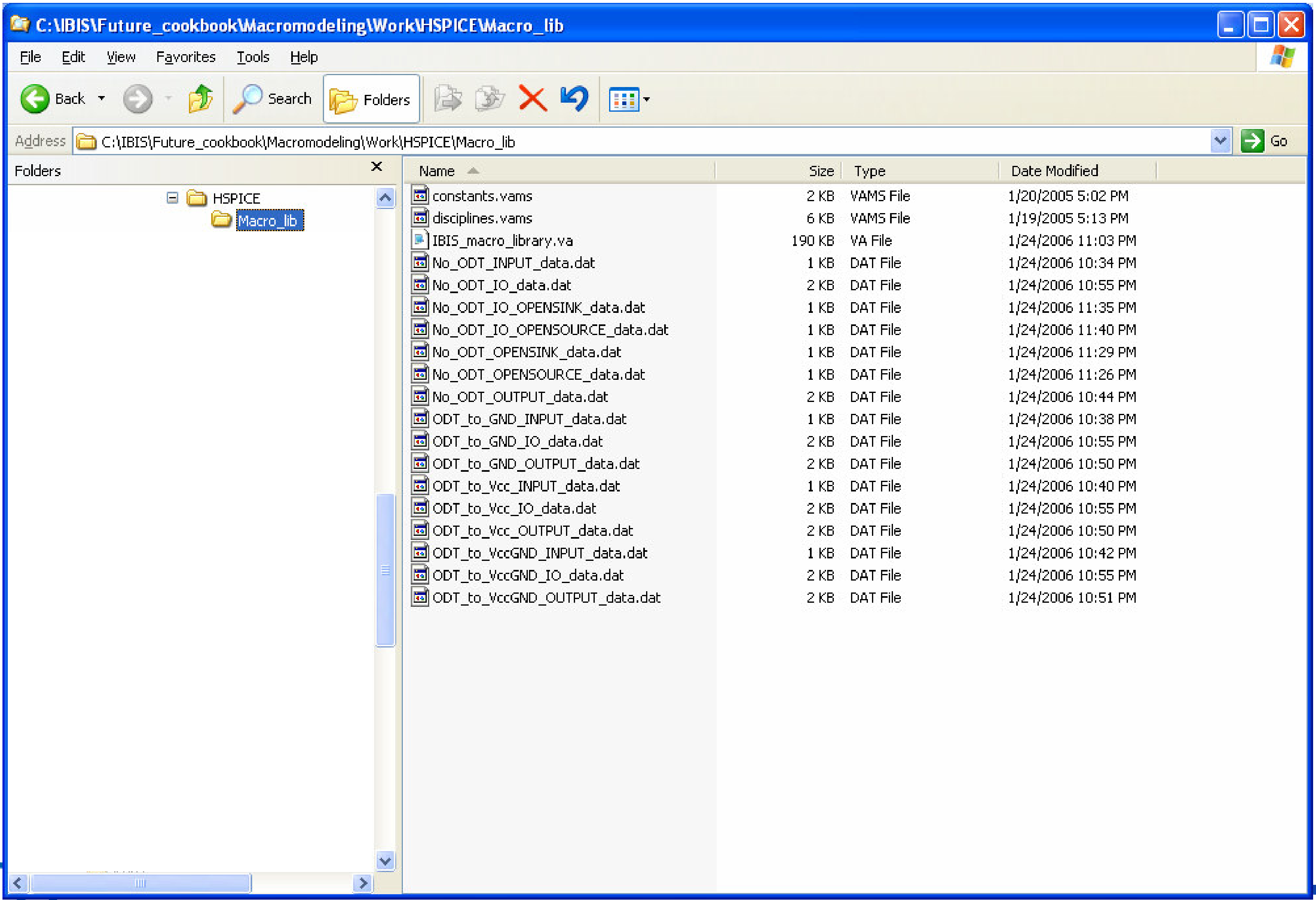
*Other brands and names are the property of their respective owners

File system of the Verilog-A(MS) distribution for HSPICE


C:\IBIS\Future_cookbook\Macromodeling\Work\HSPICE
File
Edit
View
Favorites
Tools
Help
Back
Search
Folders
Address
C:\IBIS\Future_cookbook\Macromodeling\Work\HSPICE
Go
Folders
HSPICE
Macro_lib

Name	Size	Type	Date Modified
Macro_lib		File Folder	2/2/2006 11:08 PM
C.sp	1 KB	SP File	1/19/2006 3:17 PM
C_test.va	1 KB	VA File	1/19/2006 2:39 PM
CCC.sp	1 KB	SP File	1/19/2006 3:32 PM
CCC_test.va	1 KB	VA File	1/19/2006 2:49 PM
CCCS.sp	1 KB	SP File	1/20/2006 11:10 AM
CCCS_test.va	1 KB	VA File	1/20/2006 11:18 AM
CCCSabs.sp	1 KB	SP File	1/20/2006 12:24 PM
CCCSabs_test.va	1 KB	VA File	1/20/2006 12:24 PM
CCCSdiv.sp	1 KB	SP File	1/20/2006 12:38 PM
CCCSdiv_test.va	1 KB	VA File	1/20/2006 12:39 PM
CCCSdly.sp	1 KB	SP File	1/20/2006 11:16 AM
CCCSdly_test.va	1 KB	VA File	1/20/2006 11:17 AM
CCCSmax.sp	1 KB	SP File	1/20/2006 12:19 PM
CCCSmax_test.va	1 KB	VA File	1/20/2006 12:19 PM
CCCSmin.sp	1 KB	SP File	1/20/2006 11:28 AM
CCCSmin_test.va	1 KB	VA File	1/20/2006 11:29 AM
CCCSmult.sp	1 KB	SP File	1/20/2006 12:34 PM
CCCSmult_test.va	1 KB	VA File	1/20/2006 12:34 PM
CCCSpwl.sp	1 KB	SP File	1/20/2006 12:43 PM
CCCSpwl_test.va	1 KB	VA File	1/20/2006 12:43 PM
CCCSsum.sp	1 KB	SP File	1/20/2006 12:29 PM
CCCSsum_test.va	1 KB	VA File	1/20/2006 12:29 PM
CCL.sp	1 KB	SP File	1/19/2006 3:42 PM
CCL_test.va	1 KB	VA File	1/19/2006 3:43 PM
CCR.sp	1 KB	SP File	1/19/2006 3:19 PM
CCR_test.va	1 KB	VA File	1/19/2006 2:17 PM
CCVS.sp	1 KB	SP File	1/19/2006 4:49 PM
CCVS_test.va	1 KB	VA File	1/19/2006 4:50 PM
CCVSabs.sp	1 KB	SP File	1/20/2006 8:57 AM
CCVSabs_test.va	1 KB	VA File	1/20/2006 8:57 AM
CCVSdiv.sp	1 KB	SP File	1/20/2006 10:14 AM

File system of the Verilog-A(MS) distribution for HSPICE



C:\IBIS\Future_cookbook\Macromodeling\Work\HSPICE\Macro_lib

Address C:\IBIS\Future_cookbook\Macromodeling\Work\HSPICE\Macro_lib

Name	Size	Type	Date Modified
constants.vams	2 KB	VAMS File	1/20/2005 5:02 PM
disciplines.vams	6 KB	VAMS File	1/19/2005 5:13 PM
IBIS_macro_library.va	190 KB	VA File	1/24/2006 11:03 PM
No_ODT_INPUT_data.dat	1 KB	DAT File	1/24/2006 10:34 PM
No_ODT_IO_data.dat	2 KB	DAT File	1/24/2006 10:55 PM
No_ODT_IO_OPENSINK_data.dat	1 KB	DAT File	1/24/2006 11:35 PM
No_ODT_IO_OPENSOURCE_data.dat	1 KB	DAT File	1/24/2006 11:40 PM
No_ODT_OPENSINK_data.dat	1 KB	DAT File	1/24/2006 11:29 PM
No_ODT_OPENSOURCE_data.dat	1 KB	DAT File	1/24/2006 11:26 PM
No_ODT_OUTPUT_data.dat	2 KB	DAT File	1/24/2006 10:44 PM
ODT_to_GND_INPUT_data.dat	1 KB	DAT File	1/24/2006 10:38 PM
ODT_to_GND_IO_data.dat	2 KB	DAT File	1/24/2006 10:55 PM
ODT_to_GND_OUTPUT_data.dat	2 KB	DAT File	1/24/2006 10:50 PM
ODT_to_Vcc_INPUT_data.dat	1 KB	DAT File	1/24/2006 10:40 PM
ODT_to_Vcc_IO_data.dat	2 KB	DAT File	1/24/2006 10:55 PM
ODT_to_Vcc_OUTPUT_data.dat	2 KB	DAT File	1/24/2006 10:50 PM
ODT_to_VccGND_INPUT_data.dat	1 KB	DAT File	1/24/2006 10:42 PM
ODT_to_VccGND_IO_data.dat	2 KB	DAT File	1/24/2006 10:55 PM
ODT_to_VccGND_OUTPUT_data.dat	2 KB	DAT File	1/24/2006 10:51 PM

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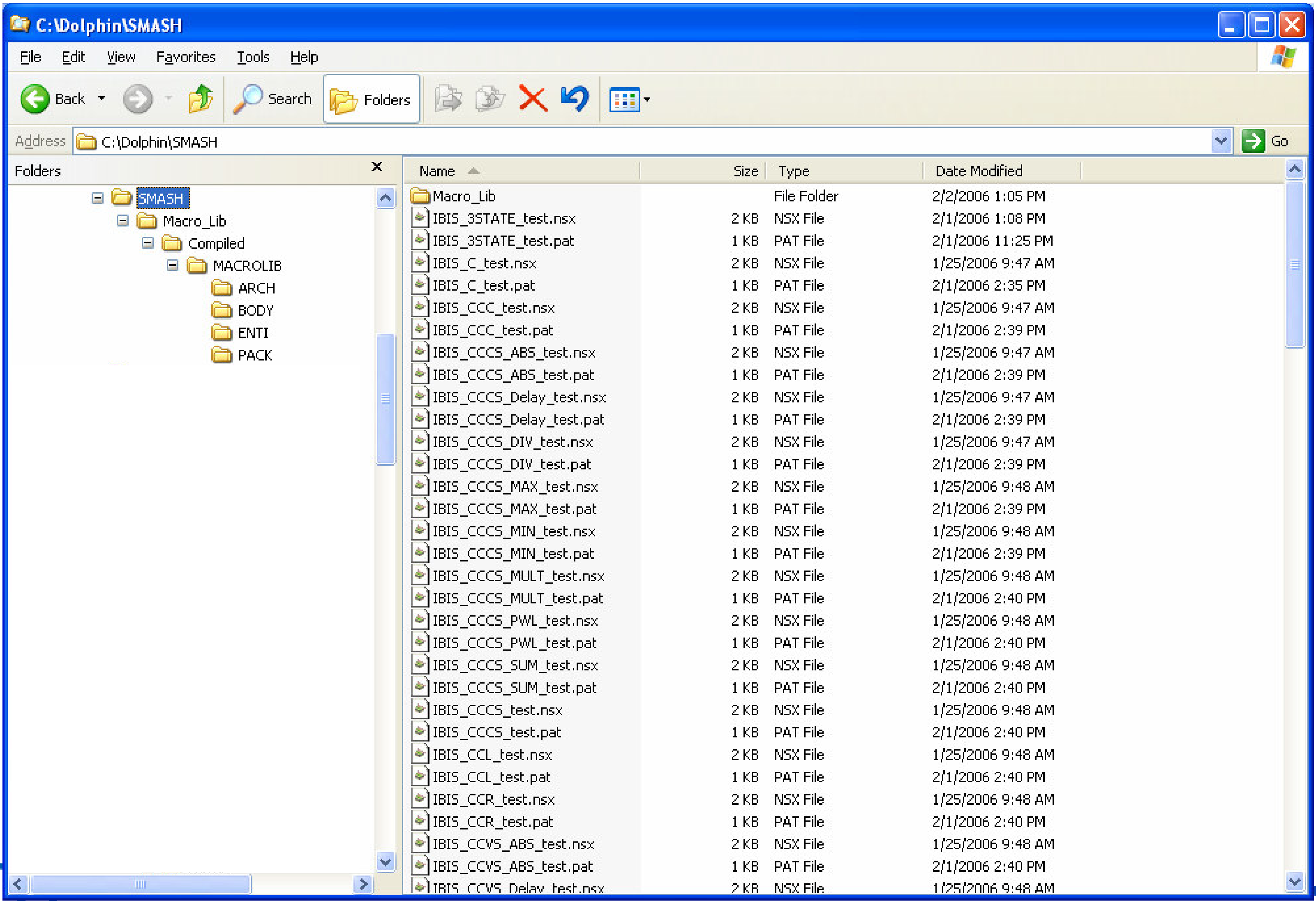
File system of the VHDL-A(MS) distribution for SMASH

- Installation directory of your choice
  - One .nsx and .pat file per library building block
  - The .pat (pattern) file contains the simulation control statements
  - The .nsx file contains both the top level SPICE and the VHDL-AMS netlist of the “template”
- Macro_lib subdirectory
  - Contains the library and a function file
    - IBIS_macro_library.vhd
    - MacroLib_functions.vhd
  - plus a collection of parameter data files (*.txt)
    - these files contain IBIS buffer parameters, such as C_comp, I-V and V-t tables, or
    - appropriate data tables for the PWL sources

File system of the VHDL-A(MS) distribution for SMASH



- SMASH
  - Macro_Lib
    - Compiled
      - MACROLIB
        - ARCH
        - BODY
        - ENTI
        - PACK

Name	Size	Type	Date Modified
Macro_Lib		File Folder	2/2/2006 1:05 PM
IBIS_3STATE_test.nsx	2 KB	NSX File	2/1/2006 1:08 PM
IBIS_3STATE_test.pat	1 KB	PAT File	2/1/2006 11:25 PM
IBIS_C_test.nsx	2 KB	NSX File	1/25/2006 9:47 AM
IBIS_C_test.pat	1 KB	PAT File	2/1/2006 2:35 PM
IBIS_CCC_test.nsx	2 KB	NSX File	1/25/2006 9:47 AM
IBIS_CCC_test.pat	1 KB	PAT File	2/1/2006 2:39 PM
IBIS_CCCS_ABS_test.nsx	2 KB	NSX File	1/25/2006 9:47 AM
IBIS_CCCS_ABS_test.pat	1 KB	PAT File	2/1/2006 2:39 PM
IBIS_CCCS_Delay_test.nsx	2 KB	NSX File	1/25/2006 9:47 AM
IBIS_CCCS_Delay_test.pat	1 KB	PAT File	2/1/2006 2:39 PM
IBIS_CCCS_DIV_test.nsx	2 KB	NSX File	1/25/2006 9:47 AM
IBIS_CCCS_DIV_test.pat	1 KB	PAT File	2/1/2006 2:39 PM
IBIS_CCCS_MAX_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCCS_MAX_test.pat	1 KB	PAT File	2/1/2006 2:39 PM
IBIS_CCCS_MIN_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCCS_MIN_test.pat	1 KB	PAT File	2/1/2006 2:39 PM
IBIS_CCCS_MULT_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCCS_MULT_test.pat	1 KB	PAT File	2/1/2006 2:40 PM
IBIS_CCCS_PWL_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCCS_PWL_test.pat	1 KB	PAT File	2/1/2006 2:40 PM
IBIS_CCCS_SUM_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCCS_SUM_test.pat	1 KB	PAT File	2/1/2006 2:40 PM
IBIS_CCCS_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCCS_test.pat	1 KB	PAT File	2/1/2006 2:40 PM
IBIS_CCL_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCL_test.pat	1 KB	PAT File	2/1/2006 2:40 PM
IBIS_CCR_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCR_test.pat	1 KB	PAT File	2/1/2006 2:40 PM
IBIS_CCVS_ABS_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM
IBIS_CCVS_ABS_test.pat	1 KB	PAT File	2/1/2006 2:40 PM
IBIS_CCVS_Delay_test.nsx	2 KB	NSX File	1/25/2006 9:48 AM

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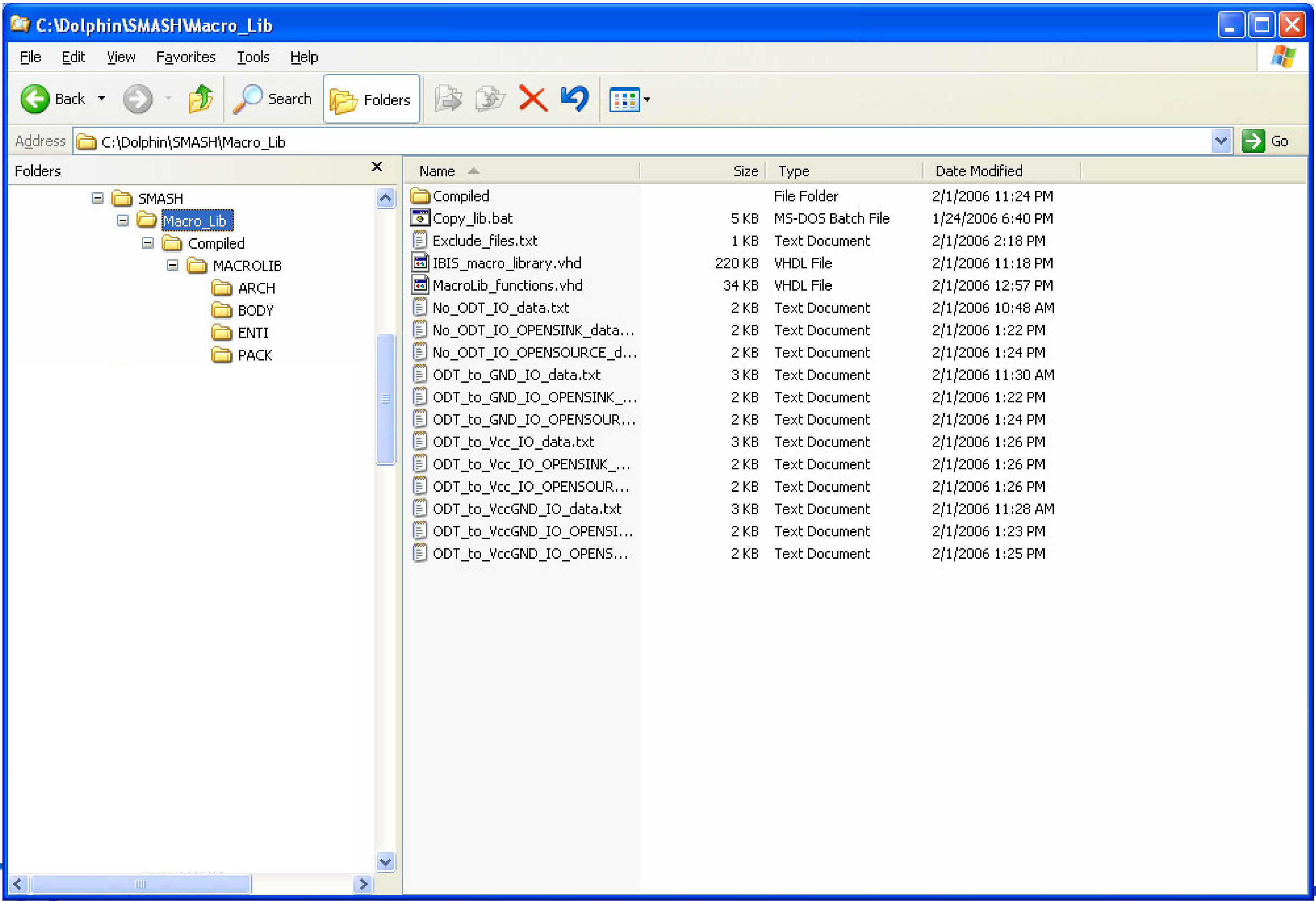
File system of the VHDL-A(MS) distribution for SMASH



C:\Dolphin\SMASH\Macro_Lib

- SMASH
  - Macro_Lib
    - Compiled
      - MACROLIB
        - ARCH
        - BODY
        - ENTI
        - PACK

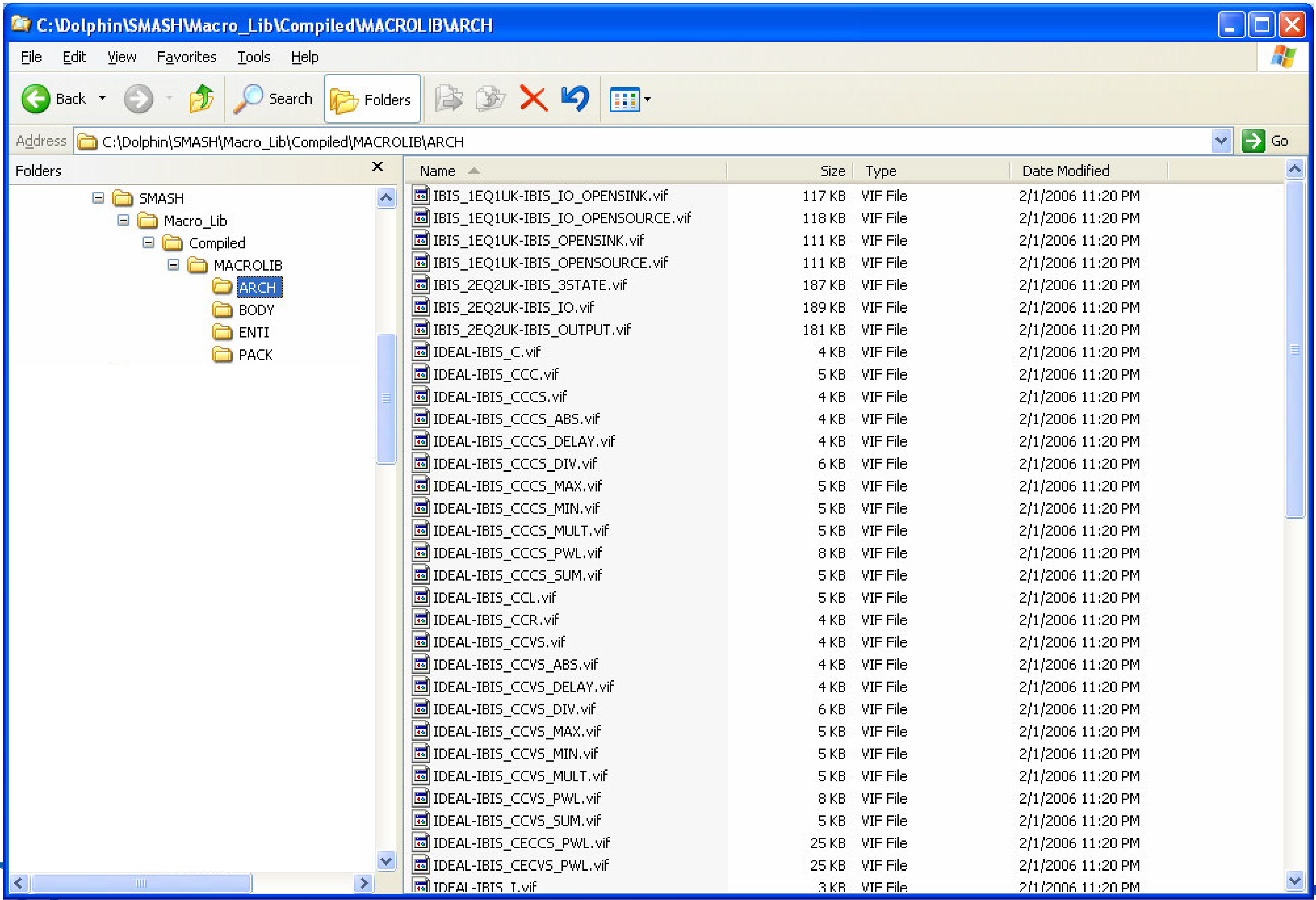
Name	Size	Type	Date Modified
Compiled		File Folder	2/1/2006 11:24 PM
Copy_lib.bat	5 KB	MS-DOS Batch File	1/24/2006 6:40 PM
Exclude_files.txt	1 KB	Text Document	2/1/2006 2:18 PM
IBIS_macro_library.vhd	220 KB	VHDL File	2/1/2006 11:18 PM
MacroLib_functions.vhd	34 KB	VHDL File	2/1/2006 12:57 PM
No_ODT_IO_data.txt	2 KB	Text Document	2/1/2006 10:48 AM
No_ODT_IO_OPENSINK_data...	2 KB	Text Document	2/1/2006 1:22 PM
No_ODT_IO_OPENSOURCE_d...	2 KB	Text Document	2/1/2006 1:24 PM
ODT_to_GND_IO_data.txt	3 KB	Text Document	2/1/2006 11:30 AM
ODT_to_GND_IO_OPENSINK_...	2 KB	Text Document	2/1/2006 1:22 PM
ODT_to_GND_IO_OPENSOUR...	2 KB	Text Document	2/1/2006 1:24 PM
ODT_to_Vcc_IO_data.txt	3 KB	Text Document	2/1/2006 1:26 PM
ODT_to_Vcc_IO_OPENSINK_...	2 KB	Text Document	2/1/2006 1:26 PM
ODT_to_Vcc_IO_OPENSOUR...	2 KB	Text Document	2/1/2006 1:26 PM
ODT_to_VccGND_IO_data.txt	3 KB	Text Document	2/1/2006 11:28 AM
ODT_to_VccGND_IO_OPENSI...	2 KB	Text Document	2/1/2006 1:23 PM
ODT_to_VccGND_IO_OPENS...	2 KB	Text Document	2/1/2006 1:25 PM

*Other brands and names are the property of their respective owners

The “Compiled” subdirectory

- The Macro_lib directory of the VHDL-A(MS) distribution includes a directory called “Compiled”
  - This contains a compiled version of the library and all of its functions as a convenience to speed up testing
  - You don’t have to use it, but it can save you time
  - The “Copy_lib.bat” file copy the compilation into the work area of each library building block example
  - (Copying is faster than compiling it 63 times)
  - The “Exclude_files.txt” file will prevent the duplication of files which do not need to be copied
- This is a SMASH specific step, other tools may deal with the WORK and user library hierarchy in a different manner

File system of the VHDL-A(MS) distribution for SMASH

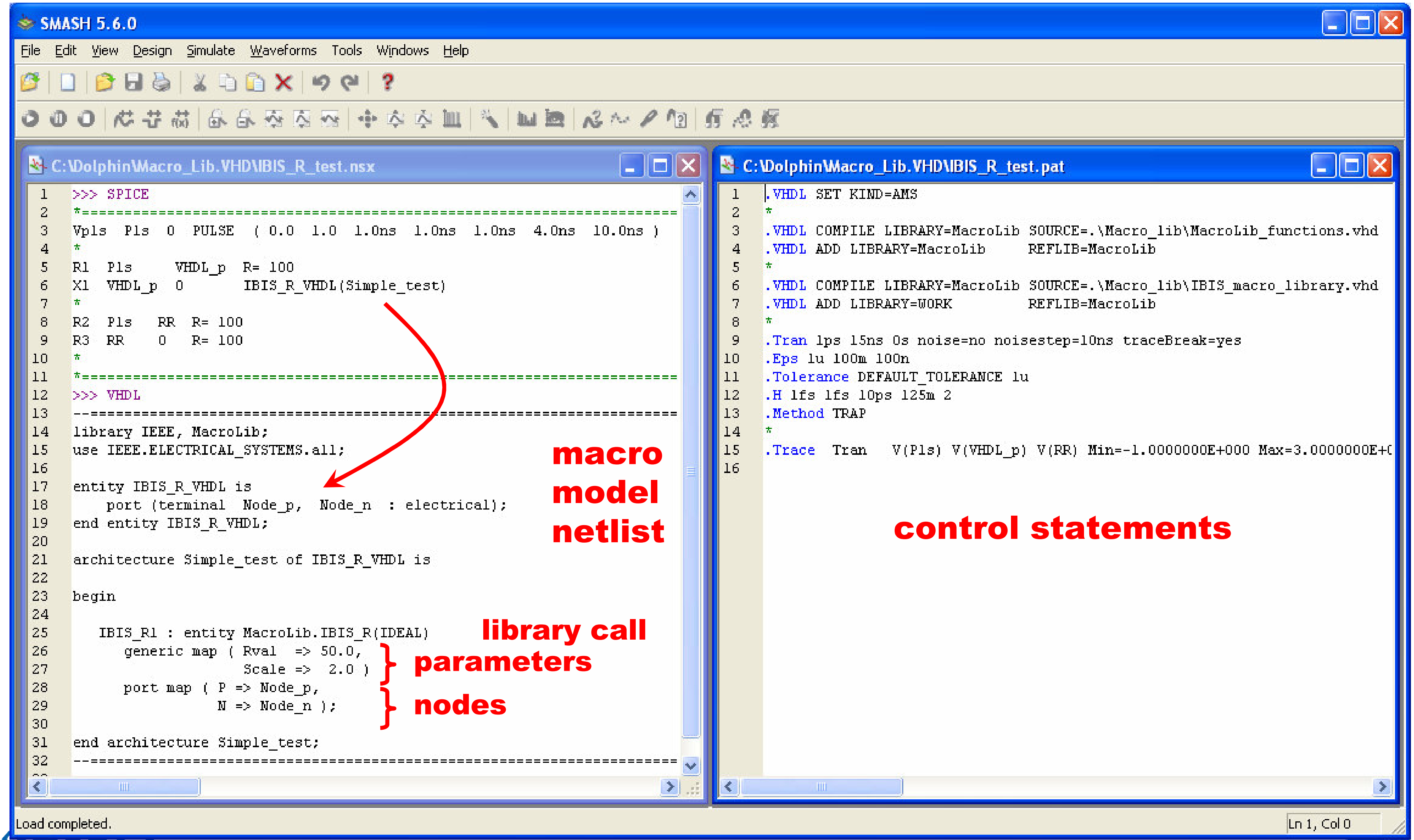


C:\Dolphin\SMASH\Macro_Lib\Compiled\MACROLIB\ARCH

Address: C:\Dolphin\SMASH\Macro_Lib\Compiled\MACROLIB\ARCH

Name	Size	Type	Date Modified
IBIS_1EQ1UK-IBIS_IO_OPENSINK.vif	117 KB	VIF File	2/1/2006 11:20 PM
IBIS_1EQ1UK-IBIS_IO_OPENSOURCE.vif	118 KB	VIF File	2/1/2006 11:20 PM
IBIS_1EQ1UK-IBIS_OPENSINK.vif	111 KB	VIF File	2/1/2006 11:20 PM
IBIS_1EQ1UK-IBIS_OPENSOURCE.vif	111 KB	VIF File	2/1/2006 11:20 PM
IBIS_2EQ2UK-IBIS_3STATE.vif	187 KB	VIF File	2/1/2006 11:20 PM
IBIS_2EQ2UK-IBIS_IO.vif	189 KB	VIF File	2/1/2006 11:20 PM
IBIS_2EQ2UK-IBIS_OUTPUT.vif	181 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_C.vif	4 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCC.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS.vif	4 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS_ABS.vif	4 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS_DELAY.vif	4 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS_DIV.vif	6 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS_MAX.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS_MIN.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS_MULT.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS_PWL.vif	8 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCCS_SUM.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCL.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCR.vif	4 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS.vif	4 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS_ABS.vif	4 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS_DELAY.vif	4 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS_DIV.vif	6 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS_MAX.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS_MIN.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS_MULT.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS_PWL.vif	8 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CCVS_SUM.vif	5 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CECCS_PWL.vif	25 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_CECVS_PWL.vif	25 KB	VIF File	2/1/2006 11:20 PM
IDEAL-IBIS_I.vif	3 KB	VIF File	2/1/2006 11:20 PM

The resistor example - code


SMASH 5.6.0
File Edit View Design Simulate Waveforms Tools Windows Help
C:\Dolphin\Macro_Lib.VHD\IBIS_R_test.nsx
C:\Dolphin\Macro_Lib.VHD\IBIS_R_test.pat

C:\Dolphin\Macro_Lib.VHD\IBIS_R_test.nsx

```
>>> SPICE
*=======================================================================
Vpls  Pls  0  PULSE  ( 0.0  1.0  1.0ns  1.0ns  1.0ns  4.0ns  10.0ns )
*
R1  Pls     VHDL_p  R= 100
X1  VHDL_p  0       IBIS_R_VHDL(Simple_test)
*
R2  Pls   RR  R= 100
R3  RR    0   R= 100
*
*=======================================================================
>>> VHDL
--======================================================================
library IEEE, MacroLib;
use IEEE.ELECTRICAL_SYSTEMS.all;

entity IBIS_R_VHDL is
    port (terminal  Node_p,  Node_n  : electrical);
end entity IBIS_R_VHDL;

architecture Simple_test of IBIS_R_VHDL is

begin

   IBIS_R1 : entity MacroLib.IBIS_R(IDEAL)
      generic map ( Rval   => 50.0,
                    Scale =>  2.0 )
      port map ( P => Node_p,
                 N => Node_n );

end architecture Simple_test;
--======================================================================
```

macro
model
netlist

library call

parameters

nodes

C:\Dolphin\Macro_Lib.VHD\IBIS_R_test.pat

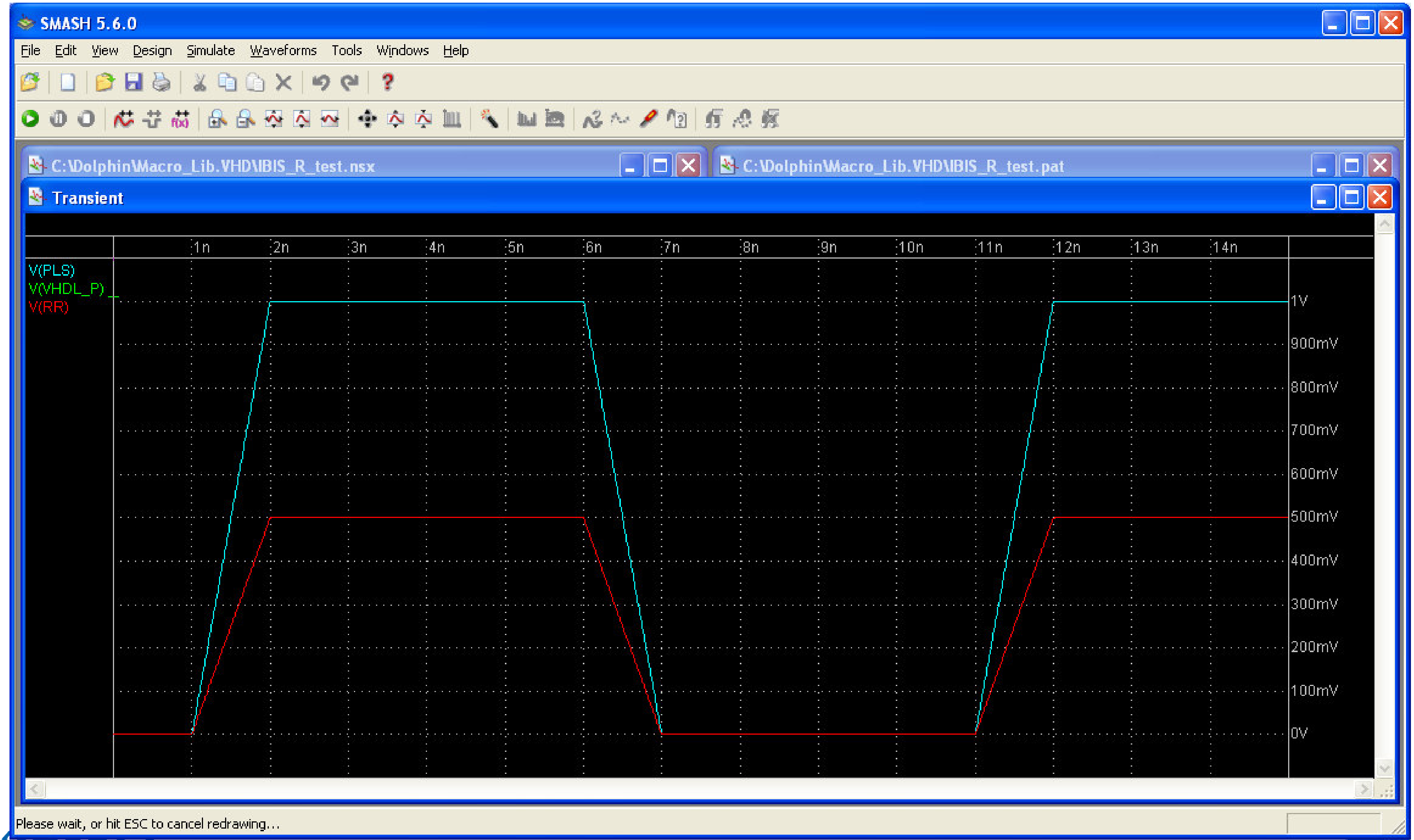
```
.VHDL SET KIND=AMS
*
.VHDL COMPILE LIBRARY=MacroLib SOURCE=.\Macro_lib\MacroLib_functions.vhd
.VHDL ADD LIBRARY=MacroLib     REFLIB=MacroLib
*
.VHDL COMPILE LIBRARY=MacroLib SOURCE=.\Macro_lib\IBIS_macro_library.vhd
.VHDL ADD LIBRARY=WORK         REFLIB=MacroLib
*
.Tran 1ps 15ns 0s noise=no noisestep=10ns traceBreak=yes
.Eps 1u 100m 100n
.Tolerance DEFAULT_TOLERANCE 1u
.H 1fs 1fs 10ps 125m 2
.Method TRAP
*
.Trace  Tran   V(Pls) V(VHDL_p) V(RR) Min=-1.0000000E+000 Max=3.0000000E+(
```

control statements

Load completed.

Ln 1, Col 0

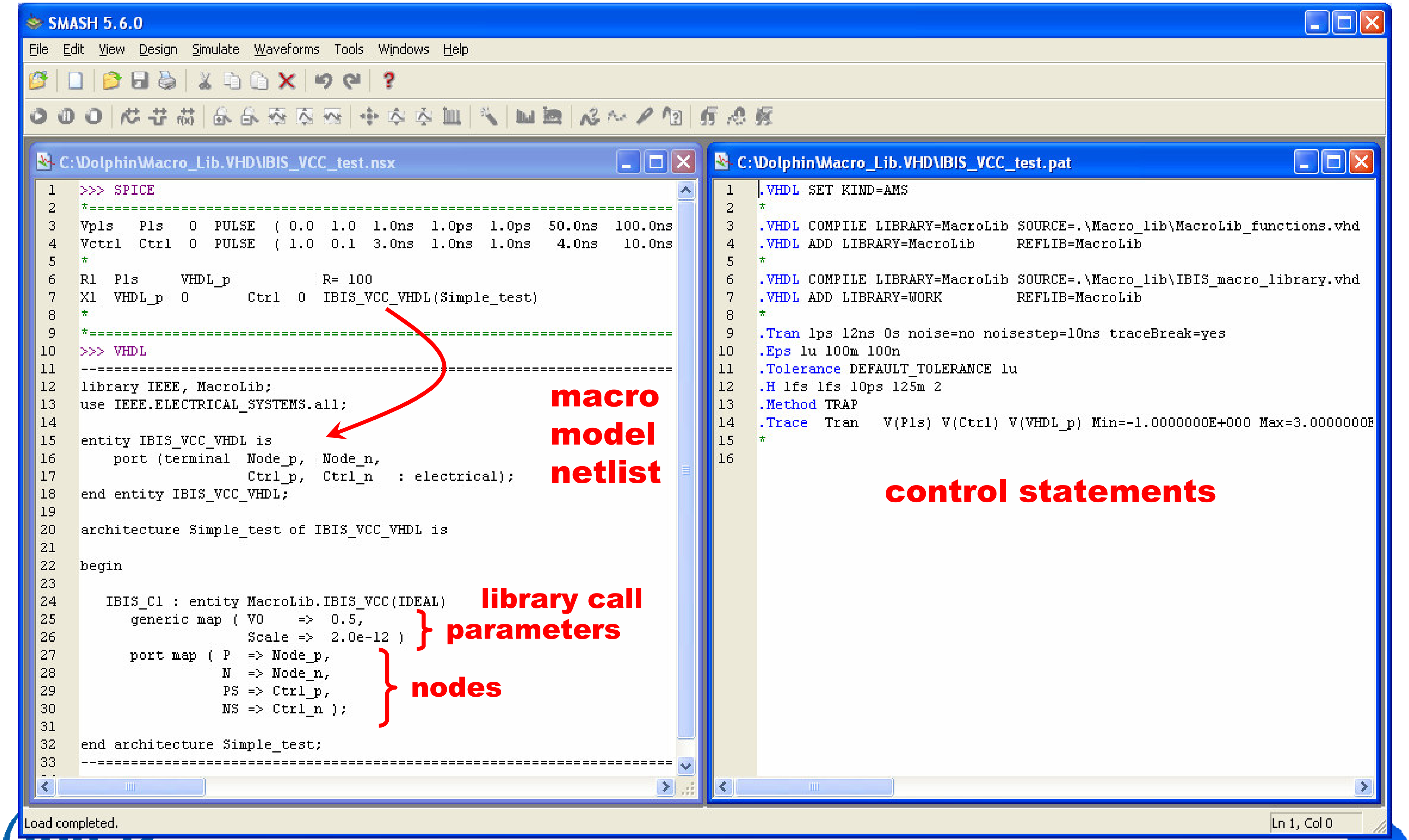
The resistor example - waveforms


SMASH 5.6.0
File Edit View Design Simulate Waveforms Tools Windows Help
C:\Dolphin\Macro_Lib.VHD\IBIS_R_test.nsx
C:\Dolphin\Macro_Lib.VHD\IBIS_R_test.pat
Transient
1n
2n
3n
4n
5n
6n
7n
8n
9n
10n
11n
12n
13n
14n
V(PLS)
V(VHDL_P)
V(RR)
1V
900mV
800mV
700mV
600mV
500mV
400mV
300mV
200mV
100mV
0V

Please wait, or hit ESC to cancel redrawing...

*Other brands and names are the property of their respective owners

The VCC example - code


SMASH 5.6.0
File Edit View Design Simulate Waveforms Tools Windows Help
C:\Dolphin\Macro_Lib.VHD\IBIS_VCC_test.nsx
C:\Dolphin\Macro_Lib.VHD\IBIS_VCC_test.pat
Load completed.
Ln 1, Col 0

C:\Dolphin\Macro_Lib.VHD\IBIS_VCC_test.nsx

```
>>> SPICE
*==========================================================================
Vpls   Pls   0  PULSE  ( 0.0  1.0  1.0ns  1.0ps  1.0ps  50.0ns  100.0ns
Vctrl  Ctrl  0  PULSE  ( 1.0  0.1  3.0ns  1.0ns  1.0ns   4.0ns   10.0ns
*
R1  Pls    VHDL_p          R= 100
X1  VHDL_p  0       Ctrl  0  IBIS_VCC_VHDL(Simple_test)
*
*==========================================================================
>>> VHDL
--=========================================================================
library IEEE, MacroLib;
use IEEE.ELECTRICAL_SYSTEMS.all;

entity IBIS_VCC_VHDL is
    port (terminal  Node_p,  Node_n,
                    Ctrl_p,  Ctrl_n   : electrical);
end entity IBIS_VCC_VHDL;

architecture Simple_test of IBIS_VCC_VHDL is

begin

   IBIS_C1 : entity MacroLib.IBIS_VCC(IDEAL)
      generic map ( V0    =>  0.5,
                    Scale =>  2.0e-12 )
      port map ( P   => Node_p,
                 N   => Node_n,
                 PS  => Ctrl_p,
                 NS  => Ctrl_n );

end architecture Simple_test;
--=========================================================================
```

macro model netlist

library call

parameters

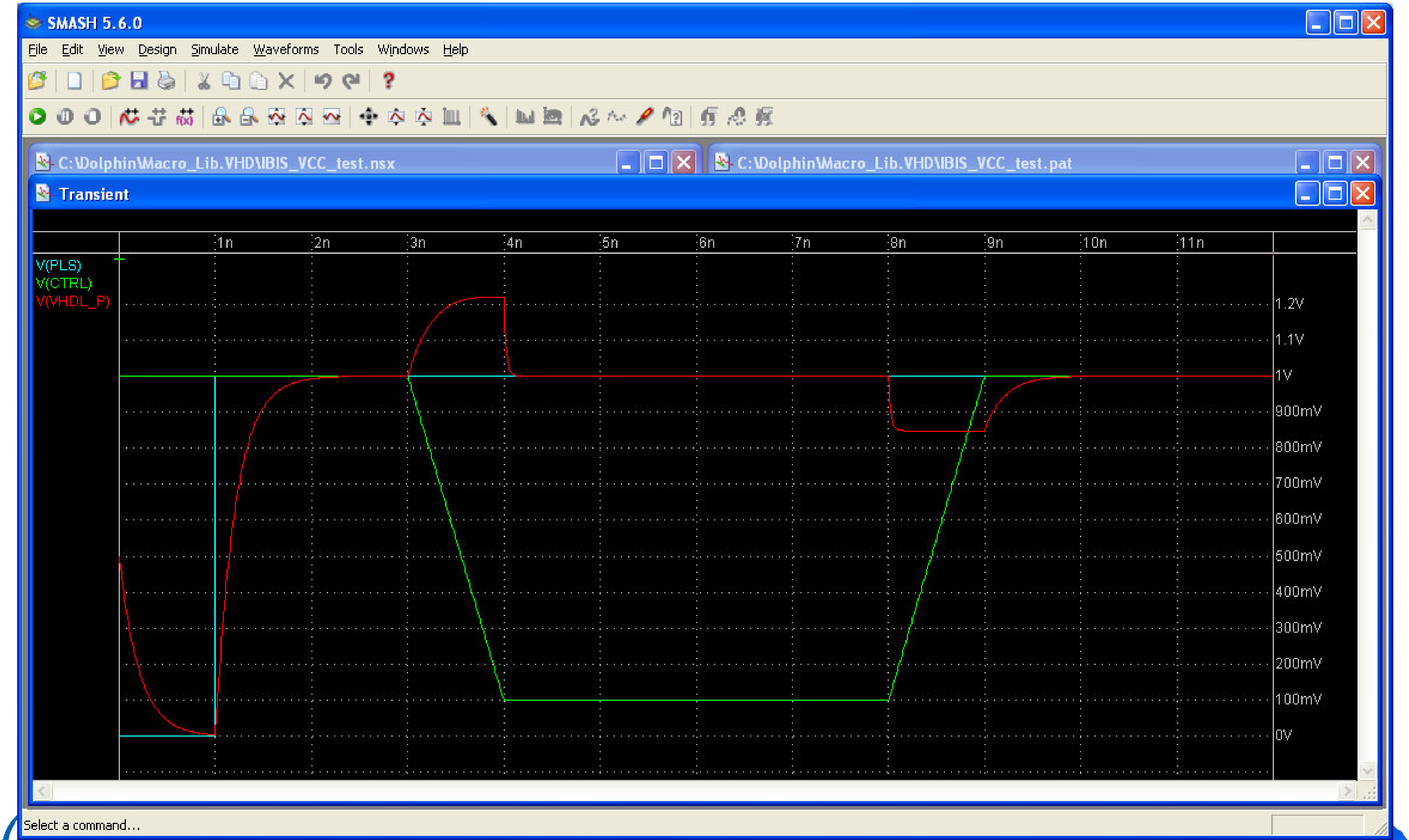
nodes

C:\Dolphin\Macro_Lib.VHD\IBIS_VCC_test.pat

```
.VHDL SET KIND=AMS
*
.VHDL COMPILE LIBRARY=MacroLib SOURCE=.\Macro_lib\MacroLib_functions.vhd
.VHDL ADD LIBRARY=MacroLib     REFLIB=MacroLib
*
.VHDL COMPILE LIBRARY=MacroLib SOURCE=.\Macro_lib\IBIS_macro_library.vhd
.VHDL ADD LIBRARY=WORK         REFLIB=MacroLib
*
.Tran 1ps 12ns 0s noise=no noisestep=10ns traceBreak=yes
.Eps 1u 100m 100n
.Tolerance DEFAULT_TOLERANCE 1u
.H 1fs 1fs 10ps 125m 2
.Method TRAP
.Trace  Tran   V(Pls) V(Ctrl) V(VHDL_p) Min=-1.0000000E+000 Max=3.0000000E
*
```

control statements

The VCC example - waveforms



SMASH 5.6.0
File Edit View Design Simulate Waveforms Tools Windows Help
C:\Dolphin\Macro_Lib.VHD\IBIS_VCC_test.nsx
C:\Dolphin\Macro_Lib.VHD\IBIS_VCC_test.pat
Transient
1n
2n
3n
4n
5n
6n
7n
8n
9n
10n
11n
V(PLS)
V(CTRL)
V(VHDL_P)
1.2V
1.1V
1V
900mV
800mV
700mV
600mV
500mV
400mV
300mV
200mV
100mV
0V
Select a command...

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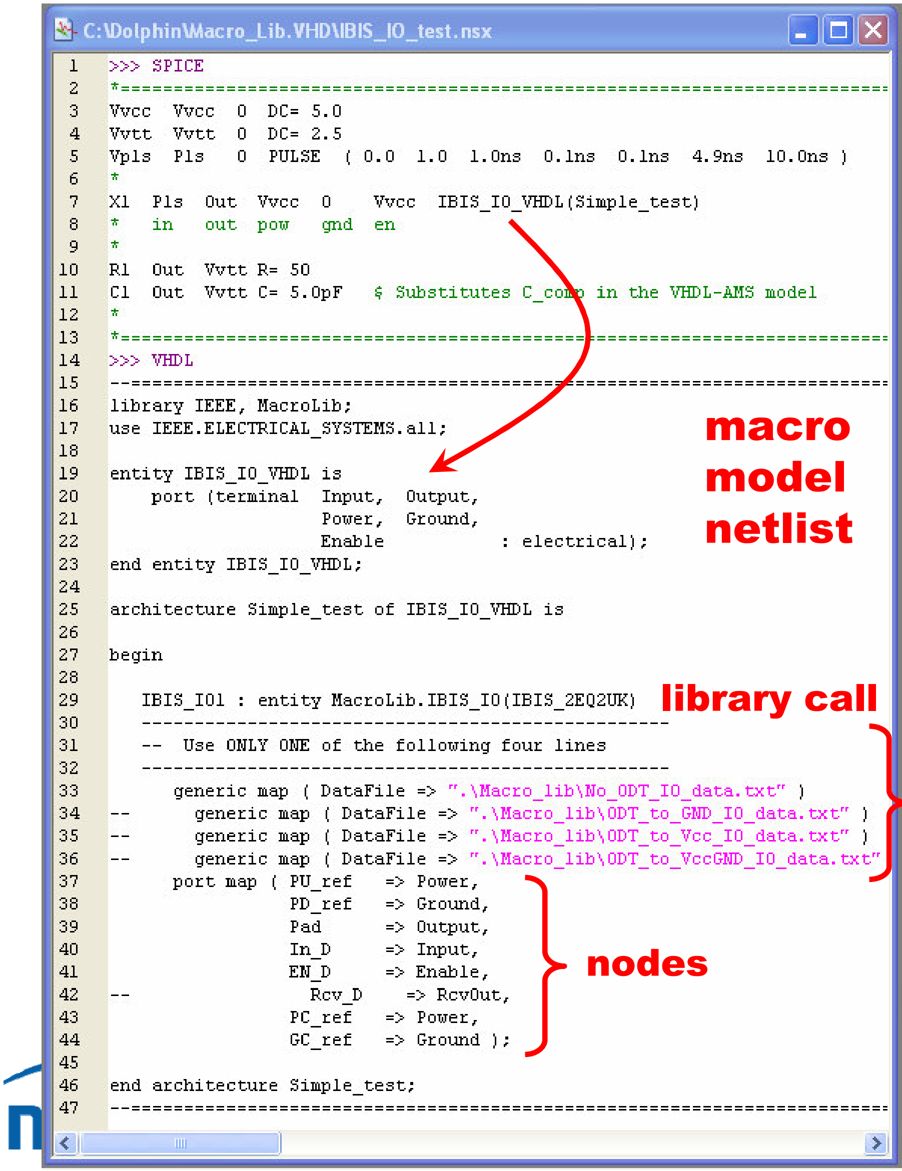
IBIS_IO buffer example - code



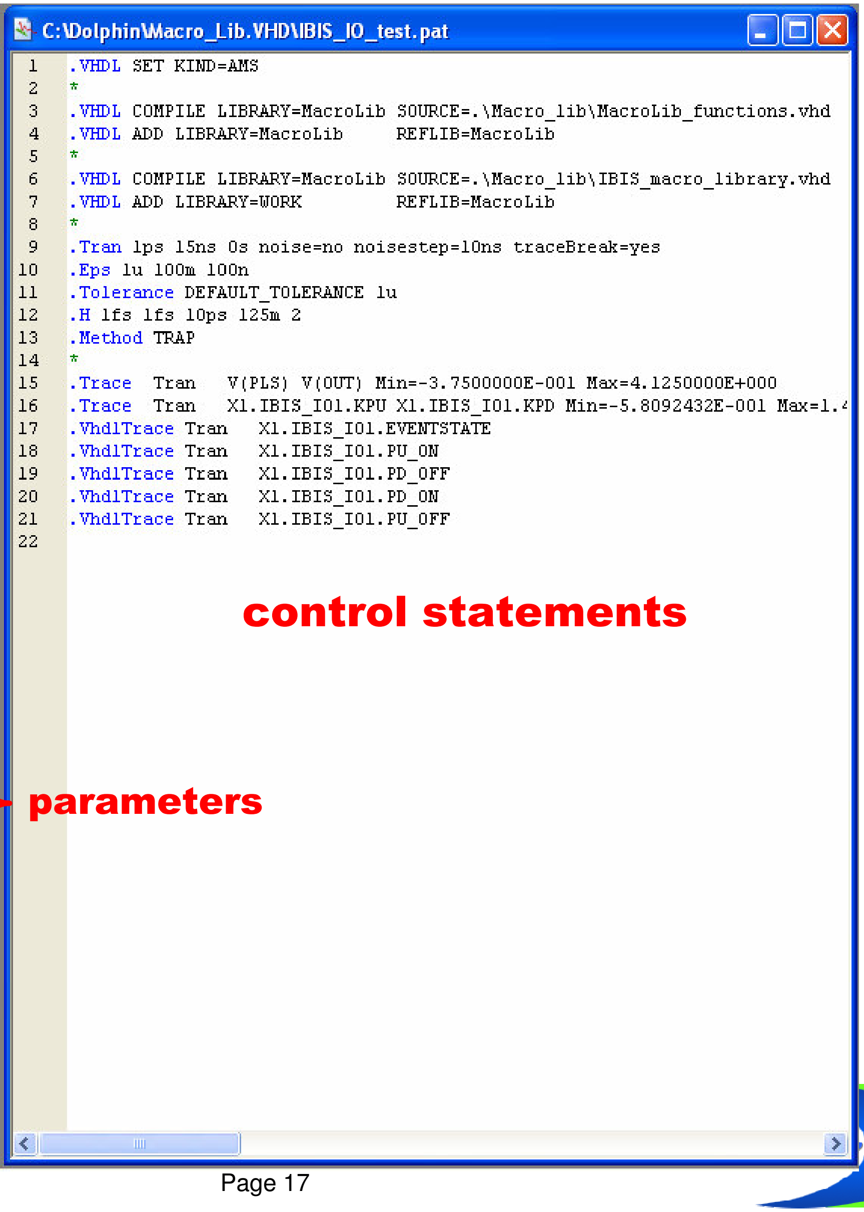
```
>>> SPICE
*=========================================================================
Vvcc  Vvcc  0  DC= 5.0
Vvtt  Vvtt  0  DC= 2.5
Vpls  Pls   0  PULSE  ( 0.0  1.0  1.0ns  0.1ns  0.1ns  4.9ns  10.0ns )
*
X1  Pls  Out  Vvcc  0    Vvcc  IBIS_IO_VHDL(Simple_test)
*   in   out  pow   gnd  en
*
R1  Out  Vvtt R= 50
C1  Out  Vvtt C= 5.0pF   $ Substitutes C_comp in the VHDL-AMS model
*
*=========================================================================
>>> VHDL
--========================================================================
library IEEE, MacroLib;
use IEEE.ELECTRICAL_SYSTEMS.all;

entity IBIS_IO_VHDL is
    port (terminal  Input,  Output,
                    Power,  Ground,
                    Enable           : electrical);
end entity IBIS_IO_VHDL;

architecture Simple_test of IBIS_IO_VHDL is

begin

   IBIS_IO1 : entity MacroLib.IBIS_IO(IBIS_2EQ2UK)
   --------------------------------------------------
   --  Use ONLY ONE of the following four lines
   --------------------------------------------------
      generic map ( DataFile => ".\Macro_lib\No_ODT_IO_data.txt" )
--      generic map ( DataFile => ".\Macro_lib\ODT_to_GND_IO_data.txt" )
--      generic map ( DataFile => ".\Macro_lib\ODT_to_Vcc_IO_data.txt" )
--      generic map ( DataFile => ".\Macro_lib\ODT_to_VccGND_IO_data.txt"
      port map ( PU_ref    => Power,
                 PD_ref    => Ground,
                 Pad       => Output,
                 In_D      => Input,
                 EN_D      => Enable,
--                 Rcv_D     => RcvOut,
                 PC_ref    => Power,
                 GC_ref    => Ground );

end architecture Simple_test;
--========================================================================
```

macro model netlist

library call

parameters

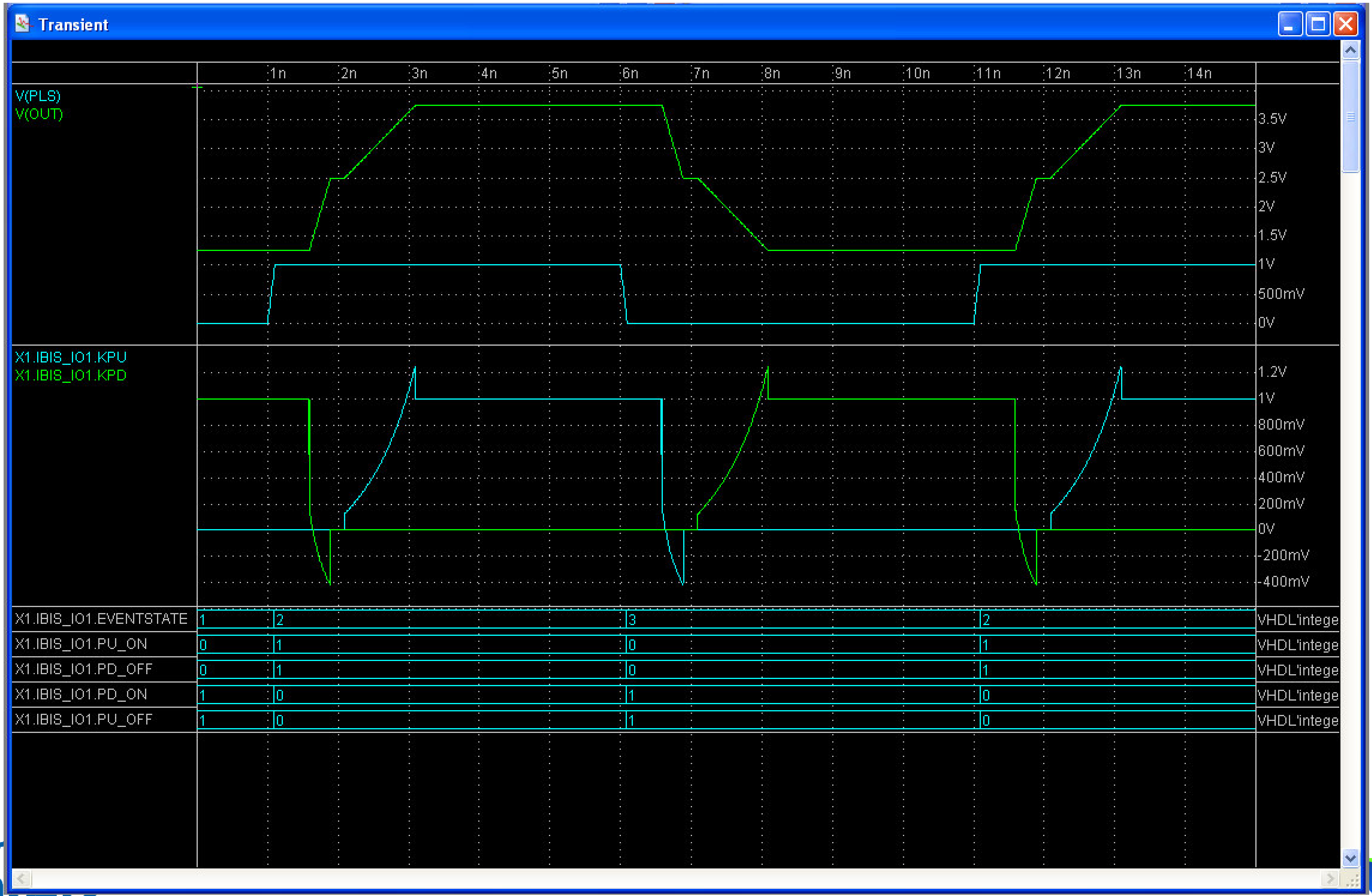
nodes



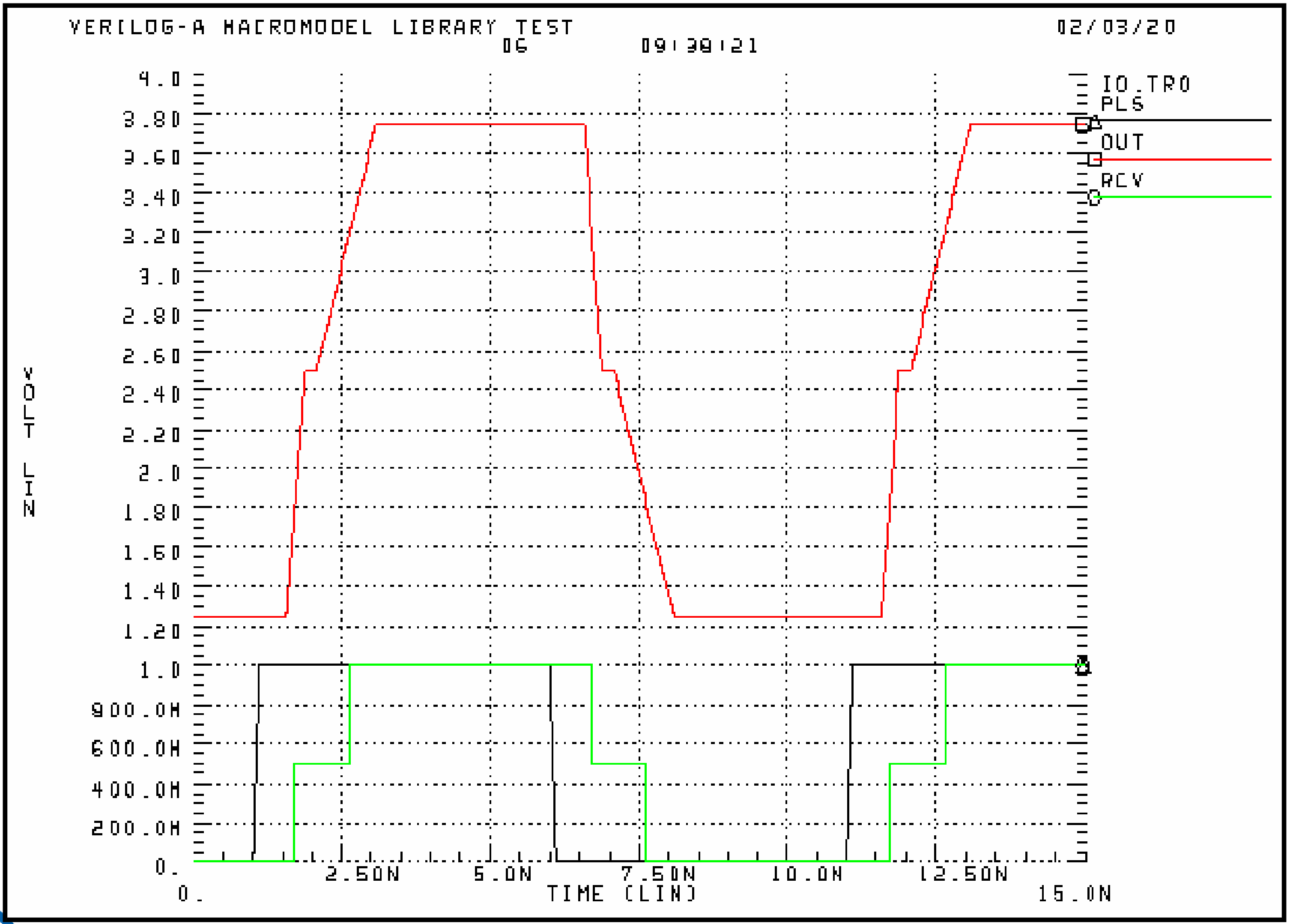
```
.VHDL SET KIND=AMS
*
.VHDL COMPILE LIBRARY=MacroLib SOURCE=.\Macro_lib\MacroLib_functions.vhd
.VHDL ADD LIBRARY=MacroLib     REFLIB=MacroLib
*
.VHDL COMPILE LIBRARY=MacroLib SOURCE=.\Macro_lib\IBIS_macro_library.vhd
.VHDL ADD LIBRARY=WORK         REFLIB=MacroLib
*
.Tran 1ps 15ns 0s noise=no noisestep=10ns traceBreak=yes
.Eps 1u 100m 100n
.Tolerance DEFAULT_TOLERANCE 1u
.H 1fs 1fs 10ps 125m 2
.Method TRAP
*
.Trace  Tran   V(PLS) V(OUT) Min=-3.7500000E-001 Max=4.1250000E+000
.Trace  Tran   X1.IBIS_IO1.KPU X1.IBIS_IO1.KPD Min=-5.8092432E-001 Max=1.4
.VhdlTrace Tran   X1.IBIS_IO1.EVENTSTATE
.VhdlTrace Tran   X1.IBIS_IO1.PU_ON
.VhdlTrace Tran   X1.IBIS_IO1.PD_OFF
.VhdlTrace Tran   X1.IBIS_IO1.PD_ON
.VhdlTrace Tran   X1.IBIS_IO1.PU_OFF
```

control statements

IBIS_IO buffer example - waveforms



Verilog-A(MS) waveforms of IBIS_IO



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Parameter data file format

```
----------------------------------
-- C_comp parameters
----------------------------------
C_comp
5.00e-12
kC_comp_pc
0.25
kC_comp_pu
0.25
kC_comp_pd
0.25
kC_comp_gc
0.25
----------------------------------
-- Vectors of the IV curve tables
----------------------------------
Ipc_data
0.08
0.00
0.00
0.00
Vpc_data
-5.00
-1.00
 5.00
10.00

Ipu_data
 0.10
 0.00
-0.10
-0.20
. . .
. . .
```

VHDL-A(MS)

```
`define IO_data \
\
.C_comp(5.0p), \
.kC_comp_pc(0.25), \
.kC_comp_pu(0.25), \
.kC_comp_pd(0.25), \
.kC_comp_gc(0.25), \
\
.IVpc_length(4), \
.Ipc_data({ 0.08,  0.00,  0.00,  0.00}), \
.Vpc_data({-5.00, -1.00,  5.00, 10.00}), \
.IVpu_length(4), \
.Ipu_data({ 0.10,  0.00, -0.10, -0.20}), \
.Vpu_data({-5.00,  0.00,  5.00, 10.00}), \
.IVpd_length(4), \
.Ipd_data({-0.10,  0.00,  0.10,  0.20}), \
.Vpd_data({-5.00,  0.00,  5.00, 10.00}), \
.IVgc_length(4), \
.Igc_data({-0.08,  0.00,  0.00,  0.00}), \
.Vgc_data({-5.00, -1.00,  5.00, 10.00}), \
\
data({0.00,  0.50e-9,  0.80e-9,  3.00e-9})
. . .
. . .
```

Verilog-A(MS)

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Pre-emphasis buffer - block diagram

- A differential pre/de-emphasis buffer
  - a circuit netlist serves as the macro model, instantiating
    - four Verilog-A or VHDL-AMS IBIS I/O buffer models,
    - an inverter,
    - two ideal delays, and
    - eight current sources to scale the Boost buffer’s current

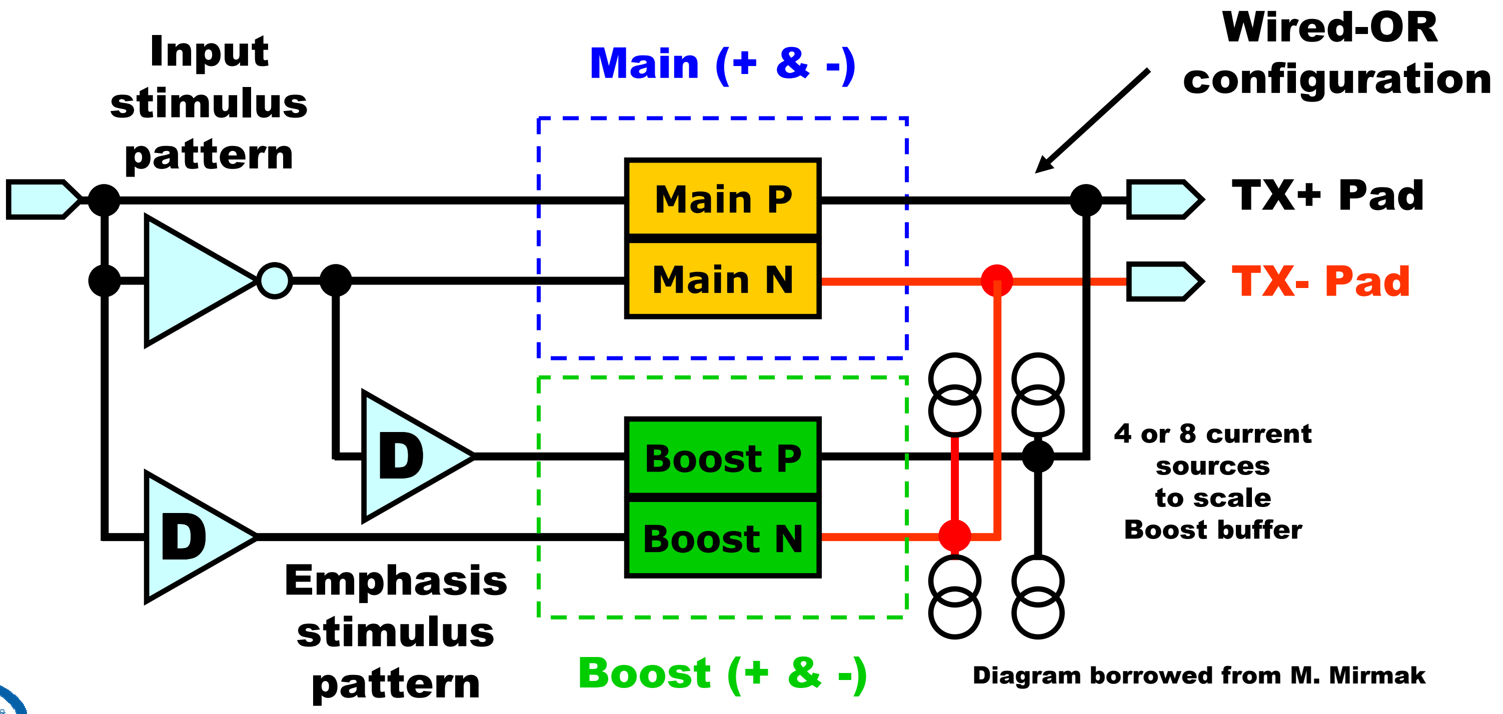

Diagram borrowed from M. Mirmak

*Other brands and names are the property of their respective owners

Pre-emphasis buffer - test bench

```
Test Verilog-A "Macro Model Template" in HSPICE
***********************************************************************
.TRAN 5.0ps 150.0ns
.OPTIONS POST=1 POST_VERSION=9007 PROBE
.hdl ".\PreDeMacro.va"
***********************************************************************
.PROBE TRAN
+ Pls  = V(Pls)
+ OutP = V(Out_p)
+ OutN = V(Out_n)
***********************************************************************
Vvcc    Vcc   0  DC= 5.0
* This source represents a 111000111000 pattern
Vpls    Pls   0  PULSE  (1.0  0.0  1.0ns  1.0ps  1.0ps  30.0ns  60.0ns)
***********************************************************************
X1      Pls   Out_p  Out_n  Vcc  Vcc  0    0    Vcc   PreDeMacro
*       In    Out_p  Out_n  PC   PU   PD   GC   En
*
Rld1  Out_p  Vtt  R= 50.0
Rld2  Out_n  Vtt  R= 50.0
***********************************************************************
.END
***********************************************************************
```

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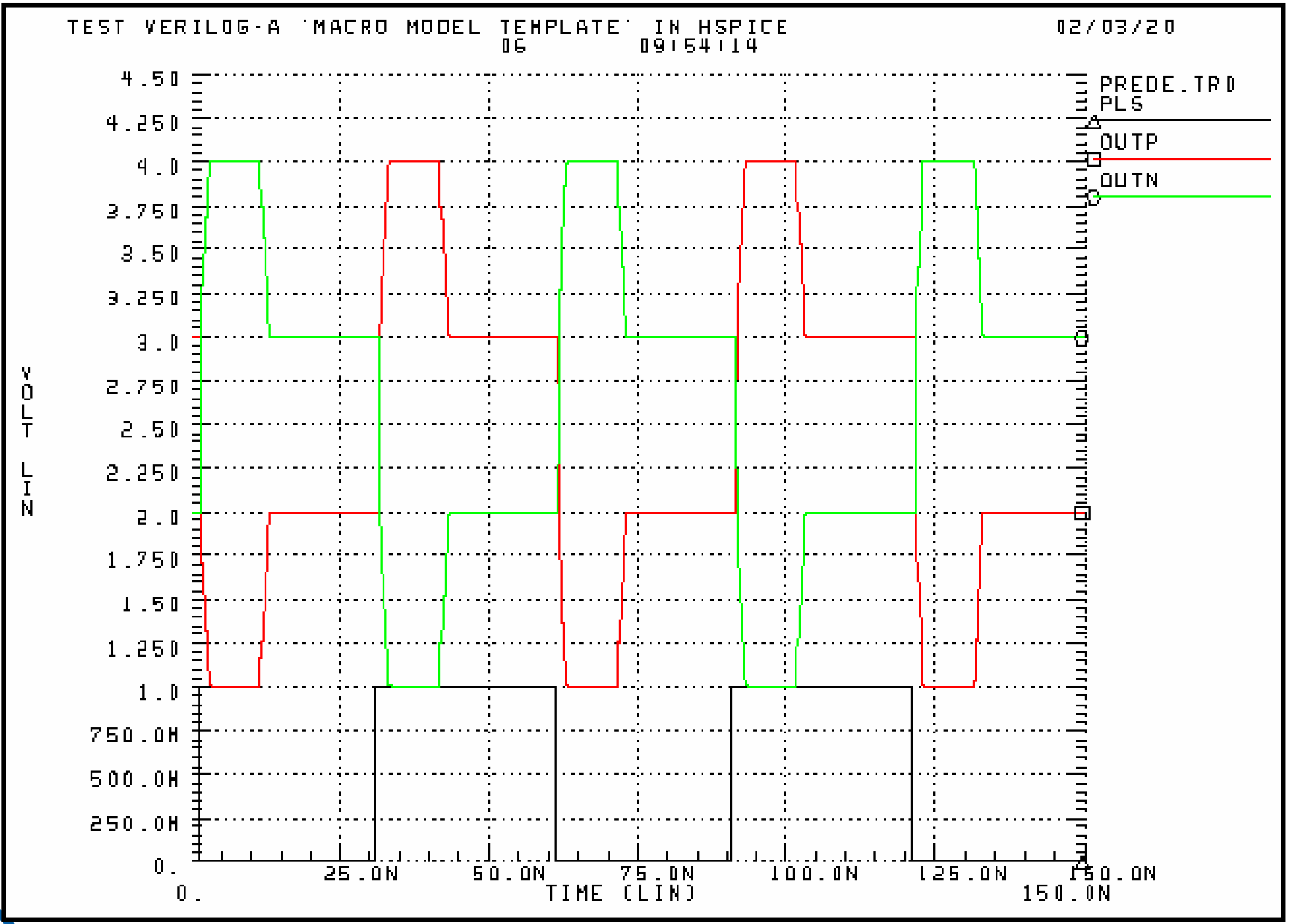
Pre-emphasis buffer - macro model

```
`include "constants.vams"
`include "disciplines.vams"
`include ".\AMS_files\IBIS_macro_library.va"
//-----------------------------------------------------------------------------
module PreDeMacro (InD, IOp, IOn, PCref,  PUref,  PDref,  GCref,  EnD);
  input      InD, EnD;
  electrical InD, EnD;
  inout      IOp, IOn, PCref, PUref, PDref, GCref;
  electrical IOp, IOn, PCref, PUref, PDref, GCref;

  electrical InNM,     InPB,     InNB,     Dref;
  electrical PUrefPB,  PDrefPB,  PCrefPB,  GCrefPB;
  electrical PUrefNB,  PDrefNB,  PCrefNB,  GCrefNB;
  electrical RcvPM,    RcvNM,    RcvPB,    RcvNB;

  parameter  real  BitDelay   = 10.0e-9;
  parameter  real  ScaleBoost = -0.5;
//-----------------------------------------------------------------------------
`include "No_ODT_IO_data.dat"

  IBIS_IO  #(`IO_data) PosM  (PUref,   PDref,   IOp, InD,  EnD, RcvPM, PCref,   GCref);
  IBIS_IO  #(`IO_data) NegM  (PUref,   PDref,   IOn, InNM, EnD, RcvNM, PCref,   GCref);
  IBIS_IO  #(`IO_data) PosB  (PUrefPB, PDrefPB, IOp, InPB, EnD, RcvPB, PCrefPB, GCrefPB);
  IBIS_IO  #(`IO_data) NegB  (PUrefNB, PDrefNB, IOn, InNB, EnD, RcvNB, PCrefNB, GCrefNB);
//- - - - - - - - - - - - - - PUref,   PDref,   IO,  In,   En,  Rcv,   PCref,   GCref

  IBIS_V           #(.Vdc(1.0))     Dig1  (Dref, PDref);
  IBIS_VCVS                         Inv1  (Dref, InNM,  InD,  PDref);
  IBIS_VCVS_DELAY  #(.TD(BitDelay)) Dly1  (InNB, PDref, InD,  PDref);
  IBIS_VCVS_DELAY  #(.TD(BitDelay)) Dly2  (InPB, PDref, InNM, PDref);

  IBIS_CCCS  #(.Scale(ScaleBoost))  IpcP  (PCref, IOp, PCref, PCrefPB);
  IBIS_CCCS  #(.Scale(ScaleBoost))  IpuP  (PUref, IOp, PUref, PUrefPB);
  IBIS_CCCS  #(.Scale(ScaleBoost))  IpdP  (PDref, IOp, PDref, PDrefPB);
  IBIS_CCCS  #(.Scale(ScaleBoost))  IgcP  (GCref, IOp, GCref, GCrefPB);
  IBIS_CCCS  #(.Scale(ScaleBoost))  IpcN  (PCref, IOn, PCref, PCrefNB);
  IBIS_CCCS  #(.Scale(ScaleBoost))  IpuN  (PUref, IOn, PUref, PUrefNB);
  IBIS_CCCS  #(.Scale(ScaleBoost))  IpdN  (PDref, IOn, PDref, PDrefNB);
  IBIS_CCCS  #(.Scale(ScaleBoost))  IgcN  (GCref, IOn, GCref, GCrefNB);
//-----------------------------------------------------------------------------
endmodule
```

Pre-emphasis buffer - waveforms



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Wrap up

- Links to the two test suites including the most current version of the macro model library

  http://www.eda.org/pub/ibis/macromodel_wip/Macro_Lib_VA_HSPICE_2006_01_26.zip
  http://www.eda.org/pub/ibis/macromodel_wip/Macro_Lib_VHDL_SMASH_2006_02_01.zip

- Please try it out and provide feedback, that is the only way this effort can be made useful!
- Lots of capabilities and features could still be added to the library, but we need to know what is needed, and what is practical, etc…
- In case you need help to find SMASH…

  http://www.dolphin-integration.com/medal/smash/smash_download.html