Algorithmic Modeling BIRD Update
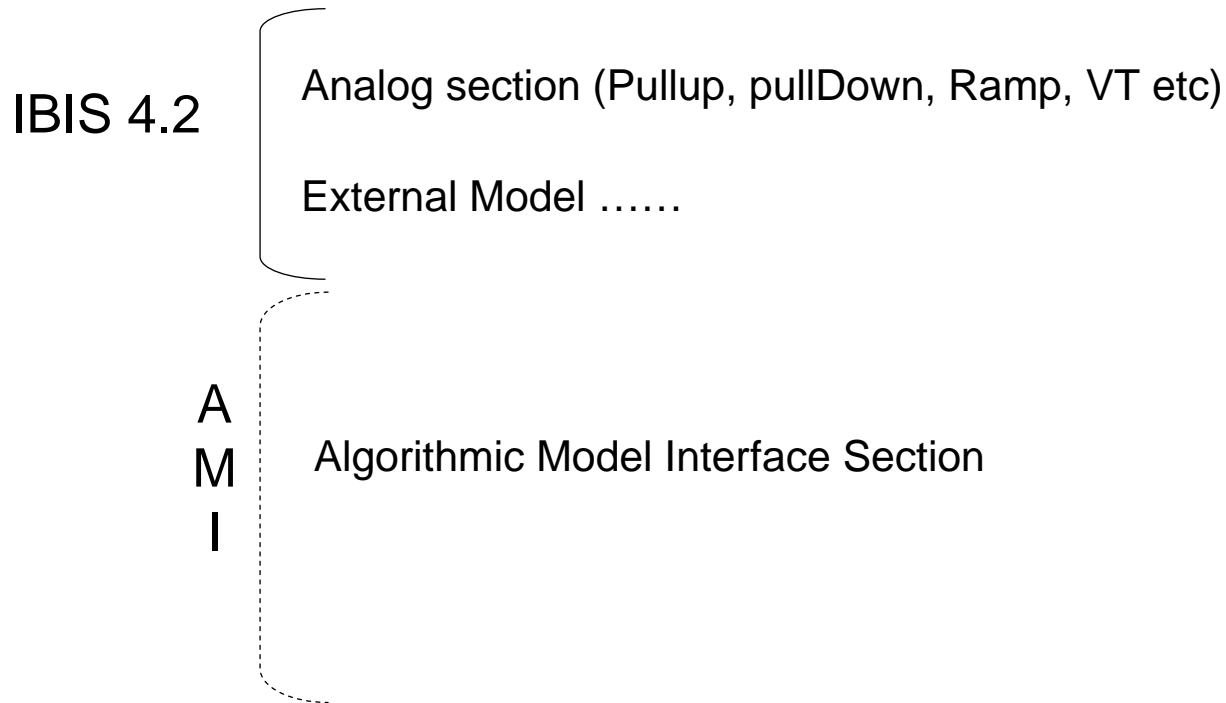# 6th March 2007

Cadence – SiSoft – Mentor

Algorithmic Modeling BIRD Update
EDA vendors Algorithmic Modeling summit

- Face to Face meeting: Cadence, SiSoft & Mentor at Cadence Chelmsford office Feb 27th and 28th
- Good progress made
  - (Lots) More work needed to finish writing the BIRD
- Updated Parameter types and Syntax
- Cadence, SiSoft, Mentor agreed to provide internal parameterized models for Tx and Rx
- Updated terminology proposed by SiSoft
- Updated Cadence and SiSoft documents for different sections
- Got on the same page for the most part

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Algorithmic Modeling BIRD Update
Proposed IBIS Model Structure changes - 1

IBIS 4.2

Analog section (Pullup, pullDown, Ramp, VT etc)

External Model ……

A
M
I

Algorithmic Model Interface Section

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Algorithmic Modeling BIRD Update
Proposed IBIS Model Structure changes - 2

IBIS 4.2

Analog section (Pullup, pullDown, Ramp, VT etc)

External Model ……

A
M
I

Algorithmic Model Interface Section

[Algorithmic Model]

Executable <exetype> <exename>

<Parameter declarations>

[End Algorithmic Model]

Where
<exetype>: exe or dll or internal
<exename>: exe or dll filename

- Parameter declarations will be discussed in future meetings in detail

- Parameters provide configurability of model and simulation for the systems user

- One new keyword: [Algorithmic Model]

- One new defined parameter: "Executable"

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Next Steps

- Update BIRD proposed by Cadence
  - Update documentation
  - Provide example simple Tx, Rx IBIS models
- Discuss changes with leading SERDES IP vendors
- Digest feedback from IP vendors, update docs if necessary
- Send out invitation to IC companies on IBIS Open Forum if they wish to review it with Cadence, SiSoft and Mentor
- Start reviewing updated BIRD in IBIS ATM – March 20th (tentative)
  - Assumes we have all our presentation and documentation ducks in a row

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