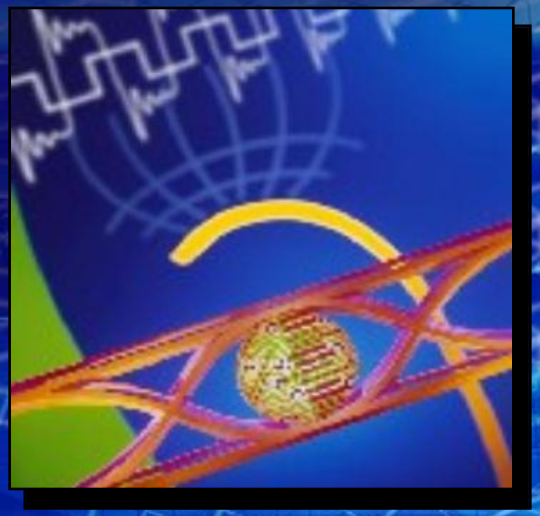
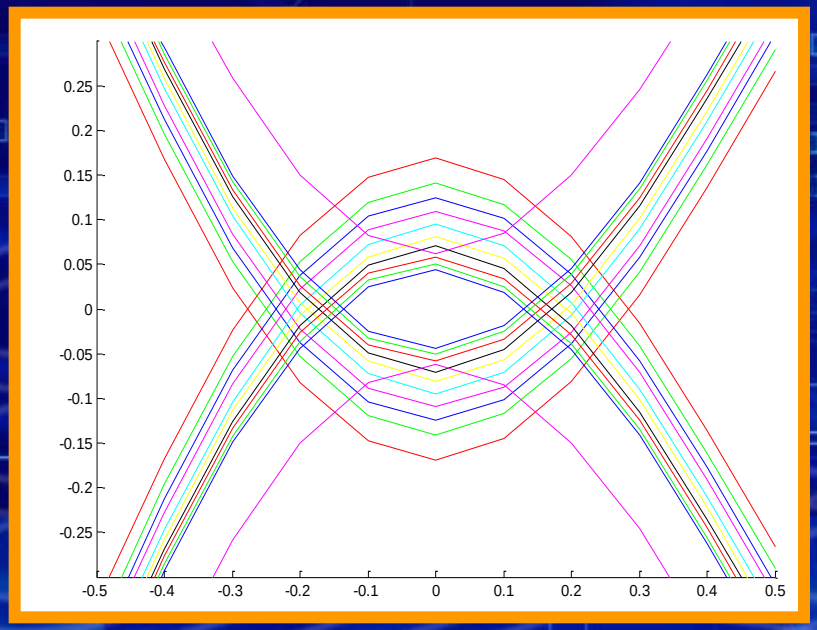
Package Modeling in IBIS



IBIS ATM Teleconference
July 24, 2012



Arpad Muranyi

Mentor Graphics®

Overview of BIRD 125

```
[Pin] signal_name  model_name
 A1   Vcc1         POWER
 B2   DQ_signal    DQ_model
 C3   GND1         GND
|
[Package Model]  A_pkg_model
|…
[Model] DQ_model
Model_type I/O
|…
[Node Declarations]
Pad_2
```

```
[Define Package Model]  A_pkg_model
[Manufacturer]          Noname Company, Inc.
[OEM]                   Noname Company, Inc.
[Description]           Illustration model
[Number Of Pins]  3
|
[Pin Numbers]
 A1  DiePortName = IDP_A1
 B2  DiePortName = Pad_2
 C3  DiePortName = IDP_C3
|…
[Package Circuit]
Language IBIS-ISS
|…
```

- The new 2nd column of [Pin Numbers] declares
  - Implicit on-die nodes (pads)
  - Explicit on-die nodes (pads)
- IBIS-ISS models can be placed between pins and pads
- This supports arbitrary mapping between pins and pads

A simple package model with BIRD 125

Legacy IBIS file:

```
|------------------------------------------------------------
| Example of an IBIS model using an IBIS-ISS package model
|------------------------------------------------------------
|
[Pin] signal_name  model_name
  1   …            …
  2   …            …
  3   …            …
  4   …            …
  5   Channel_1P   ISS_Diff_Tx
  6   Channel_1N   ISS_Diff_Tx
  7   Channel_2P   ISS_Diff_Tx
  8   Channel_2N   ISS_Diff_Tx
  9   …            …
 10   …            …
|
[Package Model]  A_4_pin_pkg_model
|…
|…
```

Matched by name

PackageModel.cir file:

```
**************************************************************
.SUBCKT  S_pkg  P1  P2  P3  P4  P5  P6  P7  P8
+ TSFile="TouchstoneFileName.s8p"

Sdriver  P1  P2  P3  P4  P5  P6  P7  P8
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]

**************************************************************
.ends
```

Matched by position

IBIS .pkg file:

```
|------------------------------------------------------------
| This example implements a package model using an IBIS-ISS
| subcircuit.
|------------------------------------------------------------
|
[Define Package Model]  A_4_pin_pkg_model
[Manufacturer]          Noname Company, Inc.
[OEM]                   Another Noname Package Company, Inc.
[Description]           4-pin
[Number Of Pins]  4
|
[Pin Numbers]
  5   DiePortName = IDP_5
  6   DiePortName = IDP_6
  7   DiePortName = IDP_7
  8   DiePortName = IDP_8
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  PackageModel.cir  S_pkg
|
| Parameters List of parameters
Parameters  TSFile = "My_TstoneFile.s8p"
|
| Ports are in same order as defined in SPICE
Ports  5      6      7      8
Ports  IDP_8  IDP_7  IDP_6  IDP_5
|
[End Package Circuit]
[End Package Model]
```

Declaration of Implicit die ports

Matched by name

Figure 12 (pg. 136) in IBIS v5.0

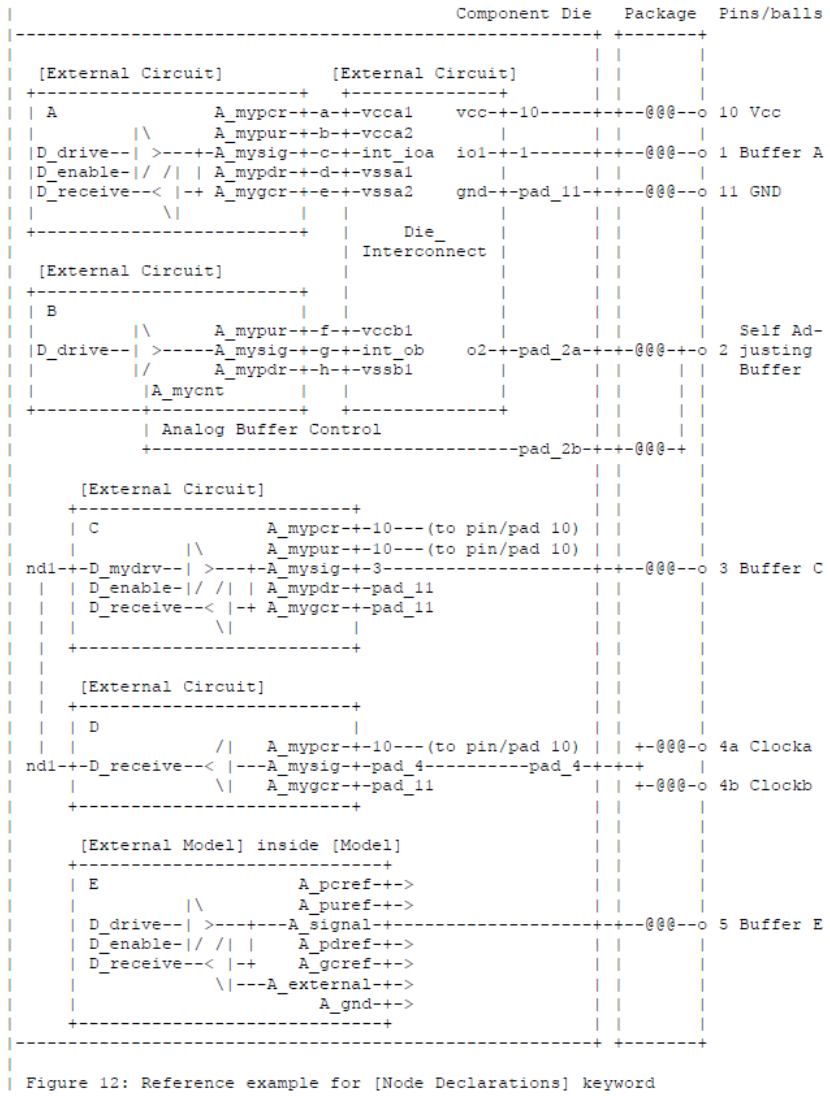


Figure 12 implemented with BIRD 125

Legacy IBIS file:

```
|-------------------------------------------------------------
| Example of an IBIS model using an IBIS-ISS package model.
| This example implements a package call for the drawing in
| Fig. 12 on pg. 136 of the IBIS v5.0 specification.
|-------------------------------------------------------------
|
[Pin] signal_name  model_name
 10   Vcc          POWER
  1   A0           CIRCUITCALL
 11   GND          GND
  2   CAS0         CIRCUITCALL
  3   A1           CIRCUITCALL
  4a  Clk_A        CIRCUITCALL
  4b  Clk_B        CIRCUITCALL
  5   A2           Buffer_E
|
[Node Declarations]
| Die nodes:
a  b  c  d  e  f  g  h  nd1    | List of die nodes
|
| Die pads:
pad_2a  pad_2b  pad_4  pad_11  | List of die pads
|
[End Node Declarations]
|
[Package Model]  QS-SMT-cer-8-pin-pkgs
|…
```

PackageModel.cir file:

```
**************************************************************
.SUBCKT  S_pkg  P1  P2   P3   P4   P5   P6   P7   P8
+               P9  P10  P11  P12  P13  P14  P15  P16
+ TSFile="TouchstoneFileName.s16p"

Sdriver  P1  P2   P3   P4   P5   P6   P7   P8
+        P9  P10  P11  P12  P13  P14  P15  P16
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]

**************************************************************
.ends
```

IBIS .pkg file:

```
|-------------------------------------------------------------
| This example implements a package model using an IBIS-ISS
| subcircuit for the drawing in Fig. 12 on pg. 136 of the
| IBIS v5.0 specification.
|-------------------------------------------------------------
|
[Define Package Model]  QS-SMT-cer-8-pin-pkgs
[Manufacturer]          Quality Semiconductors Ltd.
[OEM]                   Acme Package Co.
[Description]           8-Pin ceramic SMT package
[Number Of Pins]  8
|
[Pin Numbers]
 10   DiePort = IDP_10
  1   DiePort = IDP_1
 11   DiePort = pad_11
  2   DiePort = pad_2a
  2   DiePort = pad_2b
  3   DiePort = IDP_3
  4a  DiePort = pad_4
  4b  DiePort = pad_4
  5   DiePort = IDP_5
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  PackageModel.cir  S_pkg
|
| Parameters List of parameters
Parameters  TSFile = "My_TstoneFile.s16p"
|
| Ports are in same order as defined in SPICE
Ports  10  1  11  2  3  4a  4b  5
Ports  IDP_5  pad_4  IDP_3  pad_2b
Ports  pad_2a  pad_11  IDP_1  IDP_10
|
[End Package Circuit]
[End Package Model]
```

Matched by name

Implicit die ports (in blue)

Explicit die ports (in red) are declared under [Node Declarations]

Matched by position

Matched by name

A missing detail in the previous example for Figure 12

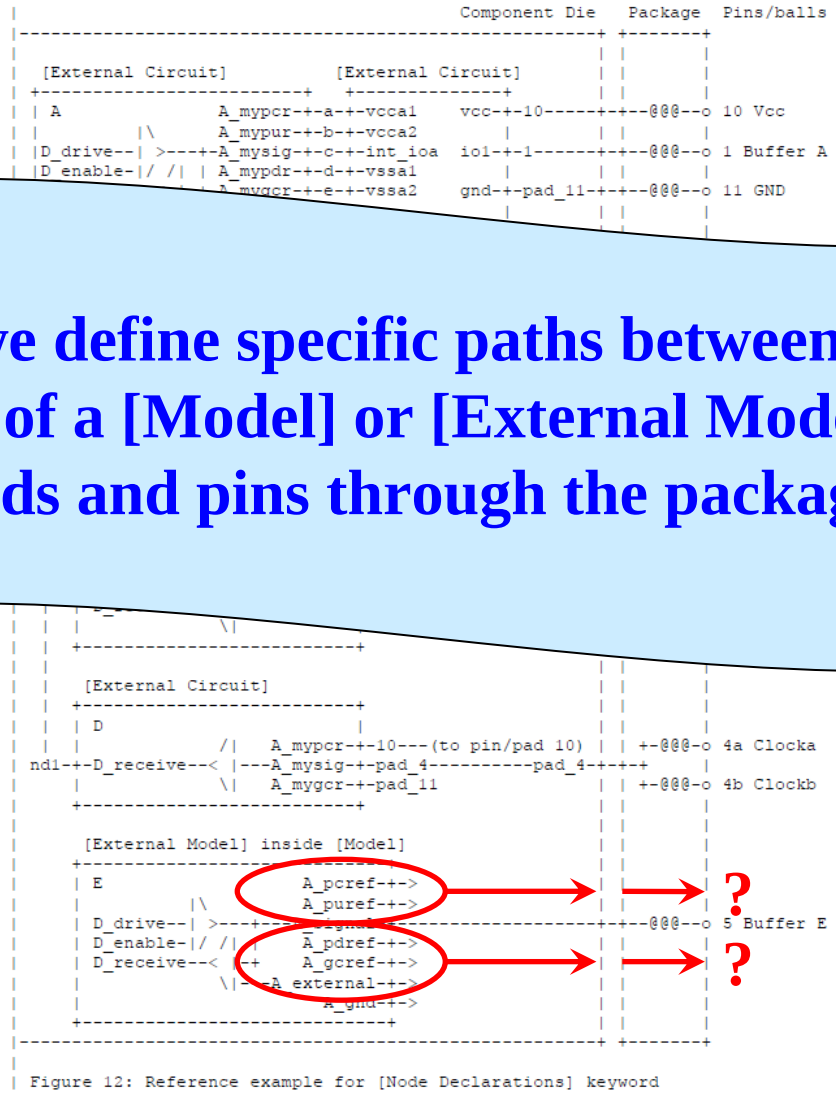
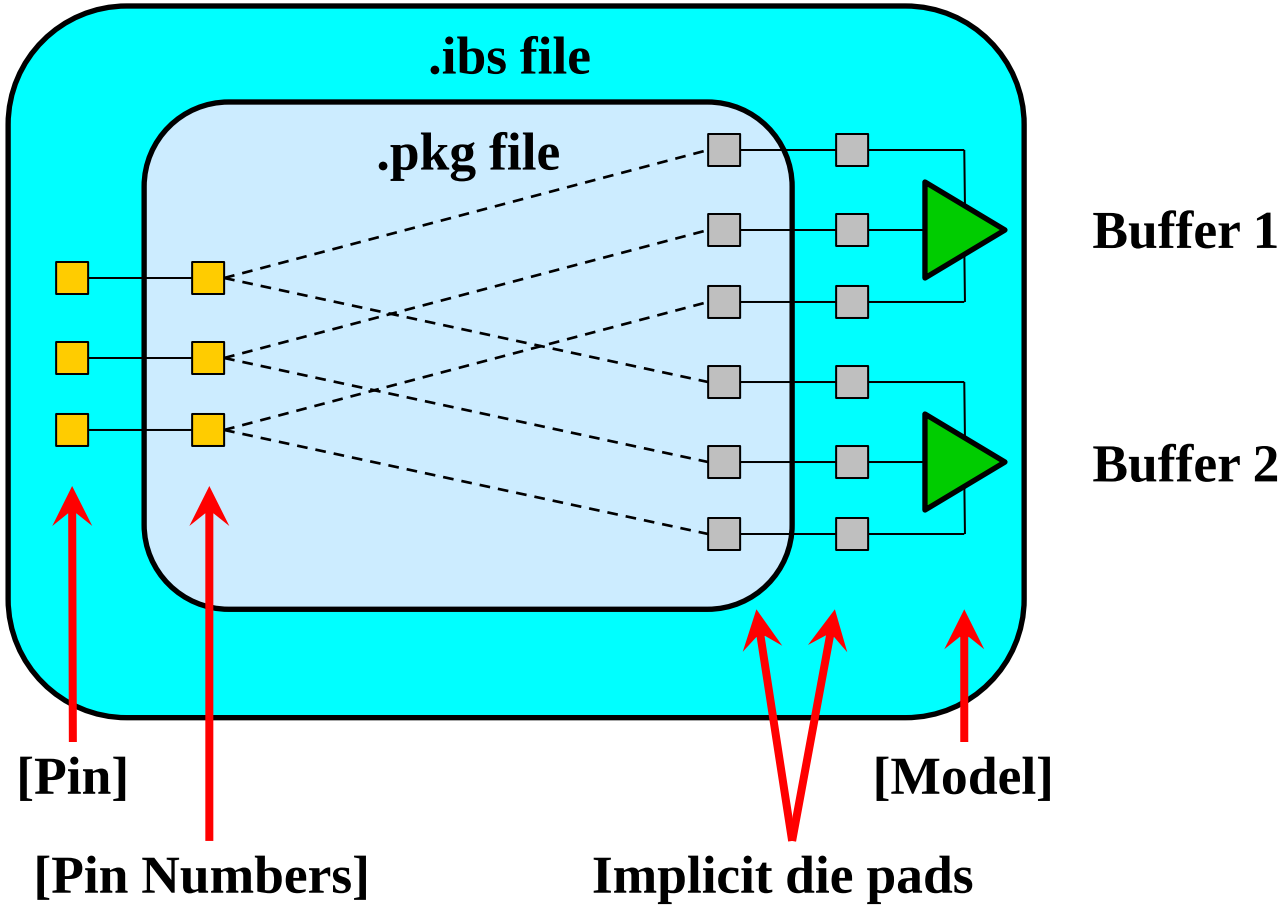


Figure 12: Reference example for [Node Declarations] keyword

How can we define specific paths between the supply terminals of a [Model] or [External Model] and the power pads and pins through the package model?

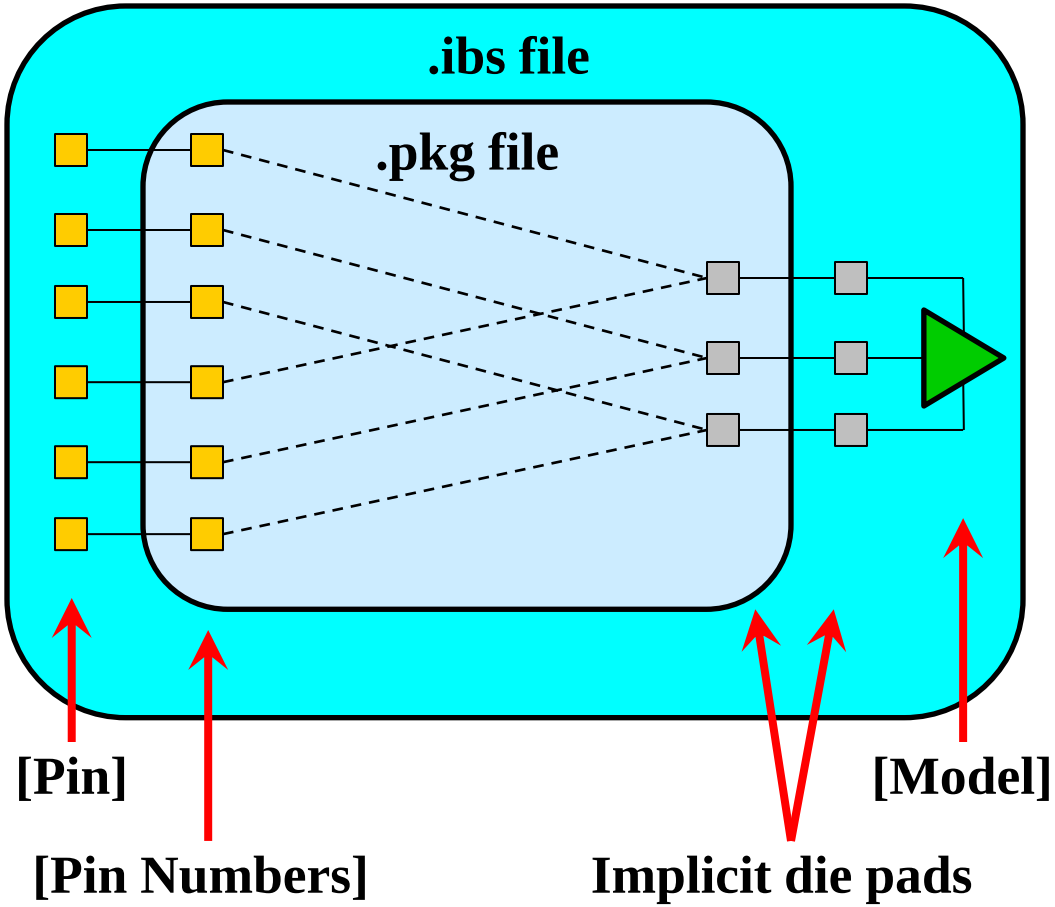
A fundamental problem in legacy IBIS



Buffers are "instantiated" by the 3rd column of the [Pin] keyword.

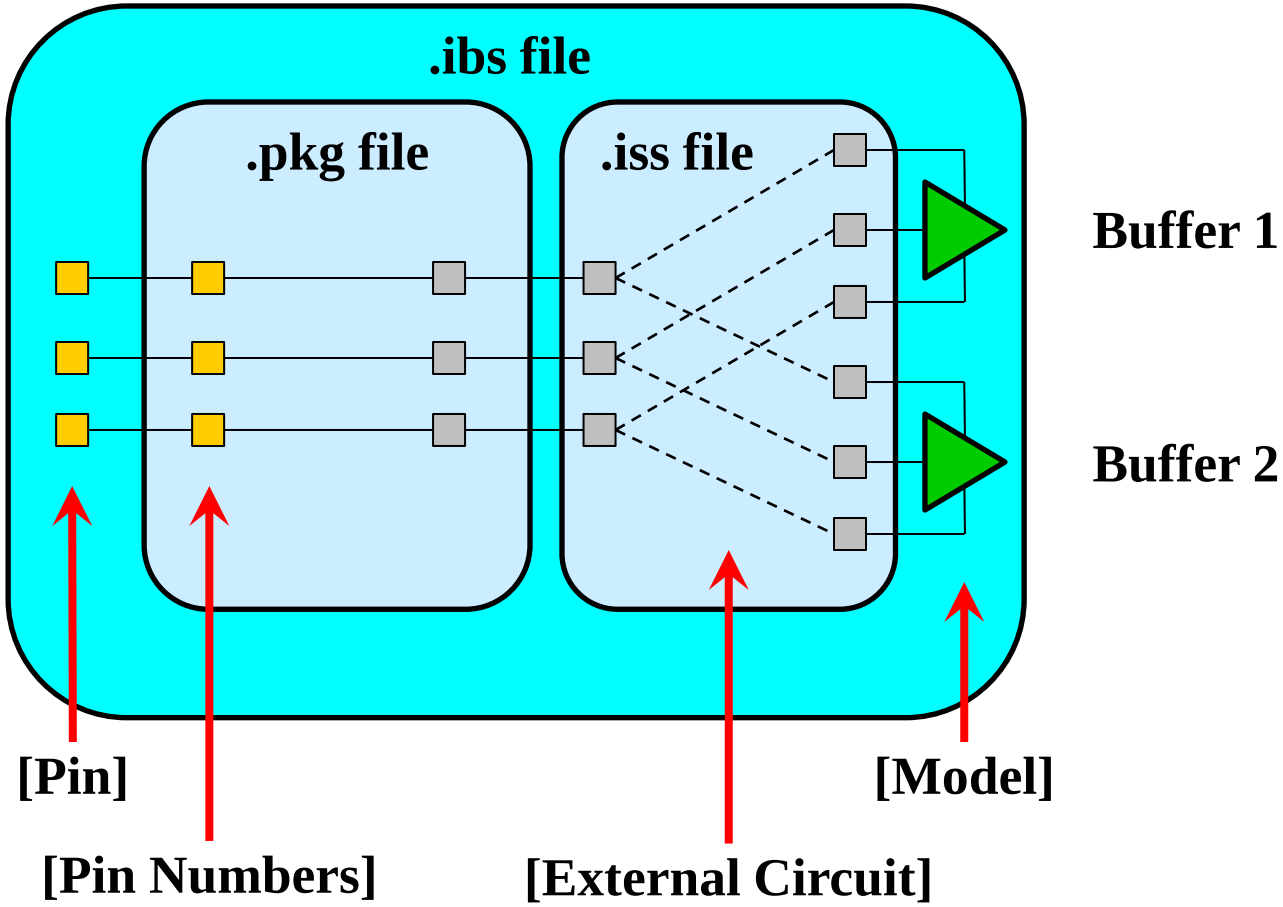
One signal pin can only instantiate one buffer in legacy IBIS.

A fundamental problem in legacy IBIS



Which signal pin should instantiate this buffer?

We also need to be able to model on-die interconnects

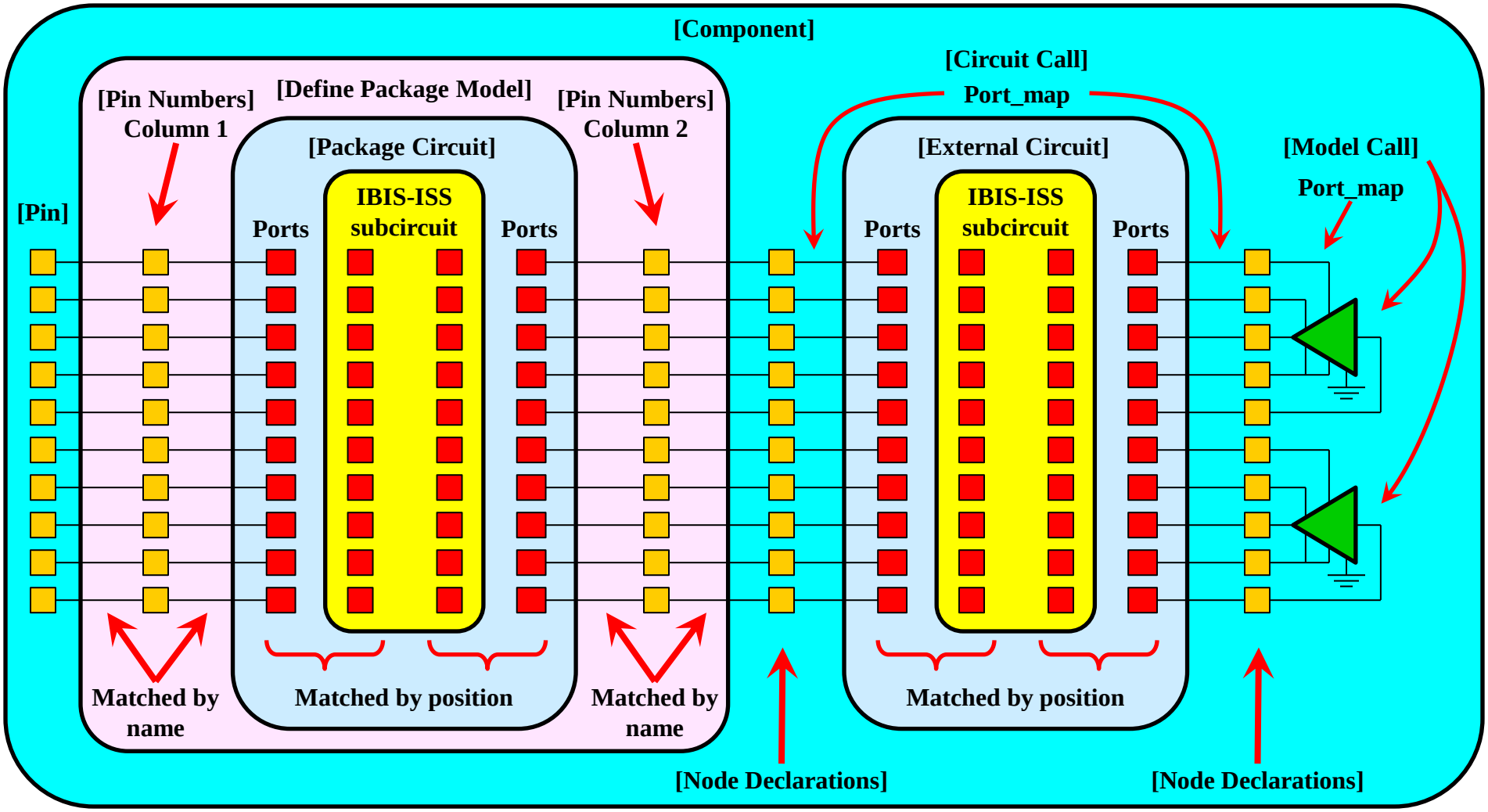


The terminals of [Model] are not declared in IBIS.
On-die interconnect models cannot be inserted between [Model] and the pads.

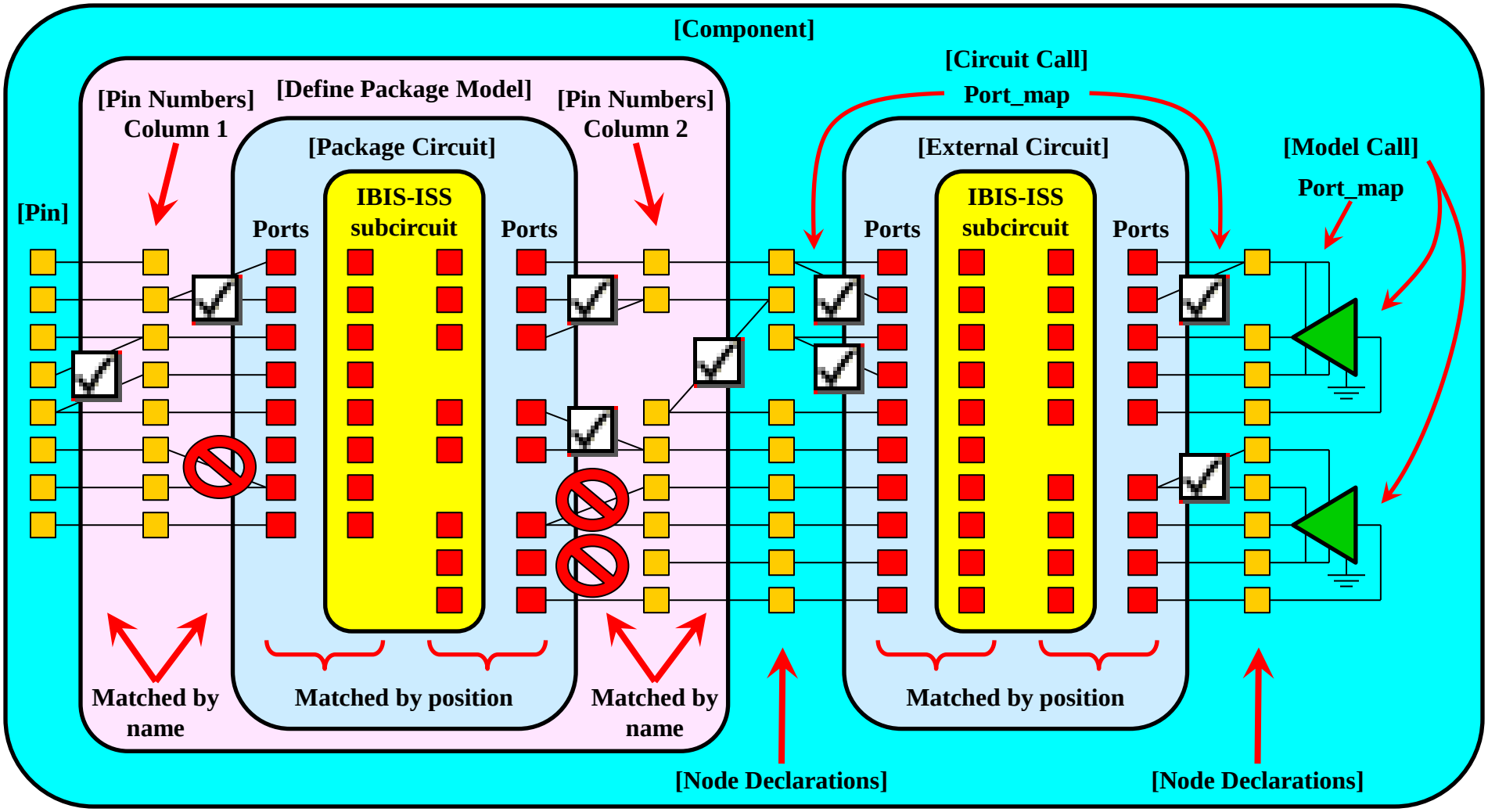
BIRD 145 helps to solve all of these challenges

- It seems that the biggest problem is that [Model]s are instantiated from the [Pin] keyword
  - useful for PCB layout or IC footprint driven EDA tools to find the [Model] for a particular "net"
  - gets in the way of non 1 to 1 pin/ball to pad/bump mapping
  - gets in the way of on-die interconnect modeling
- The best solution seems to be to instantiate [Model]s the same way as [External Circuit]s, using [Model Call]
  - supports named [Model] terminals anywhere on the die
    - does not rely on the cumbersome [Pin Mapping] keyword to achieve this
  - supports connections to named die pads/bumps
  - as a result, arbitrary package and on-die interconnect models can be described with IBIS-ISS subcircuits
  - this is what BIRD 145 proposes

Block diagram of BIRD 125 and 145



Capabilities and limitations of the proposed syntax



Explaining the limitation

```
[Define Package Model]  QS-SMT-cer-8-pin-pkgs
[Manufacturer]          NoName Company, Inc.
[OEM]                   Another NoName Package Company, Inc.
[Description]           8-Pin ceramic SMT package
[Number Of Pins]        8
|
[Pin Numbers]
 10   DiePort = IDiePort_10
  1   DiePort = IDiePort_1
 11   DiePort = pad_11
  2   DiePort = pad_2a
  2   DiePort = pad_2b
  3   DiePort = IDiePort_3
  4a  DiePort = pad_4
  4b  DiePort = pad_4
  5   DiePort = IDiePort_5
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  PackageModel.spi  S_pkg
|
| Parameters List of parameters
Parameters  TSFile = "My_TstoneFile.s16p"
|
| Ports are in same order as defined in SPICE
Ports  10  1  11  2  3  4a  4b  5
Ports  IDiePort_5  pad_4  IDiePort_3  pad_2b
Ports  pad_2a      pad_11  IDiePort_1  IDiePort_10
|
[End Package Circuit]
[End Package Model]
```

Note:

This is a minor syntactical limitation only. It does not impose any restrictions on what circuit topologies can be modeled. This limitation could be removed easily with a slight change to the proposed syntax.

The `Ports` list must contain at least one and no more than one pin/node name per "position". This could be solved by adding a `Port_map` subparameter.

Modified Figure 12 to illustrate BIRD 125 and 145

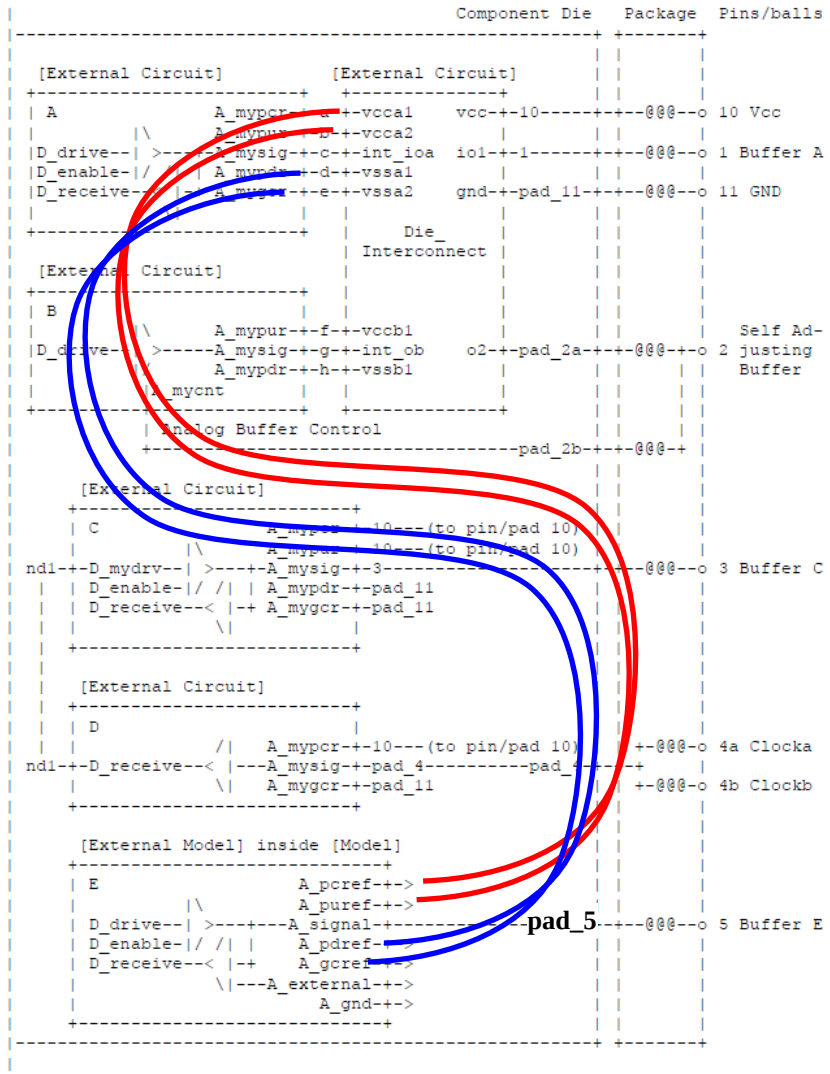


Figure 12: Reference example for [Node Declarations] keyword

Modified Figure 12 using BIRD 125 and 145

Legacy IBIS file:

```
[Pin] signal_name  model_name
 10   Vcc          POWER
  1   A0           CIRCUITCALL
 11   GND          GND
  2   CAS0         CIRCUITCALL
  3   A1           CIRCUITCALL
 4a   Clk_A        CIRCUITCALL
 4b   Clk_B        CIRCUITCALL
  5   A2           MODELCALL
|
[Node Declarations]
a  b  c  d  e  f  g  h  nd1                | List of die nodes
pad_2a  pad_2b  pad_4  pad_11  pad_5 | List of die pads
[End Node Declarations]
|
[Package Model]  QS-SMT-cer-8-pin-pkgs
|
[Model Call] E                | Instantiates [Model] named "E"
Signal_pin 5
|
Port_map   A_pcref    a       | Connection to internal die-node
Port_map   A_puref    b       | Connection to internal die-node
Port_map   A_signal   pad_5   | Connection to explicit die-pad
Port_map   A_pdref    d       | Connection to internal die-node
Port_map   A_gcref    e       | Connection to internal die-node
|
[End Model Call]
|…
```

PackageModel.cir file:

```
**********************************************************
.SUBCKT  S_pkg  P1  P2   P3   P4   P5   P6   P7   P8
+               P9  P10  P11  P12  P13  P14  P15  P16
+ TSFile="TouchstoneFileName.s16p"

Sdriver  P1  P2   P3   P4   P5   P6   P7   P8
+        P9  P10  P11  P12  P13  P14  P15  P16
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
**********************************************************
.ends
```

IBIS .pkg file:

```
|-------------------------------------------------------------
| This example implements a package model using an IBIS-ISS
| subcircuit for the drawing in Fig. 12 on pg. 136 of the
| IBIS v5.0 specification.
|-------------------------------------------------------------
|
[Define Package Model]  QS-SMT-cer-8-pin-pkgs
[Manufacturer]          Quality Semiconductors Ltd.
[OEM]                   Acme Package Co.
[Description]           8-Pin ceramic SMT package
[Number Of Pins]  8
|
[Pin Numbers]
 10   DiePort = IDP_10
  1   DiePort = IDP_1
 11   DiePort = pad_11
  2   DiePort = pad_2a
  2   DiePort = pad_2b
  3   DiePort = IDP_3
 4a   DiePort = pad_4
 4b   DiePort = pad_4
  5   DiePort = pad_5
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  PackageModel.cir  S_pkg
|
| Parameters List of parameters
Parameters  TSFile = "My_TstoneFile.s16p"
|
| Ports are in same order as defined in SPICE
Ports  10  1  11  2  3  4a  4b  5
Ports  IDP_5  pad_4  IDP_3  pad_2b
Ports  pad_2a  pad_11  IDP_1  IDP_10
|
[End Package Circuit]
[End Package Model]
```

Matched by name

Implicit die ports (in blue)

Explicit die ports (in red) are declared under [Node Declarations]

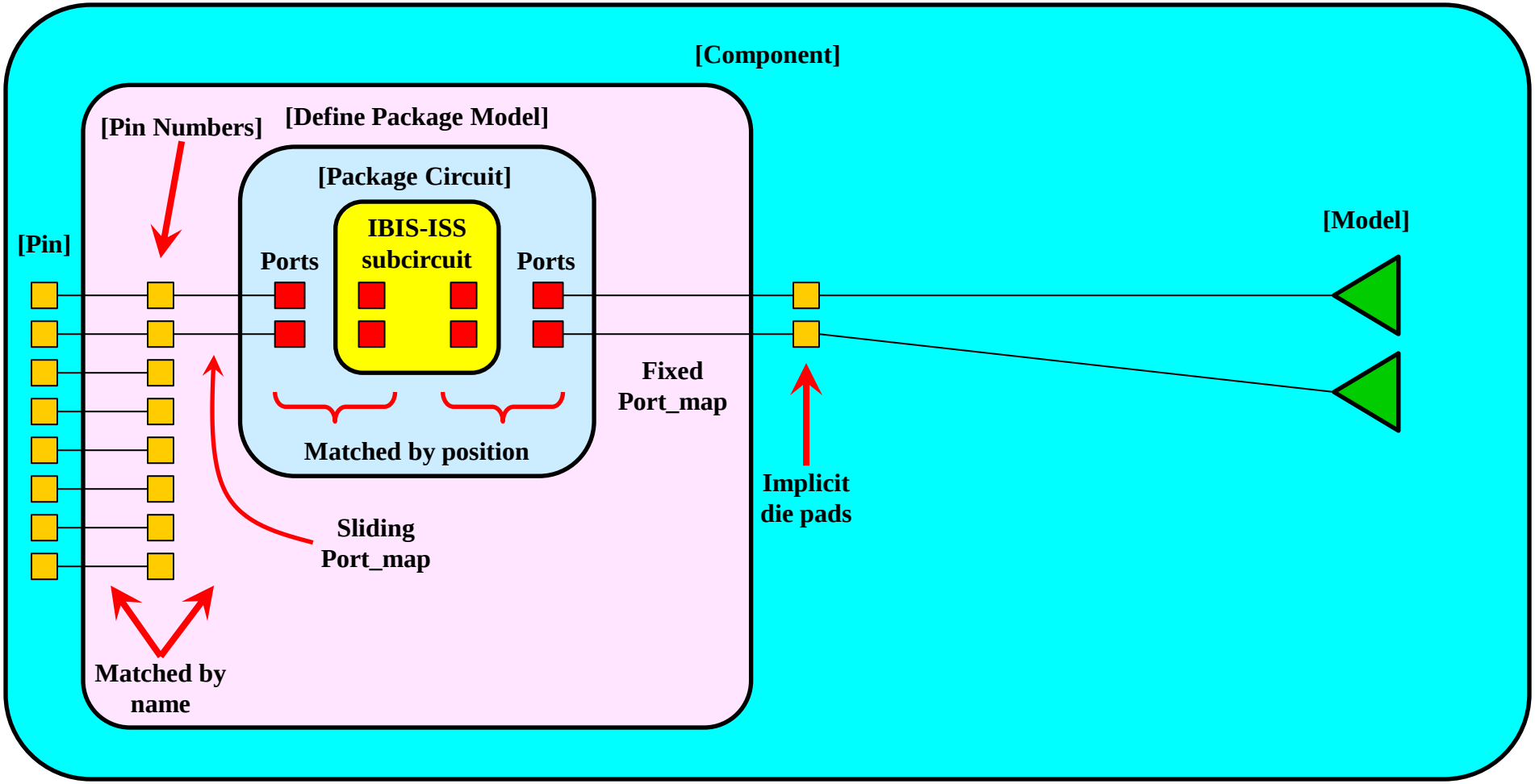
Matched by position

Matched by name

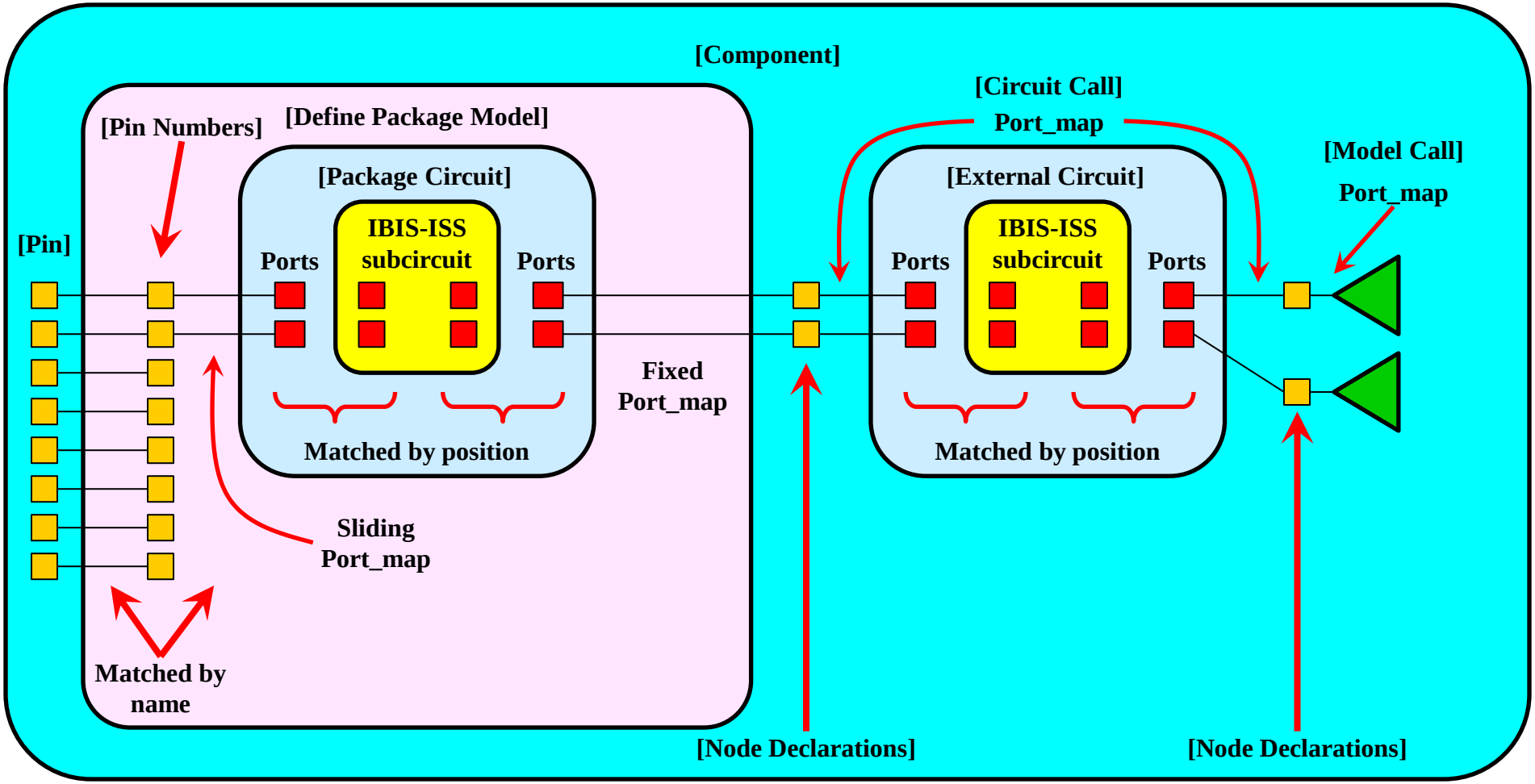
A more important limitation

- **The proposal relies on known pin/ball and pad/bump names**
  - most connections are made by matching the names of pins/balls, pads/bumps, on-die nodes and buffer model terminal names
  - only the IBIS-ISS subcircuit instantiations are made by position
- **This implies a fixed topology ("post" chip/package layout)**
- **Applying a parameterized "few-signal-lane" (no power) package (and/or on-die interconnect) model to an arbitrary subset of a larger bus (interface) is cumbersome**
  - it could be done with [Alternate Package Model] or a second level of subcircuit inside the IBIS-ISS model, but the pin/ball, and pad/bump names would still have to be known and defined
- **The idea of a "sliding Port_map" could solve this problem**
  - the following slides introduce this idea
  - this idea is in its infancy, so don't take everything literally

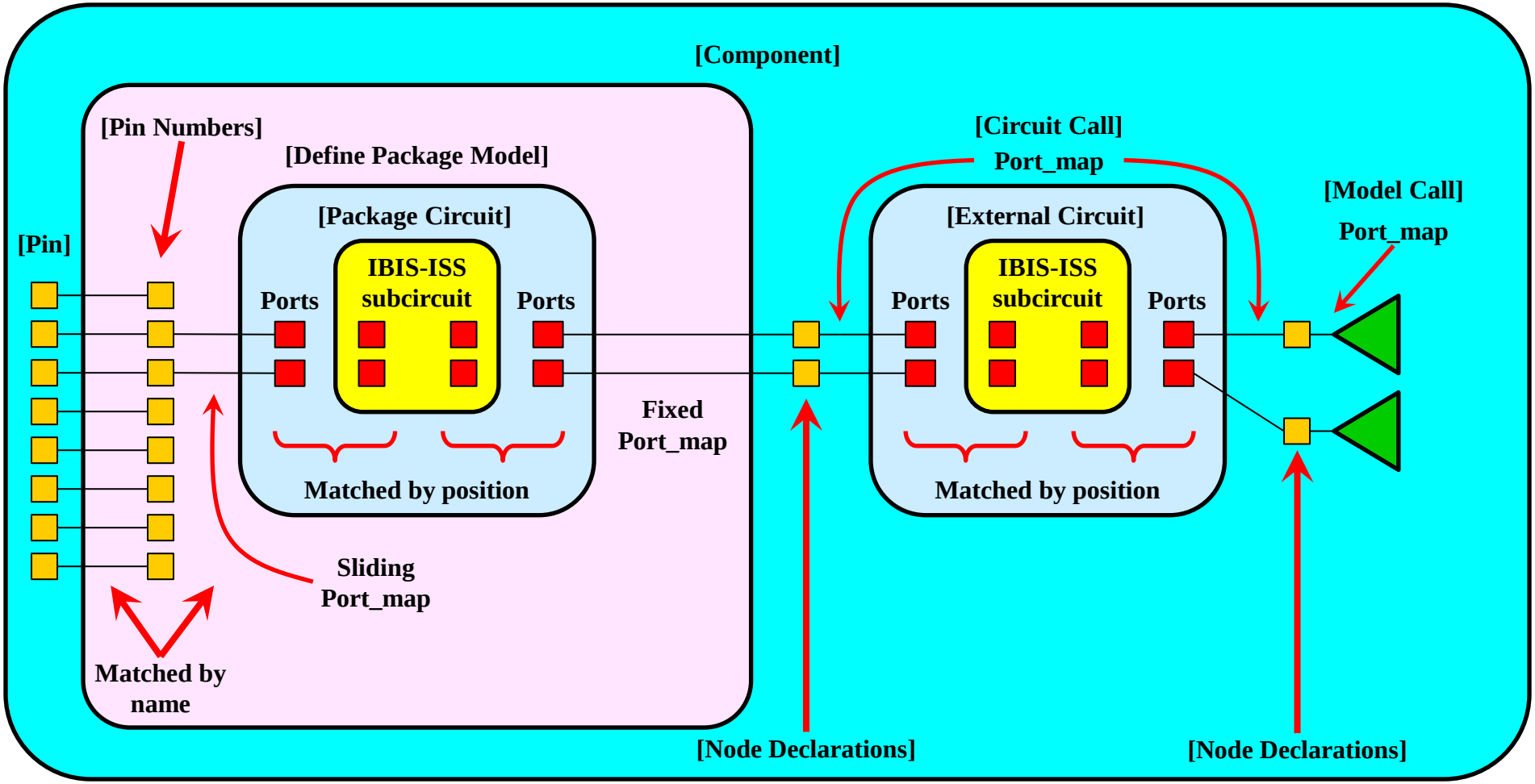
The sliding Port_map idea with package only



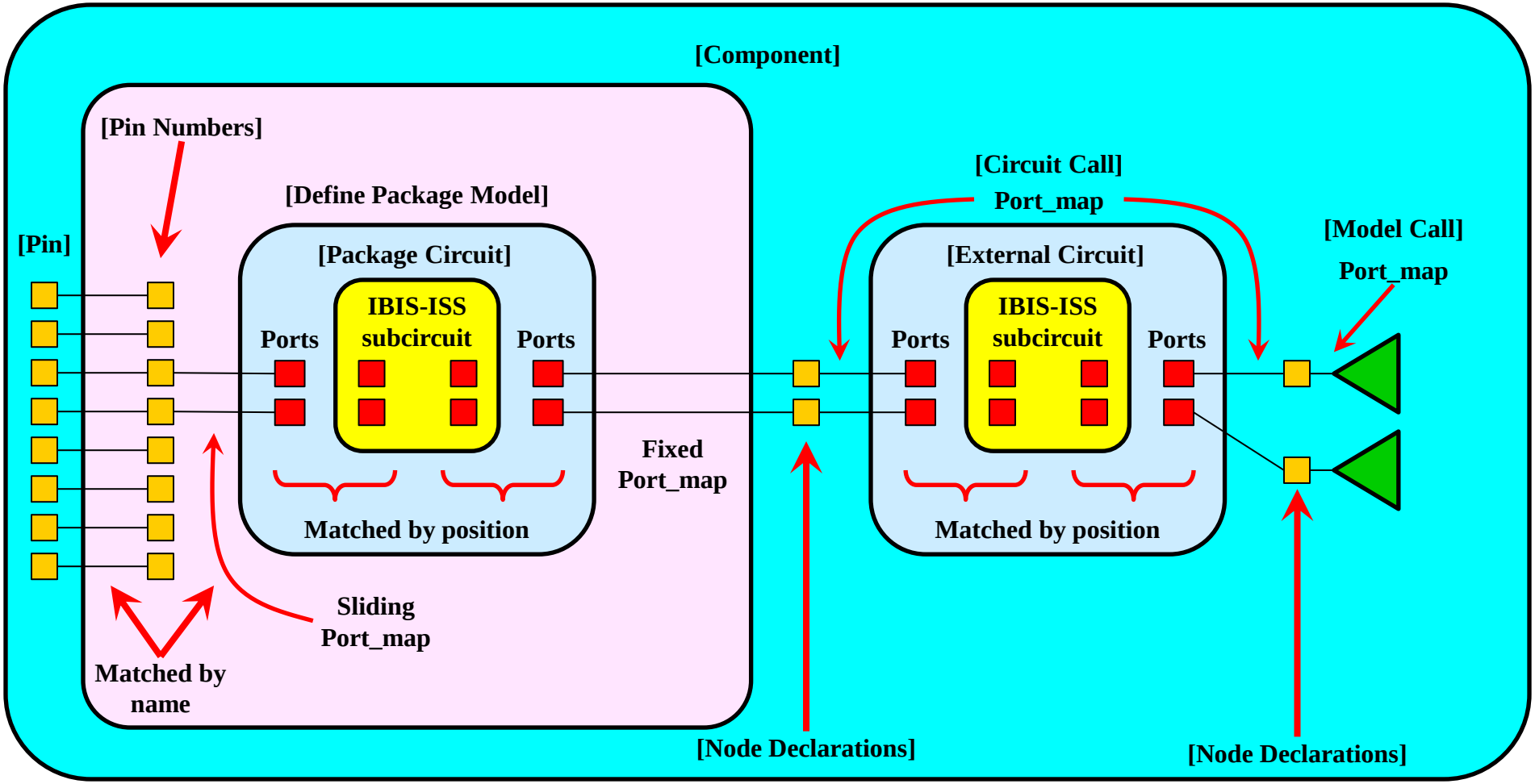
… and with package and on-die interconnect



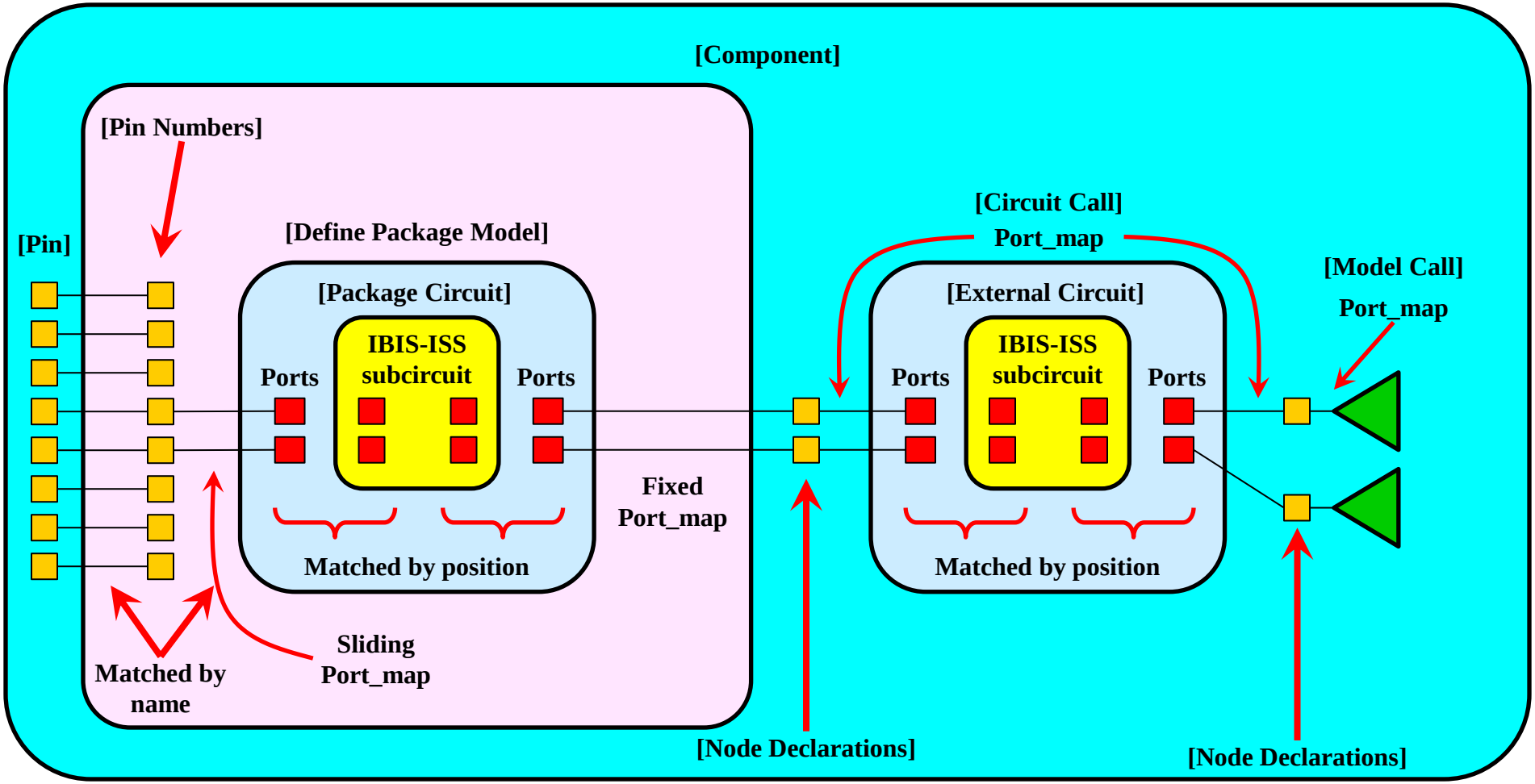
in position 2



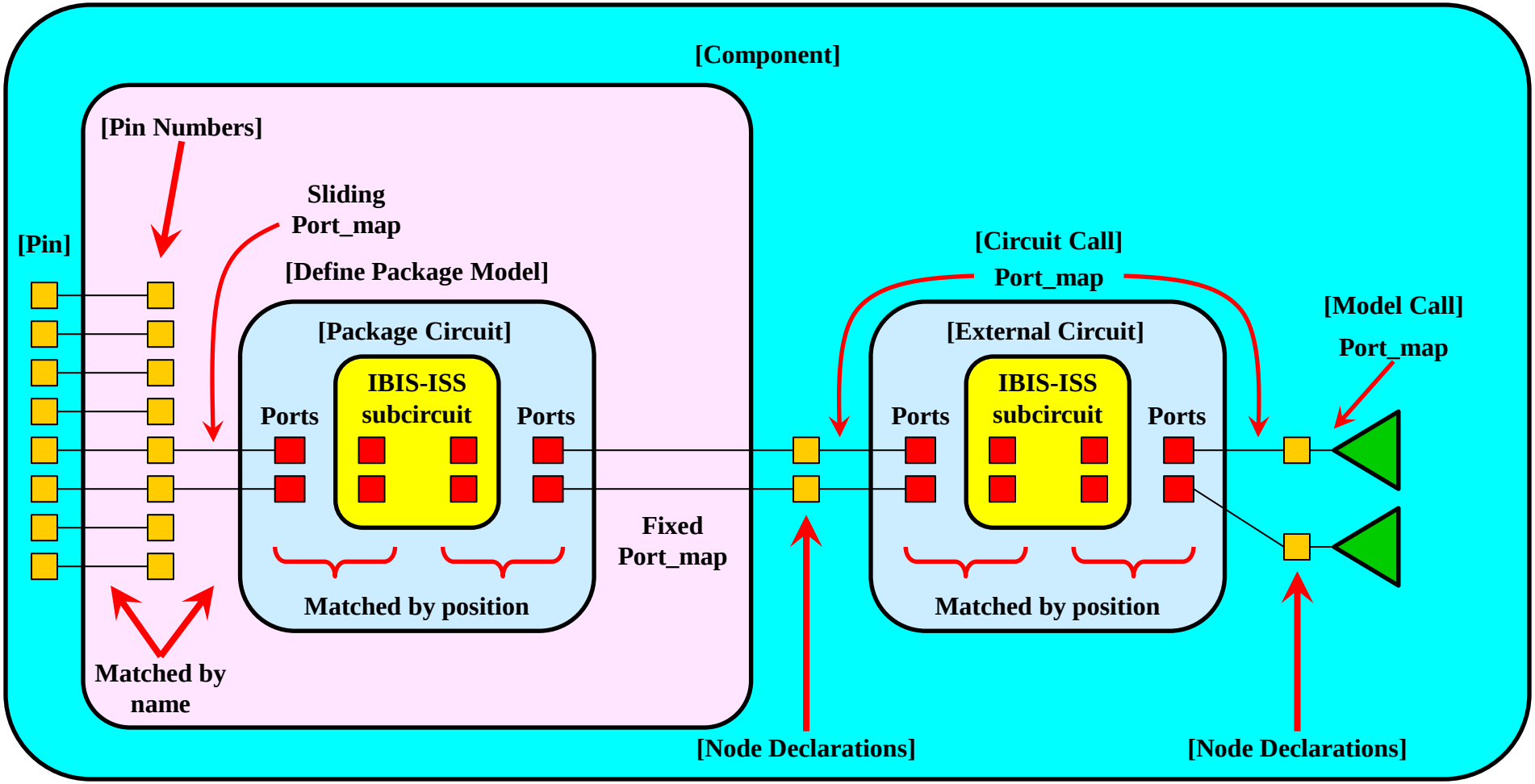
in position 3



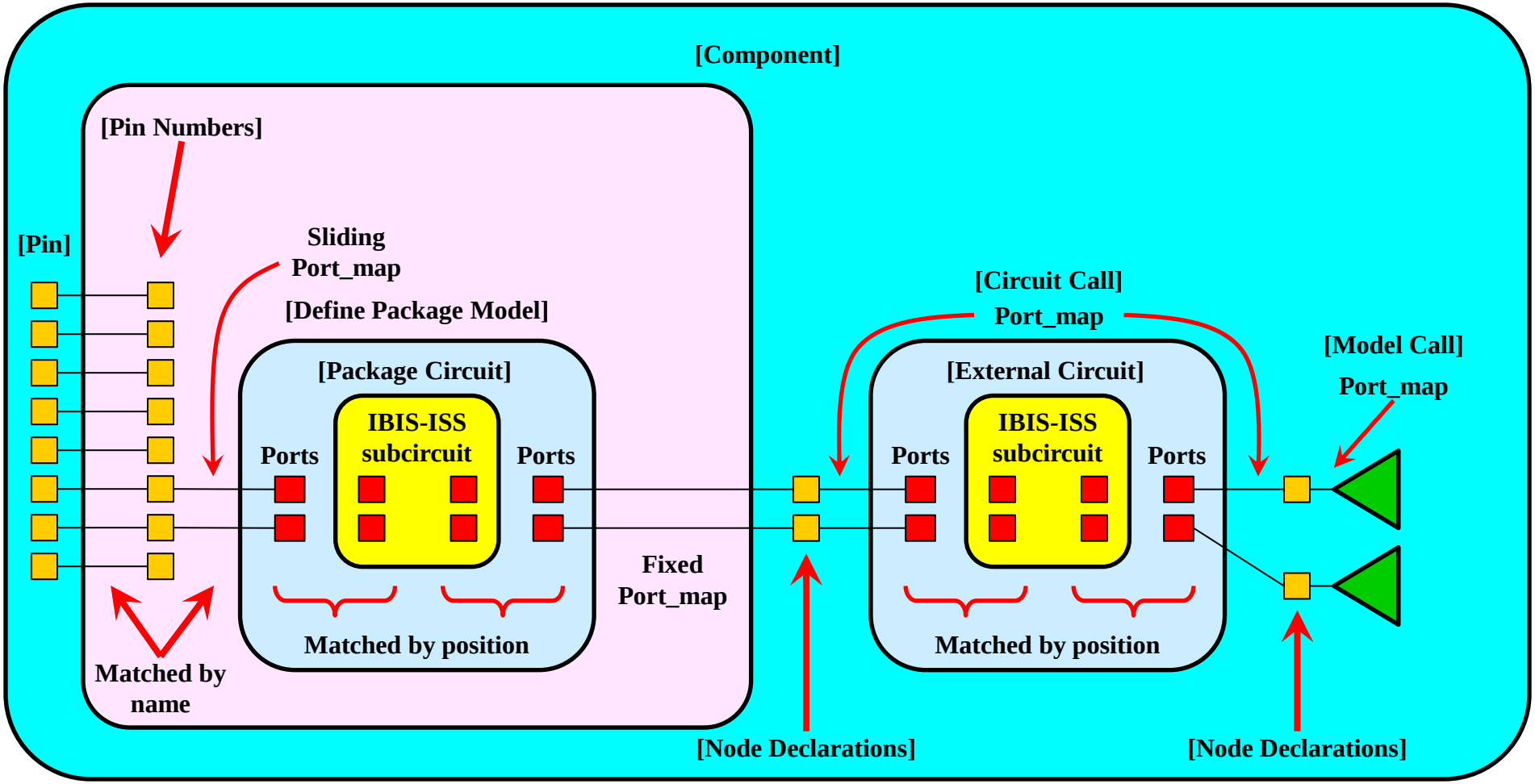
in position 4



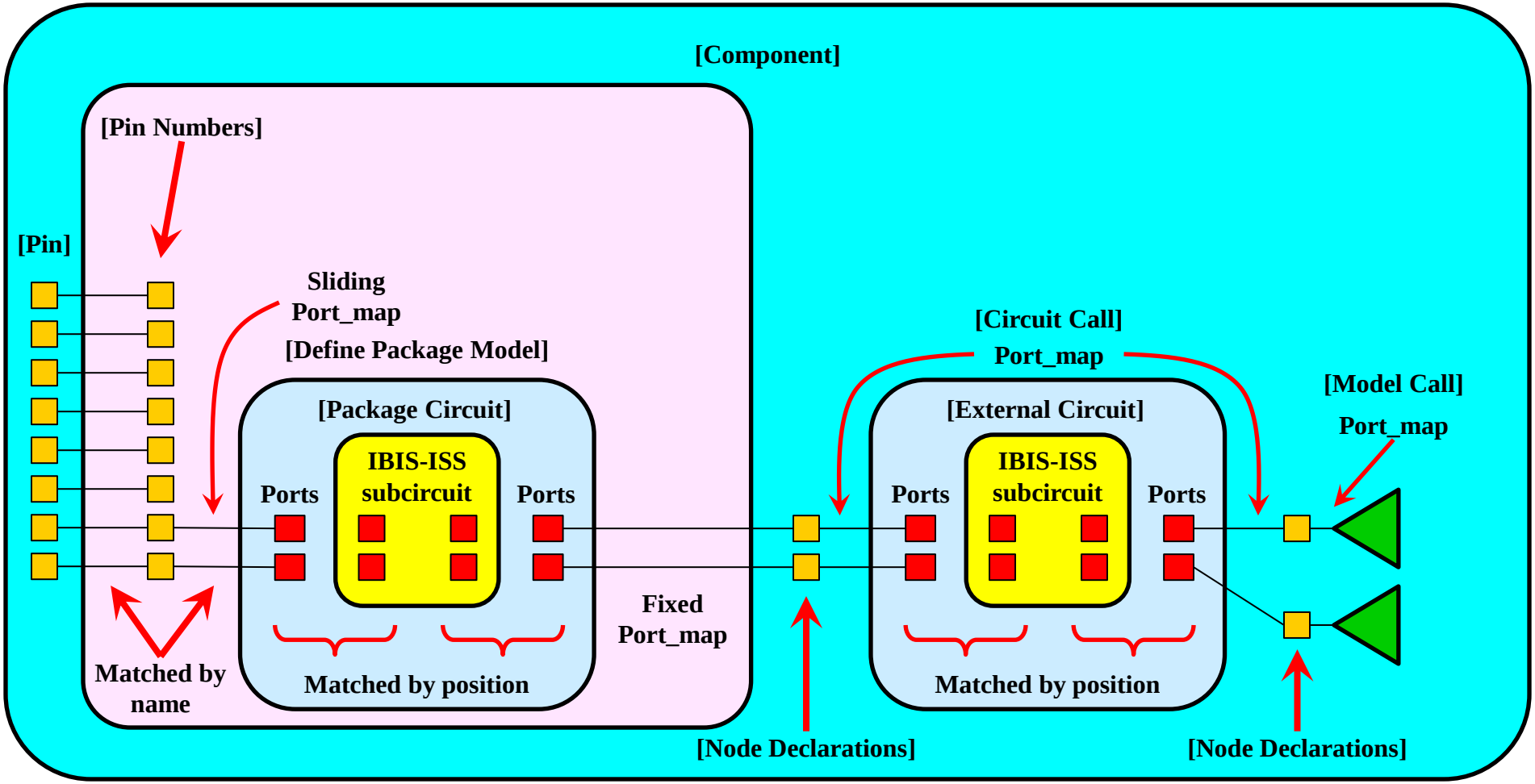
in position 5



in position 6



in position 7



Sliding Port_map syntax (in red)

Legacy IBIS file:

```
[Pin] signal_name  model_name
  1   D0p          MODELCALL
  2   D0n          MODELCALL
  3   D1p          MODELCALL
  4   D1n          MODELCALL
  5   D2p          MODELCALL
  6   D2n          MODELCALL
  7   D3p          MODELCALL
  8   D3n          MODELCALL
|
[Node Declarations]
a      b                    | List of die nodes
pad_a  pad_b                | List of die pads
[End Node Declarations]
|
[Package Model]  QS-SMT-cer-8-pin-pkgs
|
[Model Call] A               | Instantiates [Model] named "A"
Signal_pin 1
Port_map   A_signal   pad_a  | Connection to explicit die-pad
[End Model Call]
|
[Model Call] B               | Instantiates [Model] named "B"
Signal_pin 2
Port_map   A_signal   pad_b  | Connection to explicit die-pad
[End Model Call]
|
|…
```

PackageModel.cir file:

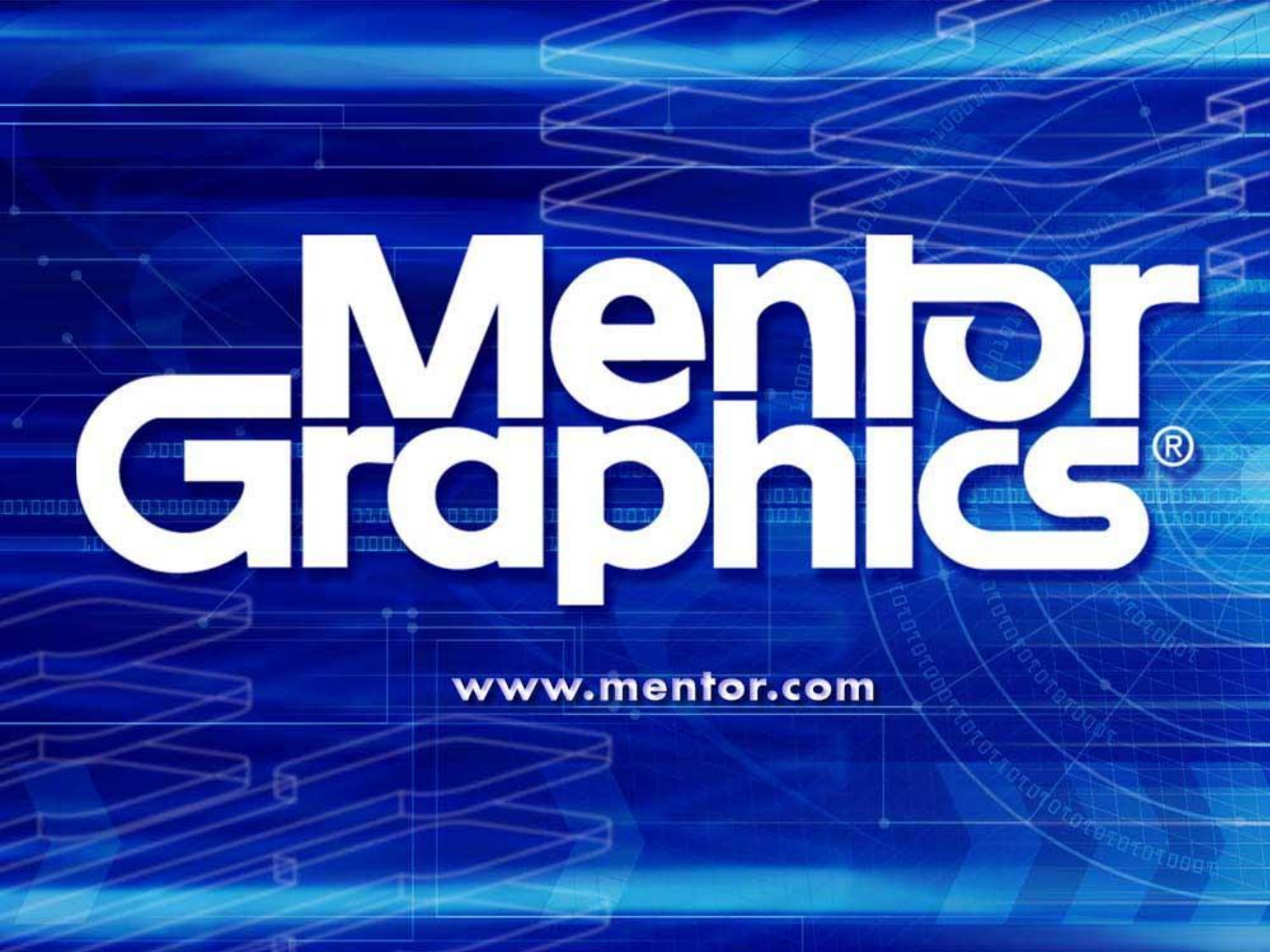
```
************************************************************
.SUBCKT  S_pkg  P1  P2   P3   P4
+ TSFile="TouchstoneFileName.s4p"

Sdriver  P1  P2   P3   P4
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
************************************************************
.ends
```

IBIS .pkg file:

```
[Define Package Model]  QS-SMT-cer-8-pin-pkgs
[Manufacturer]          Quality Semiconductors Ltd.
[OEM]                   Acme Package Co.
[Description]           8-Pin ceramic SMT package
[Number Of Pins]  8
|
[Pin Numbers]
  1
  2
  3
  4
  5
  6
  7
  8
|
[Package Circuit]
|
Port_map  PortMapName_1  Position = thisfile.pkg(TreeRootName(Position))  1
pins  1  2  3  4  5  6  7
Port_map  PortMapName_2  Position = thisfile.pkg(TreeRootName(Position))  1
pins  2  3  4  5  6  7  8
|
Port_map  PortMapName_3
nodes  pad_1
Port_map  PortMapName_4
nodes  pad_2
|
Language IBIS-ISS
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  PackageModel.cir  S_pkg
|
| Parameters List of parameters
Parameters  TSFile = thisfile.pkg(TreeRootName(TSfile)) "My_TstoneFile.s4p"
|
| Ports are in same order as defined in SPICE
Ports  PortMapName_1  PortMapName_2  PortMapName_3  PortMapName_4
|
[End Package Circuit]
[End Package Model]
```

Some observations

- The use of "Port_map" could eliminate the previously proposed 2nd column for [Pin Numbers]
  - "Port_map" would be then used to declare implicit die pads
  - "Port_map" can also support sliding along die pads or die nodes
  - this would remove the small syntactical limitation mentioned before
- This is not limited to signal paths only
  - power pins and pads could also be listed in "Port_map"
- Parameters could reference parameter trees
  - this would allow for synchronizing position with model parameter values (using Dependency Table)


Mentor Graphics®
www.mentor.com