IBIS-ISS Package Modeling Discussion

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IBIS ATM

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Agenda

- Posted 8/12/7 Presentation
  - **http://tinyurl.com/cvykehz**
- Comments During Presentation and Received by E-mail
- Response to Comments Received by E-mail
- Open Discussion on Additional Questions on Presentation
- Open Discussion on Following Questions
  - Does the functionality described in this presentation satisfy your needs to generate package and on-die models using that your customers require?
  - If not, what additional functionality do you need?
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Comments During Presentation and Received by E-mail

- Are Supply Voltages Values Necessary?
- Are X-Y Coordinates Necessary for Pins and Die Pads?
- Need to add association of Power Clamp and Ground Clamp supply signal names to [Models]
- A Related Set of Comments
  - "Ports" "Sparse Ports"
    - Functionality was agreed to but alternative method to define the ports of subckts requested.
  - FEXT/NEXT was confusing
  - Both Victim/Interface Modeling Should have Same Mechanism to Indicate Victim/Aggressor Channels

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Why Supply Voltages Values Necessary

- The [Model] [Voltage Range] describes the test conditions that were used to generate the Ramp, IV and VT data in a [Model]
  - Consider a coupled simulation that has two [Model]s, and the two [Model] Ramp, IV and VT data where generated with different [Voltage Range] test conditions.
    - What Voltage should be applied to the Pin of the package?
  - How does the IC Vendor tell the EDA tool the typ/min/max Voltage applied at the package pin?
- I believe the only answer to the above two questions is adding records to IBIS to indicate the typ/min/max Supply Voltages applied at the package pin

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Are X-Y Coordinates Necessary for Pins and Die Pads?

- No, but they can be useful
- Board, Package and On-Die Models are generated from three different tools. What “Handles” does each tool have to identify a Port of the model.
  - PCB Layout
    - Reference Designator / Pin Number (Pin_name)
    - PCB Cad Net Name
    - X-Y Board Coordinate
  - Package Layout
    - Pins
      - Board Connector Designator / Pin Number (Pin_name)
      - Package Cad Net Name
      - X-Y Package Coordinate
    - Die Pads
      - Die Connector Designator / Pin Number (Pin_name)
      - Package Cad Net Name
      - X-Y Package Coordinate
  - IC Layout
    - Die Pads
      - Chip Connector Designator / Pin Number (Pin_name)
      - Chip Cad Net Name
      - X-Y Chip Coordinate

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X-Y Coordinates are the Most Reliable Method of Making Connection Between Board/Package/Chip Models

- How to make connections between Package and Board?
  - Pin Number?
    - Sometimes reliable, sometime not
  - CAD Net Name?
    - Unreliable, Fuzzy Logic an be useful
  - X-Y Coordinate
    - Reliable
      - Can create examples that break this method
      - Practically, such examples are very rare, if not existent, and can be further resolved using Fuzzy Logic on Pin Number and Net Name
- How to make connections between Package and Chip?
  - Pin Number?
    - Rarely reliable
  - CAD Net Name?
    - Rarely reliable
  - X-Y Coordinate
    - Reliable
      - Can create examples that break this method
      - Practically, such examples are very rare, if not existent, and can be further resolved using Fuzzy Logic on Pin Number and Net Name
- Note that x-y coordinates are used as an aid to generating Package and On-Die models, and are not used in the IBIS-ISS Package or On-Die Models

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Adding association of Power Clamp and Ground Clamp supply signal names to [Models]

[Model] DQ

Pullup_Signal_name	VDD
Pulldown_Signal_name	VSS
Power_clamp_Signal_name	VDD_Clamp
Ground_clamp_Signal_name	VSS_Clamp

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Ports Interface Needs Improvement!

- The following example address the comments made during the 8/7/12 presentations and e-mails received.
- Thanks for the suggestions made.

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Rambus Forked Clock

```
(Package_models
      (Xclk
            (File          xclk.mod)
            (subckt        xclk)
|     (Ports       A1 A2 A3 A4 D.A1 D.A2)
            (Model_ports
                  (1 (Type Pin) (Pin_name A1))
                  (2 (Type Pin) (Pin_name A2))
                  (3 (Type Pin) (Pin_name A3))
                  (4 (Type Pin) (Pin_name A4))
                  (5 (Type Pad) (Pad_name D.A1))
                  (6 (Type Pad) (Pad_name D.A2))
            )
      )
)
```


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By Model_name

```
(Package_models
    (DQ
        (File           pkg1.mod)
        (Subckt         (Corner pkg1_typ pkg1_min pkg1_max))
        (Length         (Range 15 11 21))
        (Parameters Length)
        (Model_ports                Pin Pad
            (1 (Type Pin) (Model_name DQ))
            (2 (Type Pad) (Model_name DQ))))
    (DQS
        (File           pkg2.mod)
        (Subckt         (Corner pkg2_typ pkg2_min pkg2_max))
        (Length         (Range 15 11 21))
        (Parameters Length)
            (1 (Type Pin) (Polarity +) (Model_name DQS))
            (2 (Type Pin) (Polarity -) (Model_name DQS))
            (1 (Type Pad) (Polarity +) (Model_name DQS))
            (2 (Type Pad) (Polarity -) (Model_name DQS)))))
```


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By Pin_name

```
(Package_models
    (DQ
        (File           pkg1.mod)
        (Subckt         (Corner pkg1_typ pkg1_min pkg1_max))
        (Pin_name (List A1 A2 A3 A4 A5 A6 A7 A8))
        (Length         (Range 15 11 21))
        (Parameters Length)
        (Dependency_Table
            (ParameterNames Pin_name Length)
            (ColumnTypes In Out_Match)
            (A1                 11)
            (A2                 12)
            (A3                 14)
            (A4                 14)
            (A5                 11)
            (A6                 21)
            (A7                 18)
            (A8                 11)
        )
    )
```


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Signal / Power Coupling

```
(Package_models
    (DQ
        (File          pkg1.mod)
        (Subckt        (Corner pkg1_typ pkg1_min pkg1_max))
        (Length        (Range 15 11 21))
        (Parameters Length)
        (Model_ports
            (1 (Type Pin) (Channel 1) (Victim True) (Model_name DQ))
            (2 (Type Pad)(Channel 1) (Victim True) (Model_name DQ))
            (3 (Type Pin) (Channel 2) (Victim False) (Model_name DQ))
            (4 (Type Pad)(Channel 2) (Victim False) (Model_name DQ))
            (5 (Type Pin) (Channel 3) (Victim False) (Model_name DQ))
            (6 (Type Pad)(Channel 3) (Victim False) (Model_name DQ))
            (7 (Type Pin) (Channel 4)(Victim False)(Polarity +)(Model_name DQS))
            (8 (Type Pin) (Channel 4)(Victim False)(Polarity -)(Model_name DQS))
            (9 (Type Pad)(Channel 4)(Victim False)(Polarity +)(Model_name DQS))
            (10(Type Pad)(Channel 4)(Victim False)(Polarity -)(Model_name DQS))
            (11(Type Pin) (Supply VDD))
            (12(Type Pad)(Supply VDD))
        )
    )
```


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Sparse Ports

```
(Package_models
    (DDR3_DQ1 (Tstonefile        package.s1000p)
        (Model_Ports
            (1 (Type Pin) (Pin_name A1))          |DQ1
            (501 (Type Pad) (Pad_name D.A1))      |DQ1
            (102 (Type Pin) (Pin_name B1))        |VDD
            (202 (Type Pin) (Pin_name B2))        |VDD
            (302 (Type Pin) (Pin_name B3))        |VQQ
            (402 (Type Pin) (Pin_name B4))        |VQQ
            (502 (Type Pin) (Pin_name B5))        |VSS
            (602 (Type Pin) (Pin_name B6))        |VSS
            (752 (Type Pad) (Pad_name S7))        |VDD
            (852 (Type Pad) (Pad_name S1))        |VQQ
            (952 (Type Pad) (Pad_name T1))        |VSS
        )
    )
)
```

It is assumed that the EDA tool will extract an s11p from the s1000p

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