

# How to “Measure” VT Curves When Simulating

Walter Katz

Signal Integrity Software, Inc.

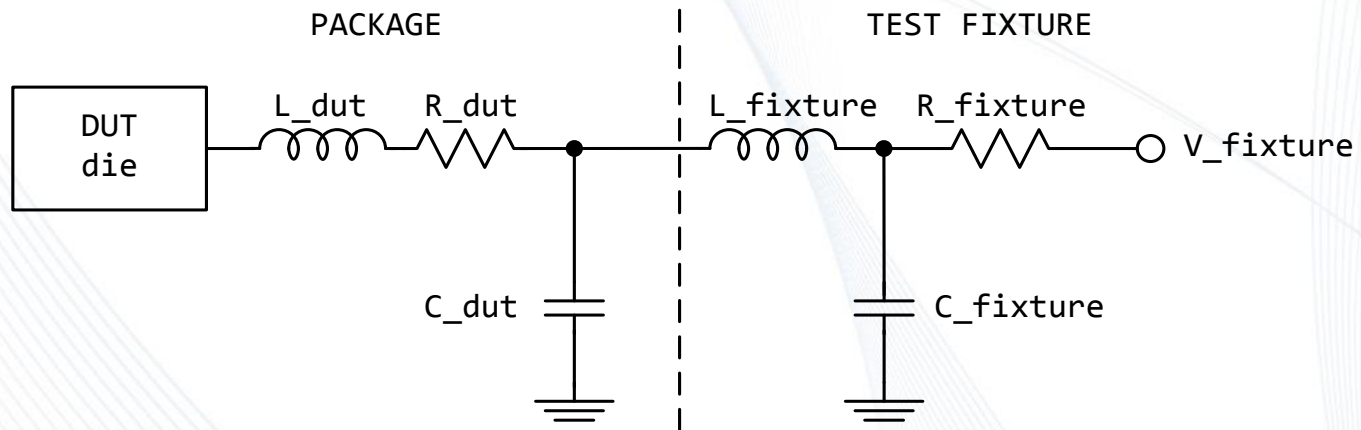
IBIS ATM

December 2, 2014

# Assumption being made in C\_comp Modeling BIRD

- The IBIS-ISS package on-die interconnect BIRD allows for an on-die interconnect circuit between the IBIS buffer and the die pad. This BIRD shall assume that VT and IV curves are measured at the signal terminal of the [Model] ([Model] Terminal). If there is no on-die interconnect model, then this is the “Die-Pad” in legacy IBIS models. If there is on-die interconnect, and an associated on-die interconnect model, then the IV and VT curves are assumed to be measured at the node between the [Model] and on-die interconnect ([Model] Terminal).
  - If the VT and IV curves are measured in a test fixture that includes the on-die interconnect, package and the test fixture itself, then all of the on-die interconnect, package and test fixture shall be de-embedded to give the VT and IV curves as if generated using the following simulation method.
  - If the VT and IV curves are generated by SPICE simulation it shall be assumed that the SPICE model shall include the C\_comp Model and that the terminal of the SPICE model shall be connected directly to the Test Fixture. When using the C\_comp Model, the model may not use L\_dut, R\_dut and C\_dut.

# IBIS 6.0 Waveform Fixtures

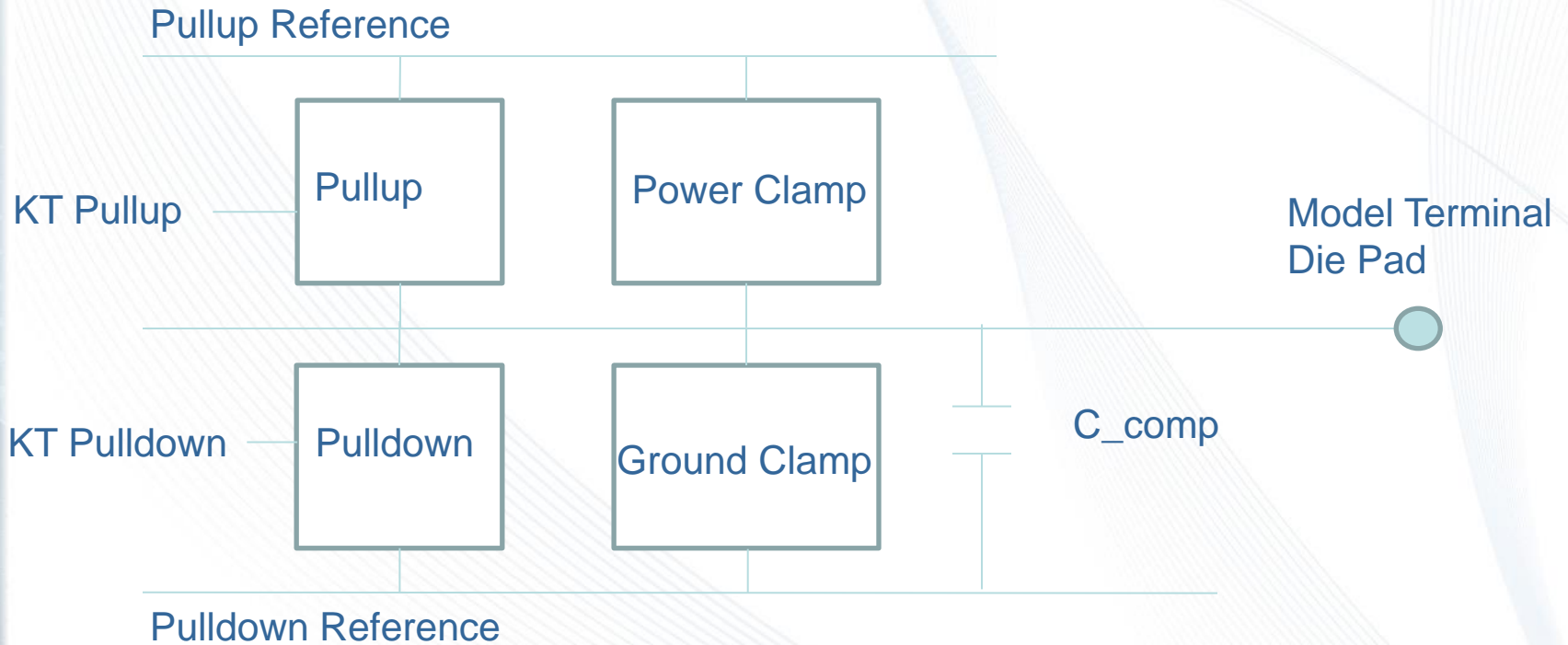


## •5 - [Rising Waveform] and [Falling Waveform] Fixtures

NOTE: The use of  $L_{dut}$ ,  $R_{dut}$ , and  $C_{dut}$  is strongly discouraged in developing waveform data from simulation models. Some simulators may ignore these parameters because they may introduce numerical time constant artifacts.

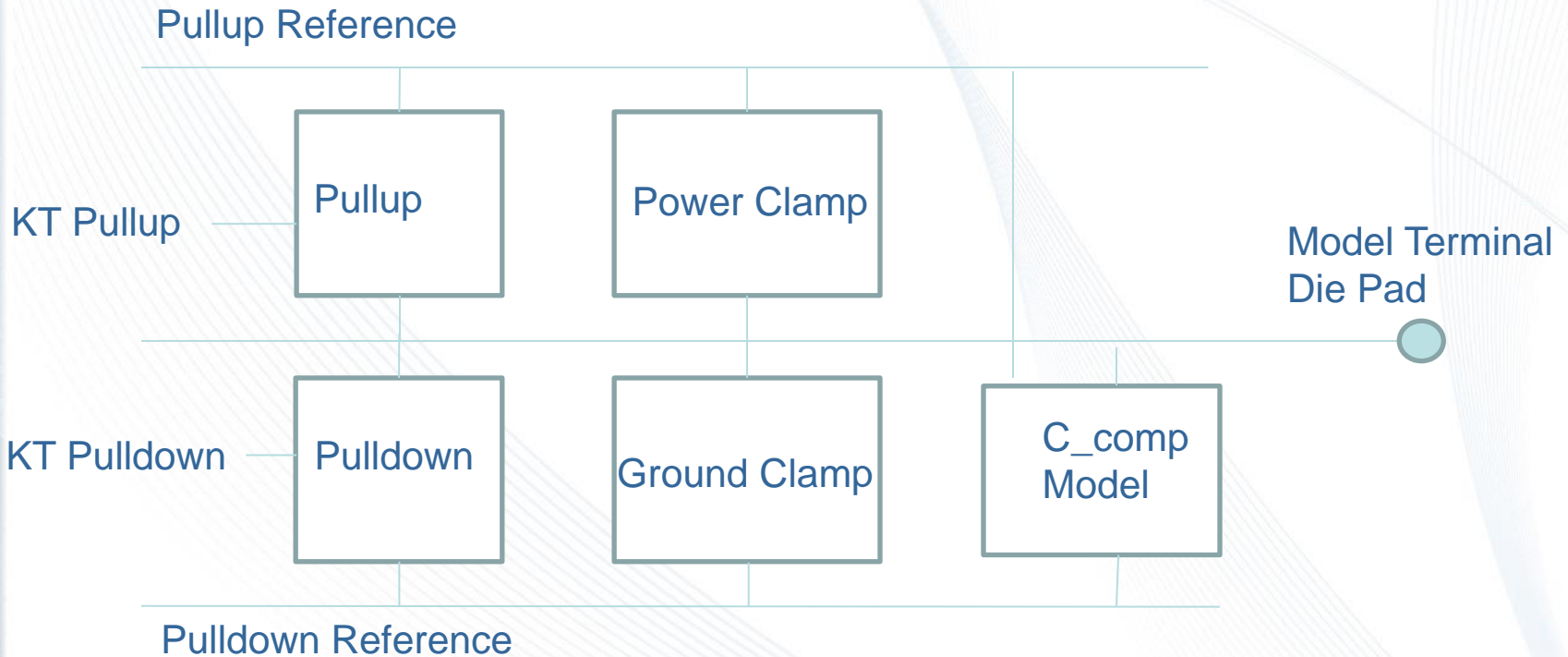
70

# Device Under Test (DUT) IBIS 6.0

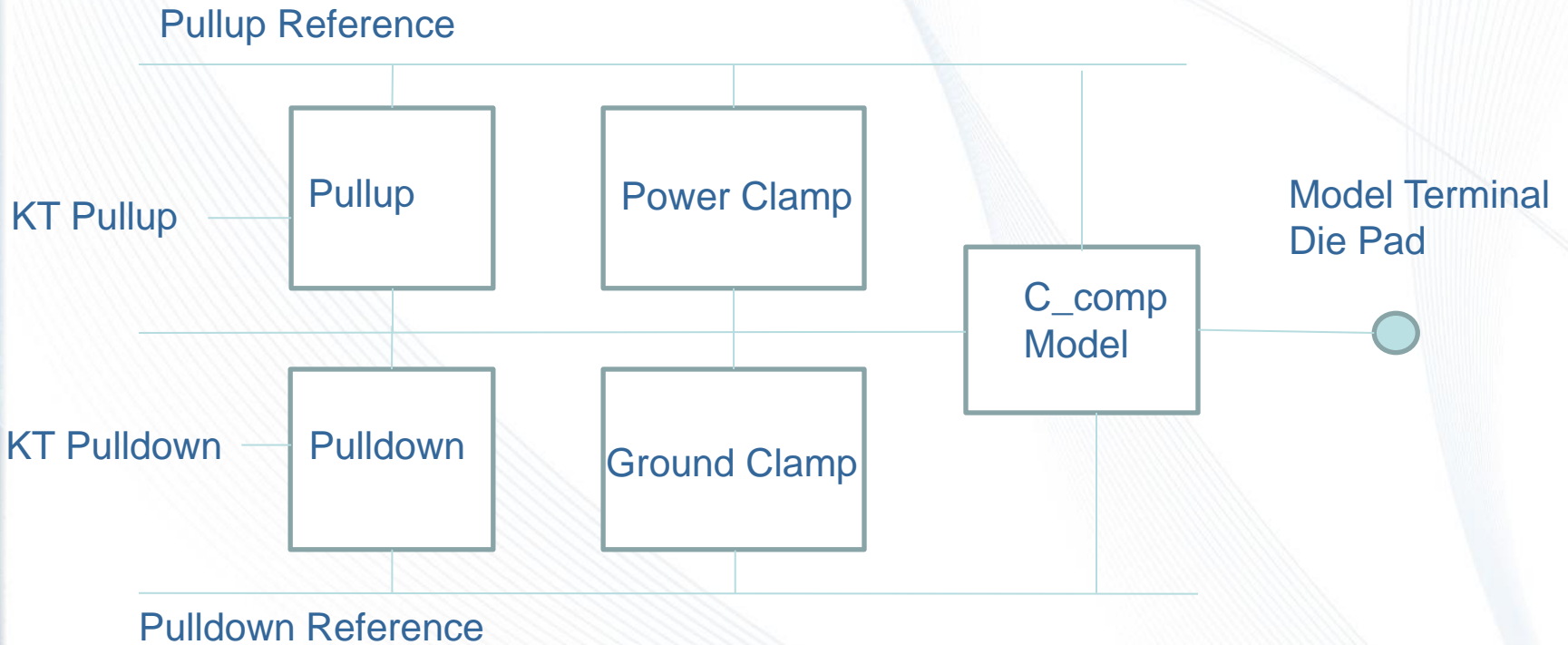




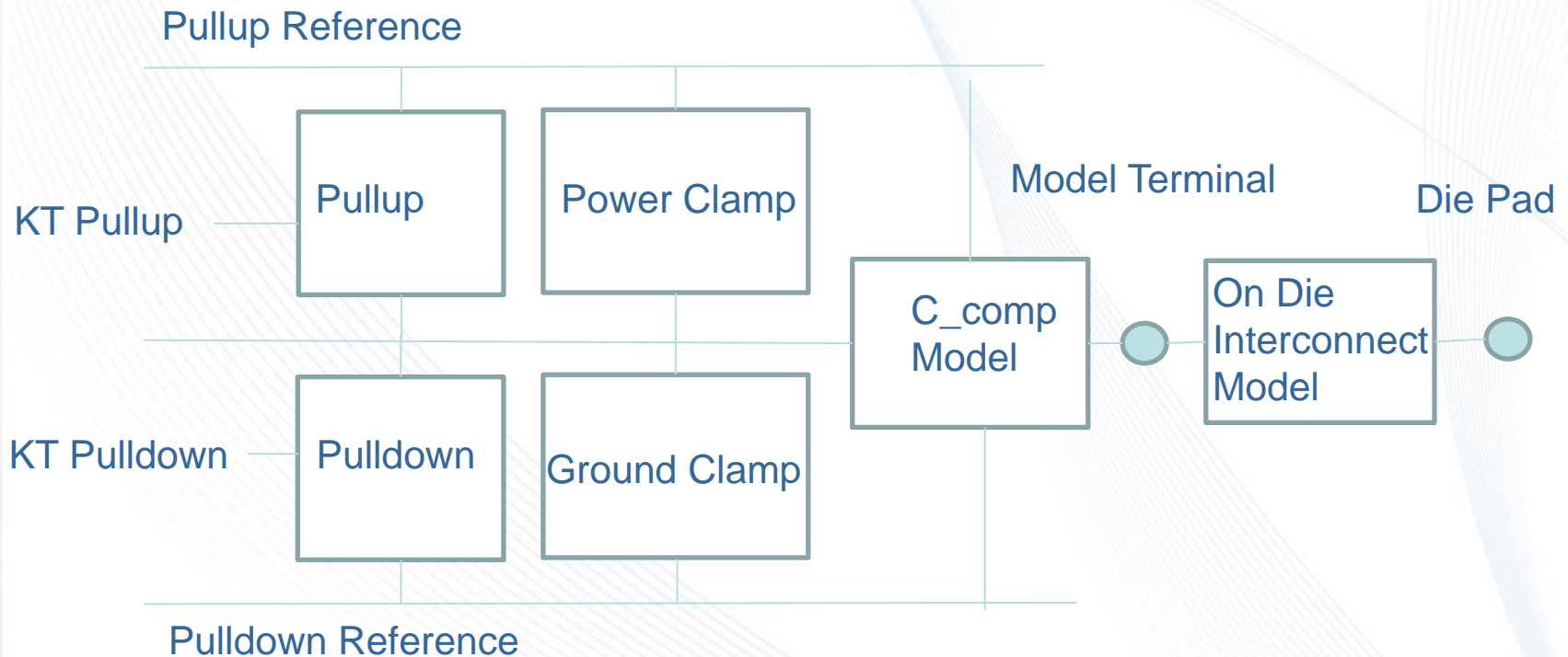
# Device Under Test (DUT) Parallel C\_comp Model



# Device Under Test (DUT) Series C\_comp Model



# Device Under Test (DUT) With On Die Interconnect



# Device Under Test (DUT) Simulate with On-Die Interconnect Replaced with Test Fixture

