

Reference [Model]s in IBIS

Bob Ross, Teraspeed Labs
bob@teraspeedlabs.com

ATM Meeting
March 22, 2016



Goals and Contents

- Reference models in IBIS
- C_comp connected to GND
- Reference models in EDA tools
- C_comp issues
- I-V, V-T, C_comp* extraction assumptions
- Extraction methods
- Recommendations

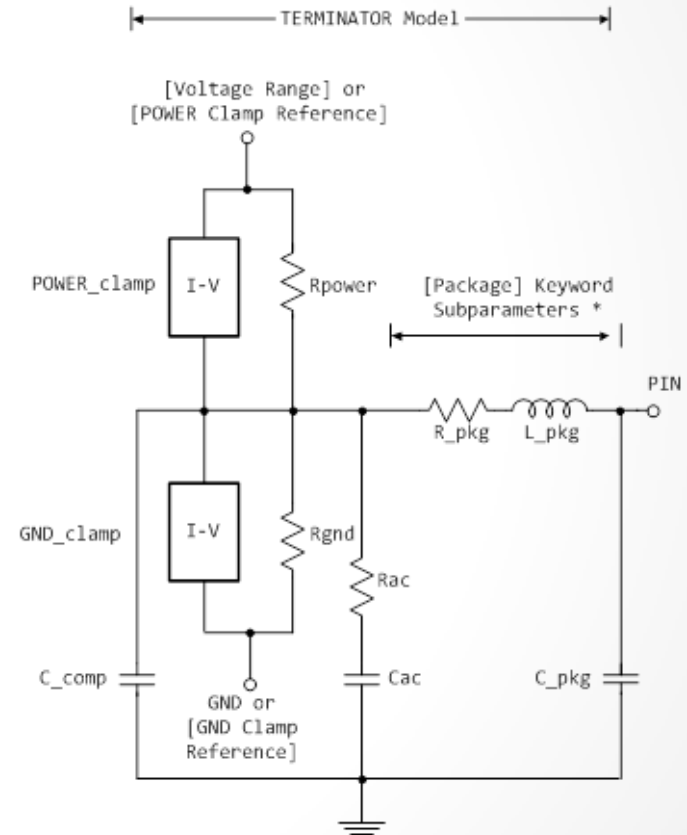
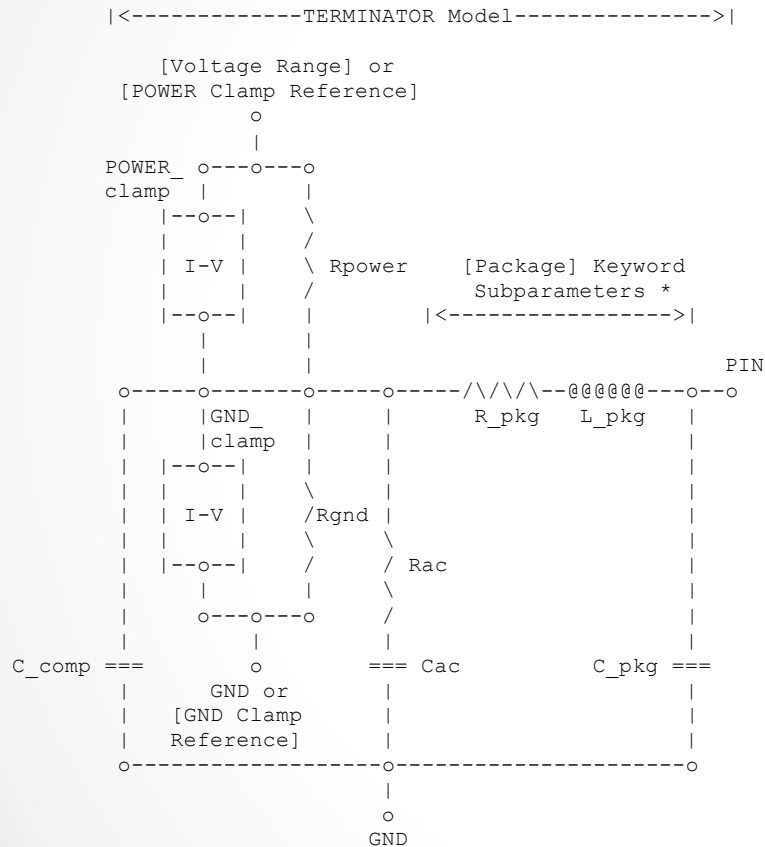


Reference [Model] Terminals

- Show all four terminals
- C_comp to GND
- Note, Terminator [Rac], [Cac] also goes to GND; no other option available without new keywords
- C_comp never intended to be only a connection to gnd_clamp_ref or pulldown_ref terminal
- C_comp_* and general C_comp subckt resolves many issues



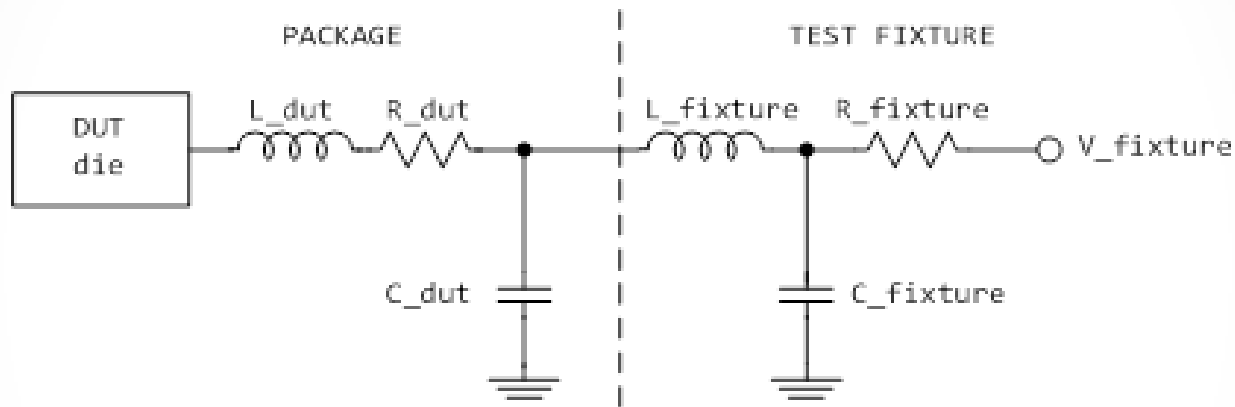
Terminator [Model] “ground” in IBIS 5.0 and 6.1 Figure 11



* Note: More advanced package parameters are available within this standard, including more detailed power and ground net descriptions.



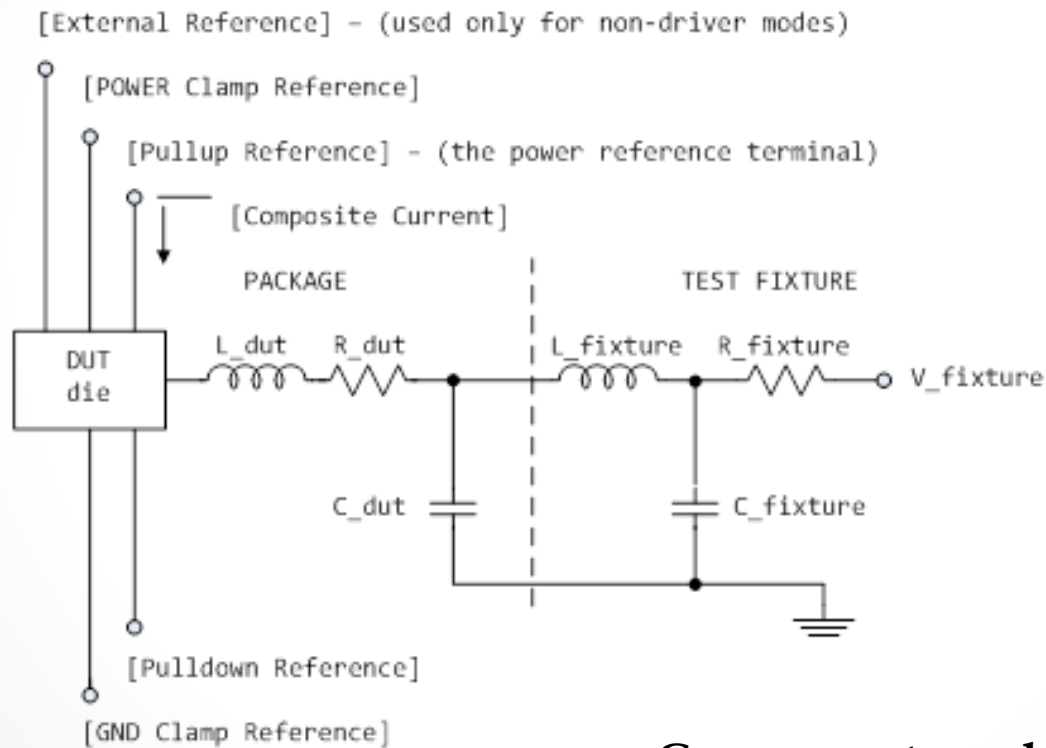
Figure 15 – Extraction Setup with [* Waveform] Subparameters



C_{comp} is embedded in DUT die and goes to all rails; DUT assumes no package ($*_{dut}$ provides approximate package if physical measurement is made, but this feature is NOT recommended)



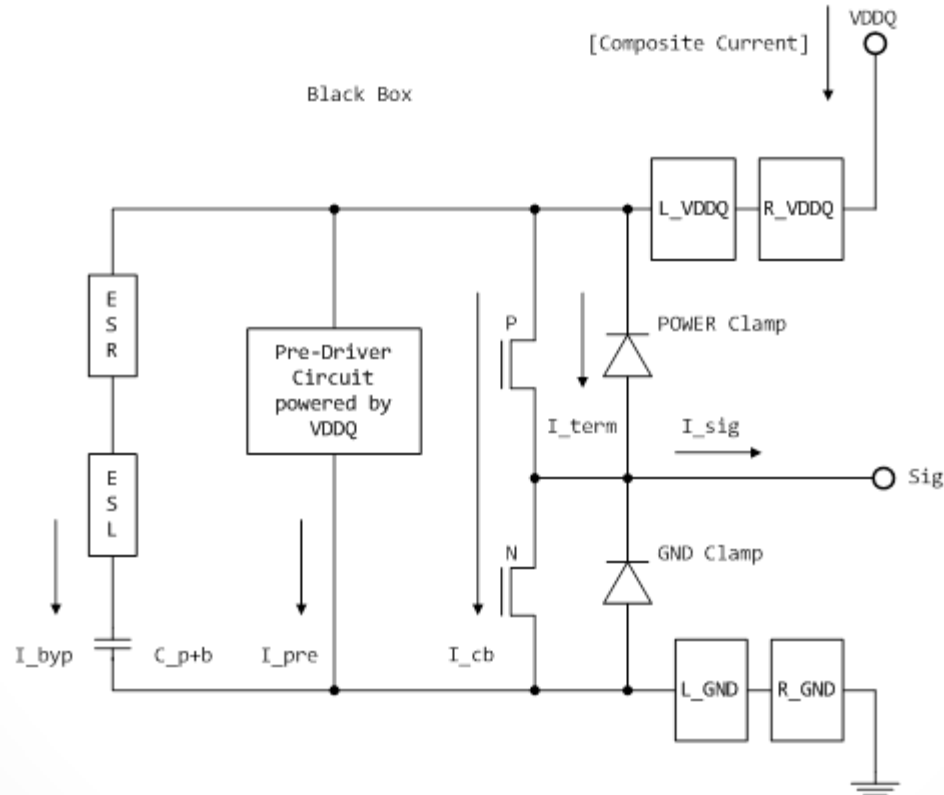
Figure 16 - Extraction Setup Showing [Composite Current]



C_{comp} not needed



Figure 17 – Internal Currents with [Composite Current]



EDA Tool Reference [Model]s for Simulation

- **Four rails**
- **C_comp to GND**
- **Split C_comp options available, with, without I-V tables**
- **Not shown - reference models supporting all other Model_types (e.g., ECL, Open_drain, Open_source, Terminators, Differential models, etc.)**
- **IBIS should not change its reference model (tools will not change)**



IBIS I/O [Model]s in EDA Tools

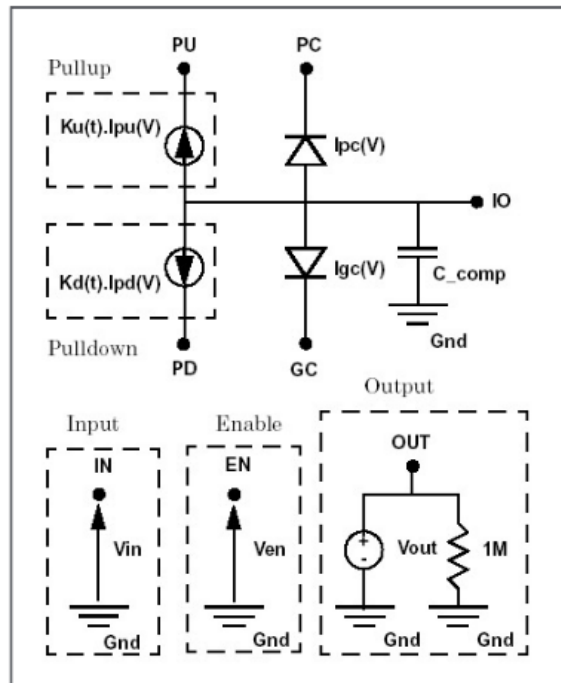
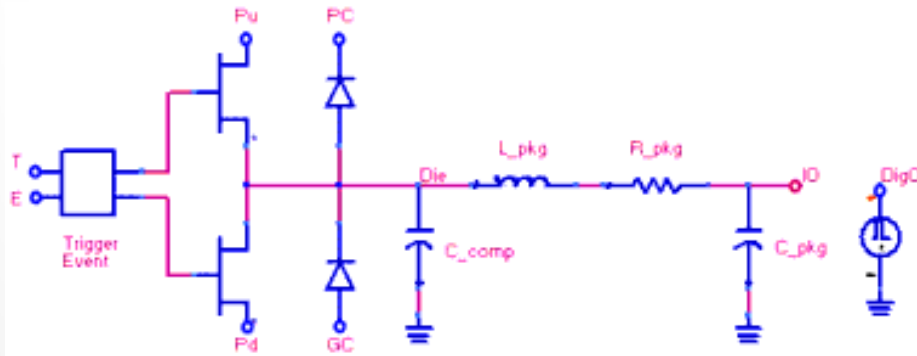
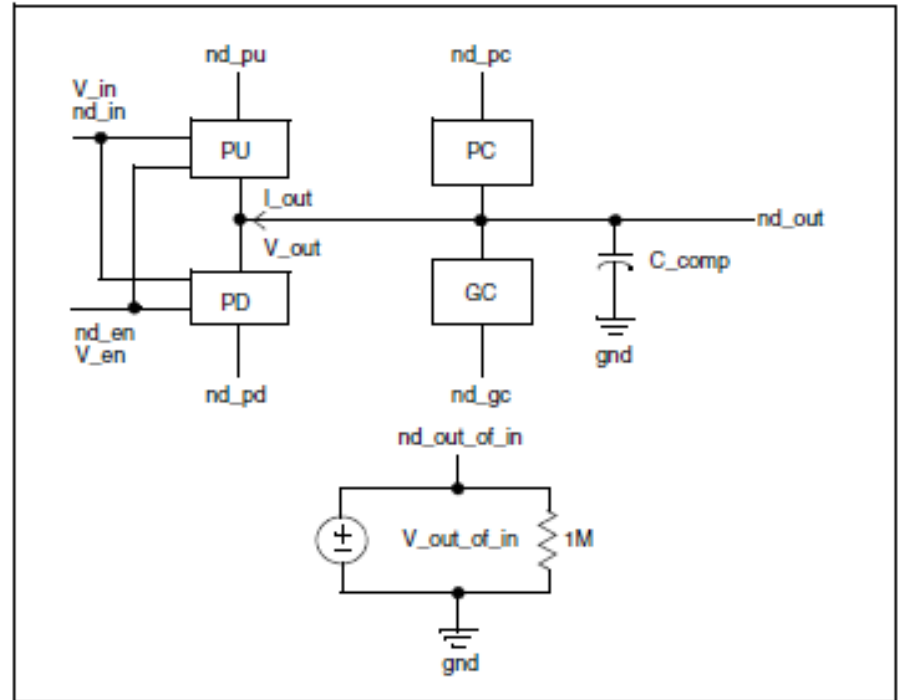


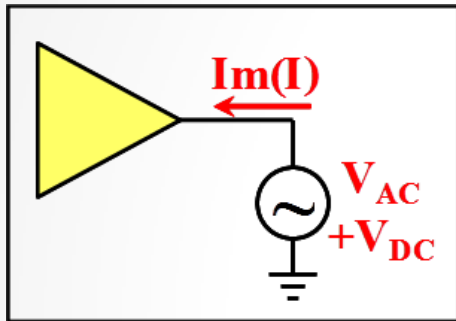
Figure 1. IBIS Buffer General Circuit Diagram.



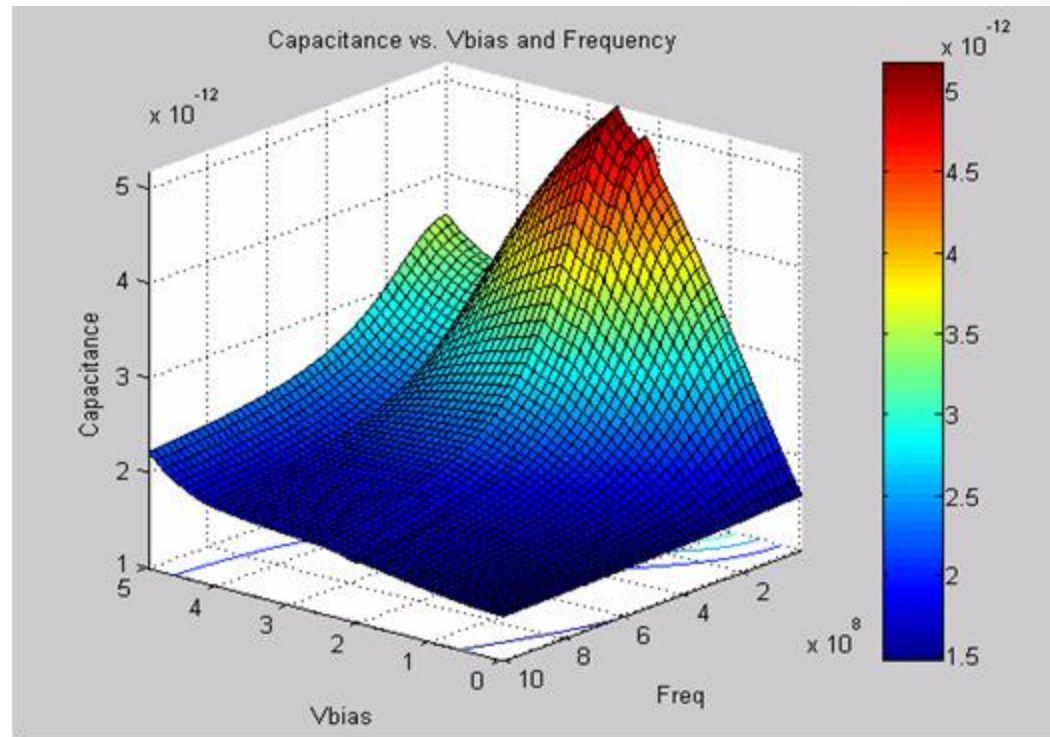
Includes default *_pkg



C_comp NOT Constant, See IBIS Cookbook Plot



$$C_{\text{comp}} = -\text{Im}(I_{AC}) / (2 * \pi * f * V_{AC}),$$

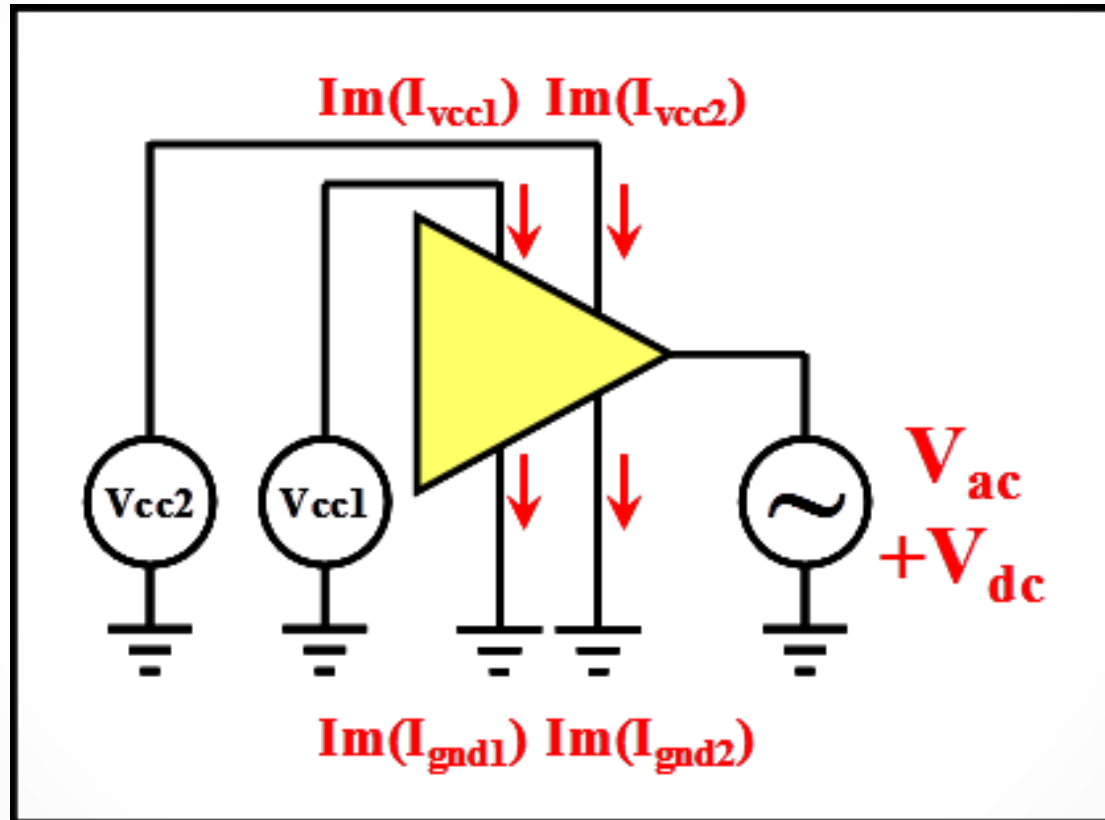


Four extraction methods mentioned that probably give different results

Total C_{comp} to all terminals (AC short)



Split C_comp Extraction Method in IBIS Cookbook

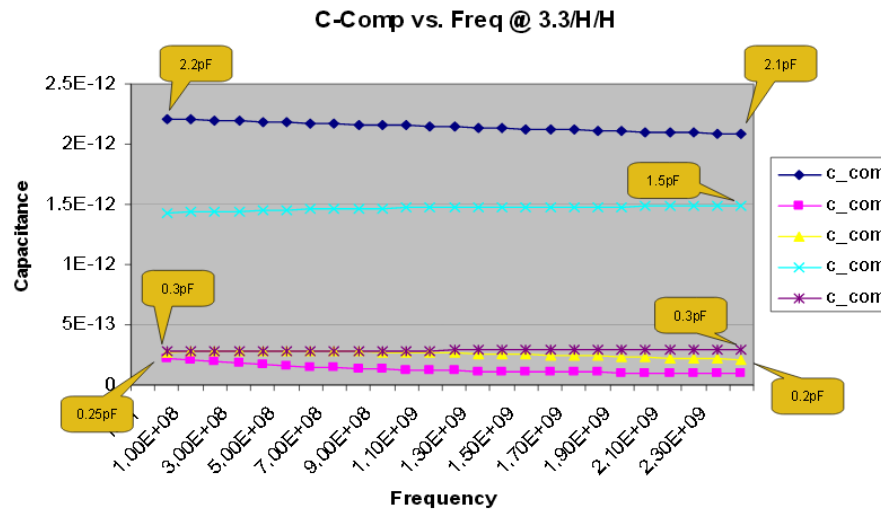


Split C_comp Results 1

C_comp_gc or C_comp_pd can be small percentage of C_comp

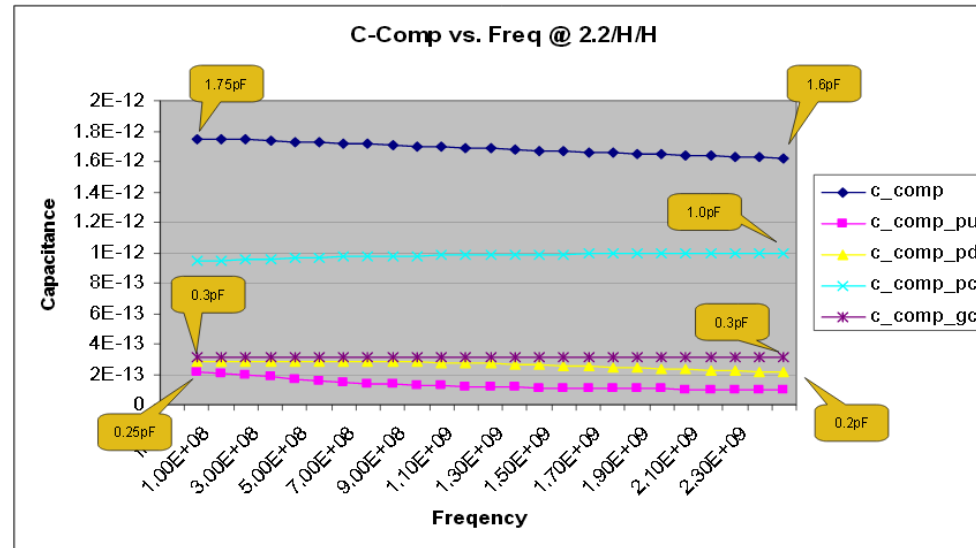
Pad DC = 3.3v

Driving mode = Disabled



Pad DC = 2.2v

Driving mode = Disabled

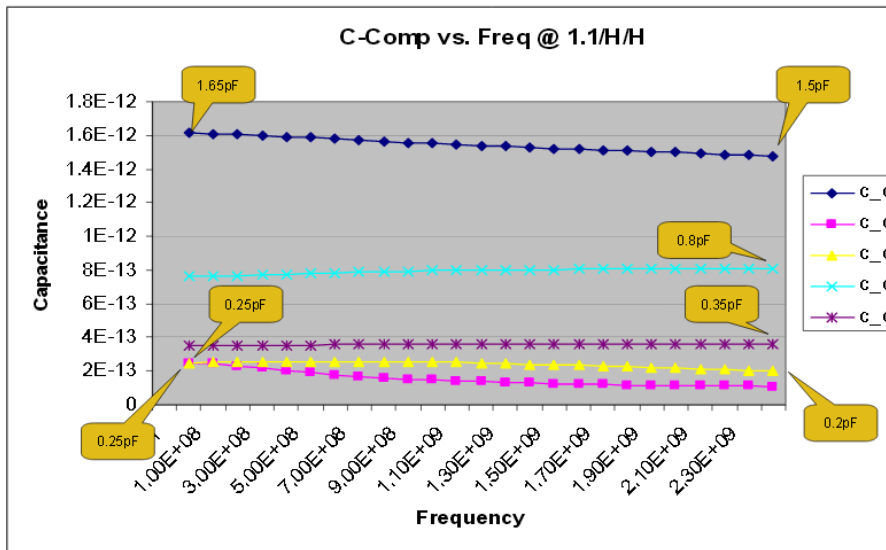


Lance Wang, "C-comp Extraction Methods for High-Speed I/O Buffers", Asian IBIS Summit (Tokyo), November 6, 2009
<http://www.ibis.org/summits/nov09b/wang.pdf>

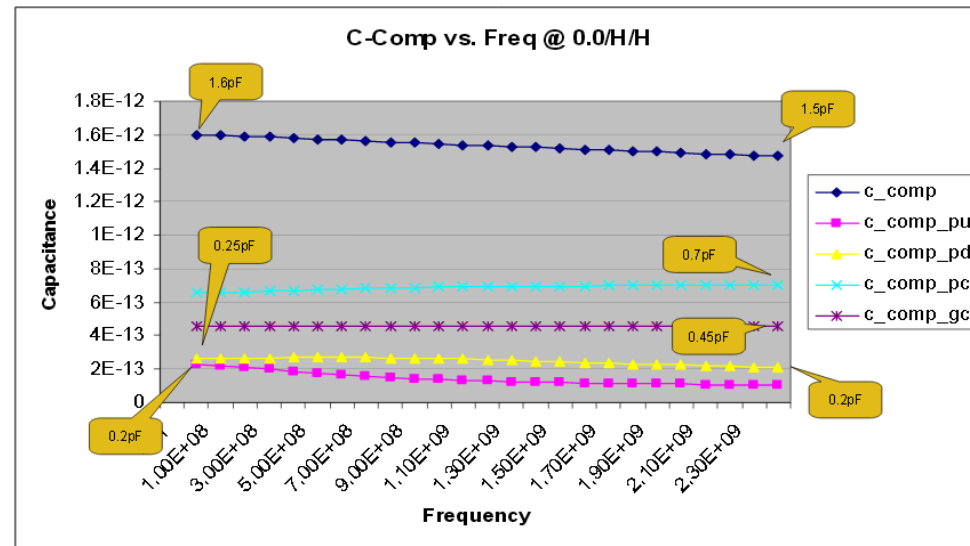


Split C_comp – Results 2

Pad DC = 1.1v
Driving mode = Disabled



Pad DC = 0.0v
Driving mode = Disabled



Also, similar results in Lance Wang, "More on C_comp", European IBIS Summit, Hildesheim, Germany, May 12, 2010, <http://www.ibis.org/summits/may10/wang.pdf>



IBIS [Model] Extraction

- **From simulation model (e.g., SPICE model)**
 - Remove package
 - Discussed in IBIS, Section 9, and in Cookbook
 - S2ibis used to create test decks
- **From measurement**
 - Process requires advanced equipment and skills
 - Create 2-layer or 4-layer test board with many more rail decoupling capacitors than economically practical in actual multilayer (up to 20 layers) designs with SMA's and launch via designs, etc.
 - Requires programmable supplies for rails and programmable stimulus to active drivers internally (e.g., set up internal registers for fixed buffer states or for switching the buffer states)
 - TDR extraction for C_comp based on reflection at die location
 - Post-processing (I-V extrapolation, response cleanup, adjustments)
 - Details outside the scope of IBIS

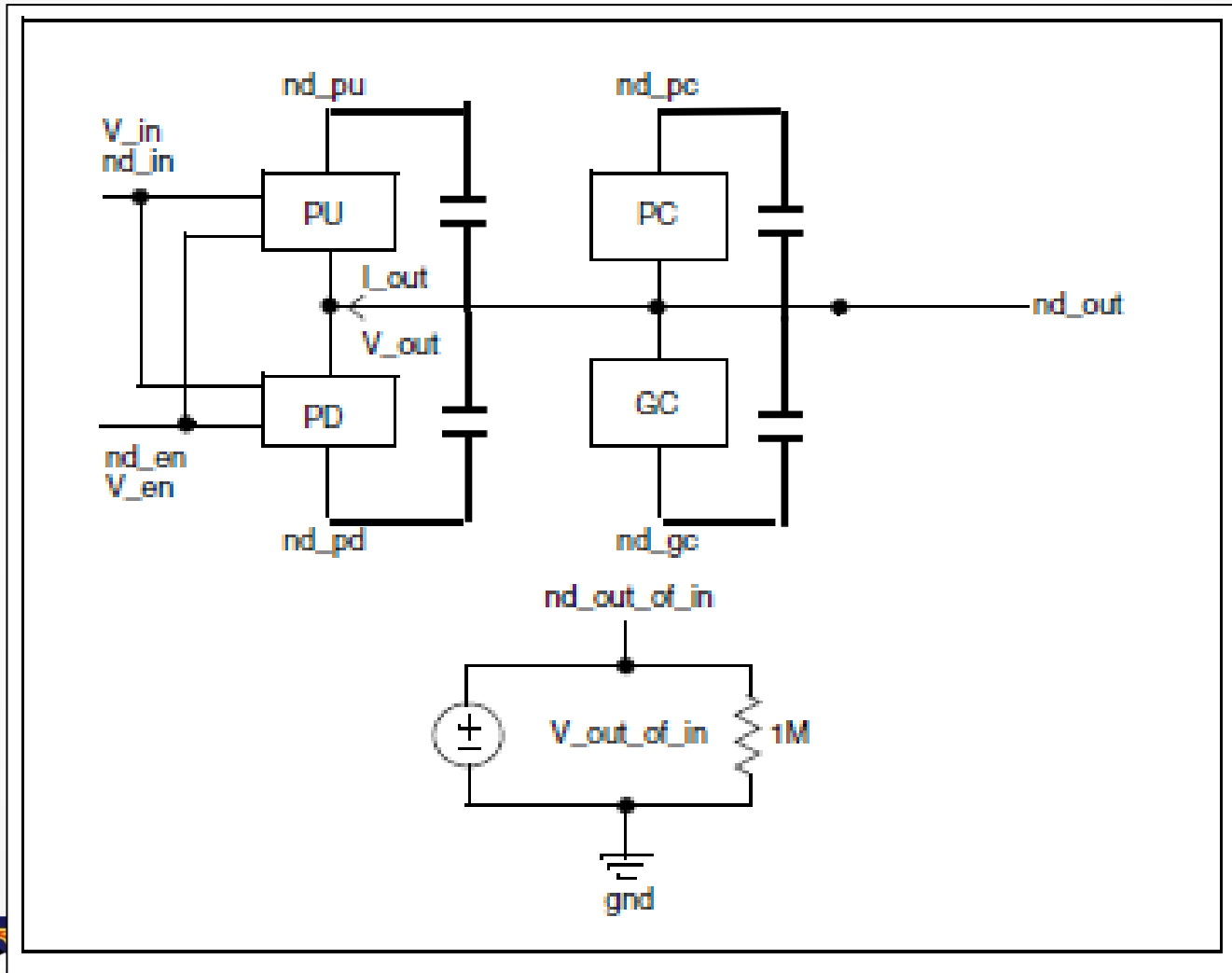


EDA Tool IBIS Model Simulation

- Well understood by EDA tools
- Tools may have vendor-differentiation approaches such as
 - Including pkg in their IBIS element
 - Automatically split C_comp?
- No one approach is “correct”
- Models with elements to GND probably not suitable for power aware analysis



General IBIS I/O [Model]



Recommendations

- Reference model expanded from Figure 11 with C_comp to GND and four terminals
- State “not recommended for power aware analysis”
- Add new reference model with C_comp_* connections for power aware analysis and in new C_comp subckt
- Note that IBIS model extraction from reference simulation model (e.g., SPICE model) assumes that package circuitry is removed
- Extraction details in IBIS Cookbook should focus mostly on simulation model extractions
- Physical measurement extraction information outside scope of IBIS or even the Cookbook

