Modeling and Simulation Interface for Memory Channels

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AMI Extension: Init

- Function arguments

  Input: rise and fall impulse/step responses

  Tx output: Tx EQ

  Rx output: Rx linear EQ, Rx DFE

- Crosstalk impulse/step responses are not needed in the signature
- Rx DLL is expected to determine static Vref for DFE slicer
- How to model Vref that is shared among a byte lane in a real system? Or it can be ignored?
- How to model controller's control on Vref in a real system? Or it can be ignored?
- Need CM DC bias if we want Rx to determine Vref
- What is the DC bias at the Rx input in the presence of Tx EQ? Given an arbitrary Tx EQ impulse, we don't necessarily know its impact on DC, unless it's in the form of FIR
- Need to clarify how Rx DFE is aligned with step responses
- More radical overhaul: split Init into multiple functions for memory allocation, optimization, time-domain and statistical domain, etc.

AMI Extension: GetWave

- Function arguments

  signal waveform (input and output)

  reference clock waveform (input)

- DLL uses the input clock waveform to clock DFE if needed
- Need to inform DLL whether the waveform is in READ or WRITE cycle so that DLL can derive proper DFE switching times from clock waveform
- Reference clock waveform is differential
- DQS and CA don’t use reference clock. Do we need different GetWave signatures for DQ, DQS and CA?
- DQ signal is single-ended, and DQS signal is differential. Do we need different signal waveform definitions for DQ and DQS GetWave functions?
- What is the digital stimulus to Tx DLL? 0/1 for single-ended and +/-0.5 for differential? Do we need to define different stimulus types for single-ended and differential?
- Need to clarify the relation between Tx GetWave output and channel output (Rx input)
- Can Tx GetWave be eliminated?

Beyond AMI: Component Centric Model

- All DQ, DQS, CA, CLK signals are handled in a single DLL
- A single Init function handles impulse/step responses of all signals
- A single GetWave function handles all signal waveforms, including single-ended and differential
- Tx DLL takes single-ended and differential stimuli for different signals
- No need for reference clock waveform in GetWave
- Vref can be shared naturally within a byte lane
- Increases model complexity
- May force all signal to be simulated even if user is only interested on a subset of the signals
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Beyond AMI

- Do we need to confine our options to the AMI framework?
- Essentials

  common modeling interface (model interoperability and portability)

  IP protection

  channel simulation speed (support both statistical and time-domain analyses)