GDDR6X Introduction

IBIS ATM Task Group

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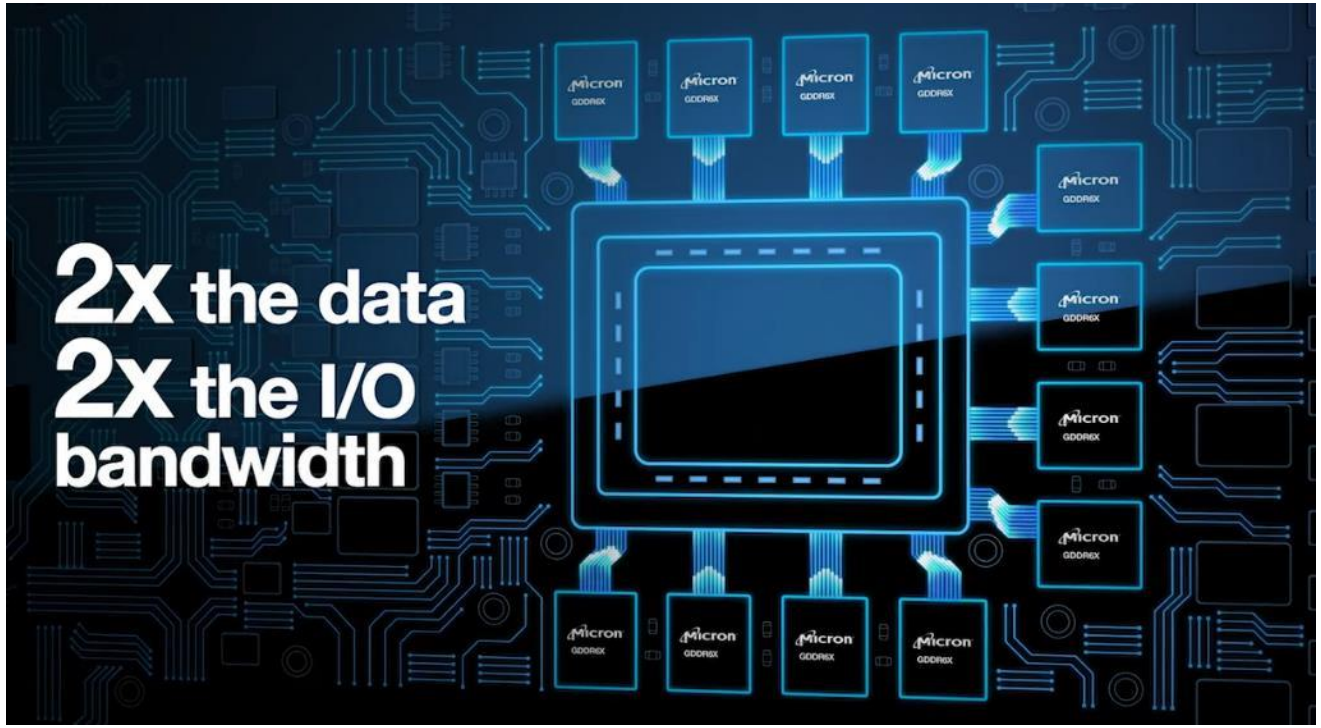
What's New?

- Micron introduced new Graphics DDR memory – GDDR6X
  - https://www.micron.com/products/ultra-bandwidth-solutions/gddr6x
  - Micron Technical Brief
- First use of single-ended PAM4 I/O signaling
- Pushes single-ended I/O speeds beyond 16 Gb/s, targeting up to 32 Gb/s



PAM4 Benefit – Beyond 16 Gb/s

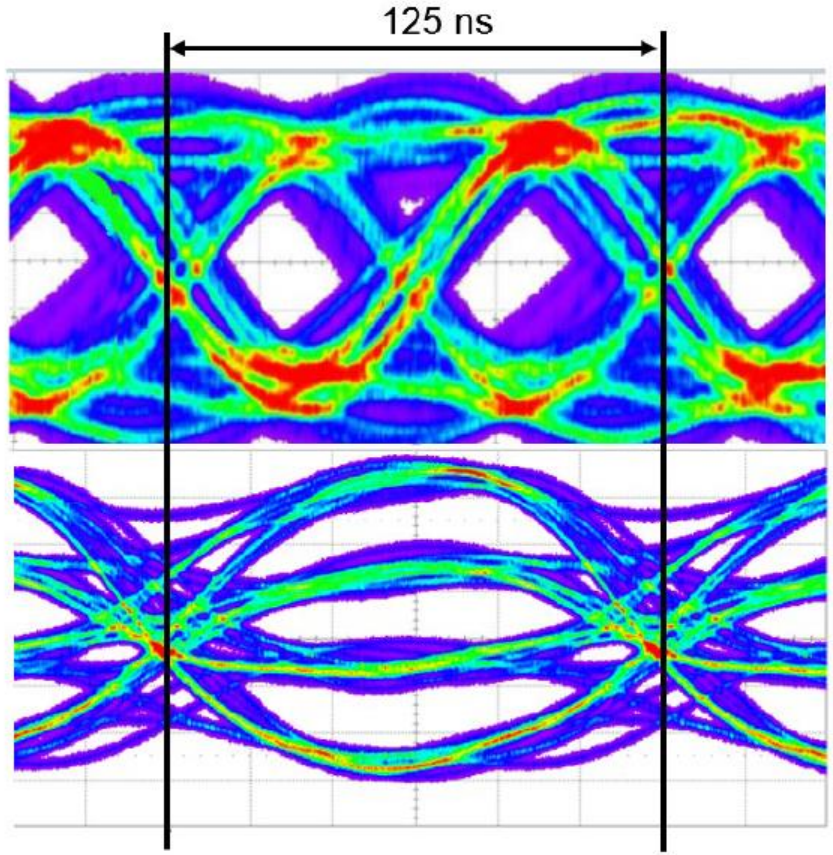
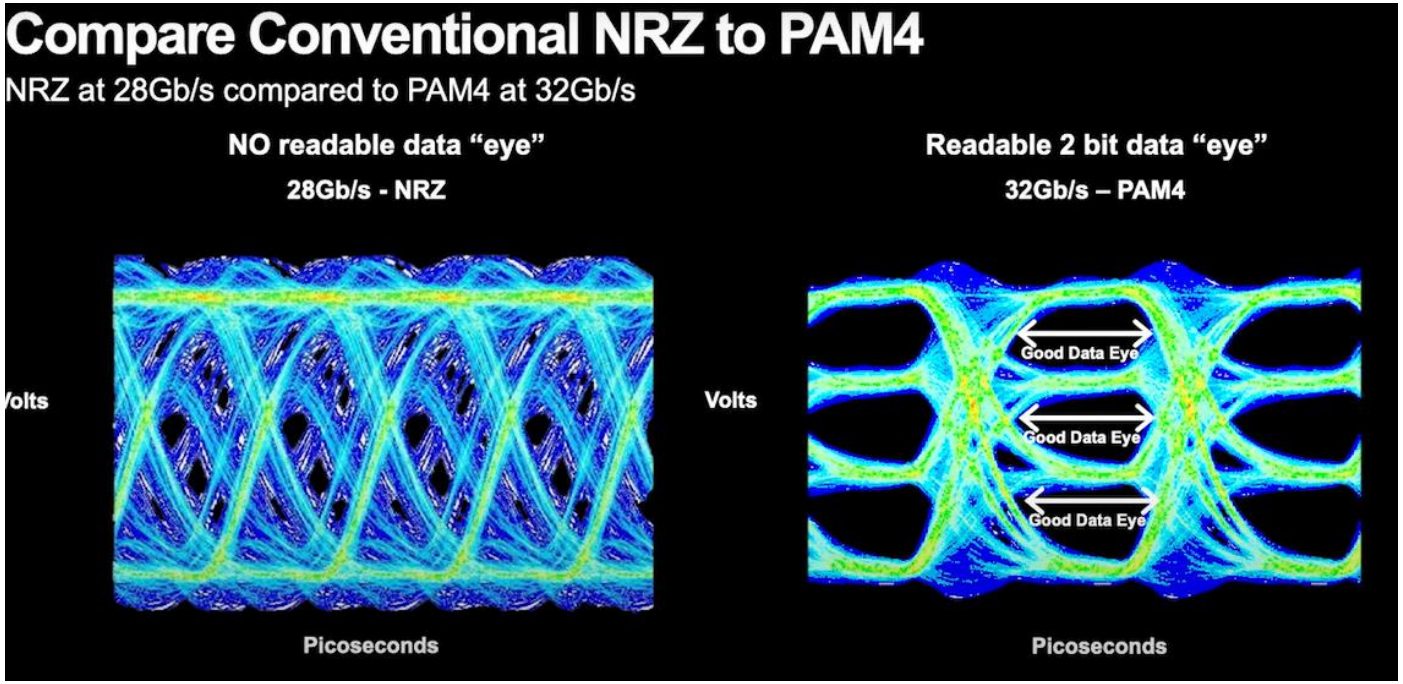


Figure 2: Data Eye Comparison Between GDDR6 (top) and GDDR6X (bottom) That Shows the Timing for a 2 Bits Data Transfer at 16Gb/s



Tx/Rx Specs

- Tx/Rx Equalization
- VDD/VDDQ @ 1.25V or 1.35V
- Datarate (today): 19Gb/s, 21 Gb/s, >21 Gb/s (per pin)
- Data is gray-coded
- V_{REFD} level internal per pin (64 steps), 3 sub-receivers per pin
- 40/48 Ohm ODT

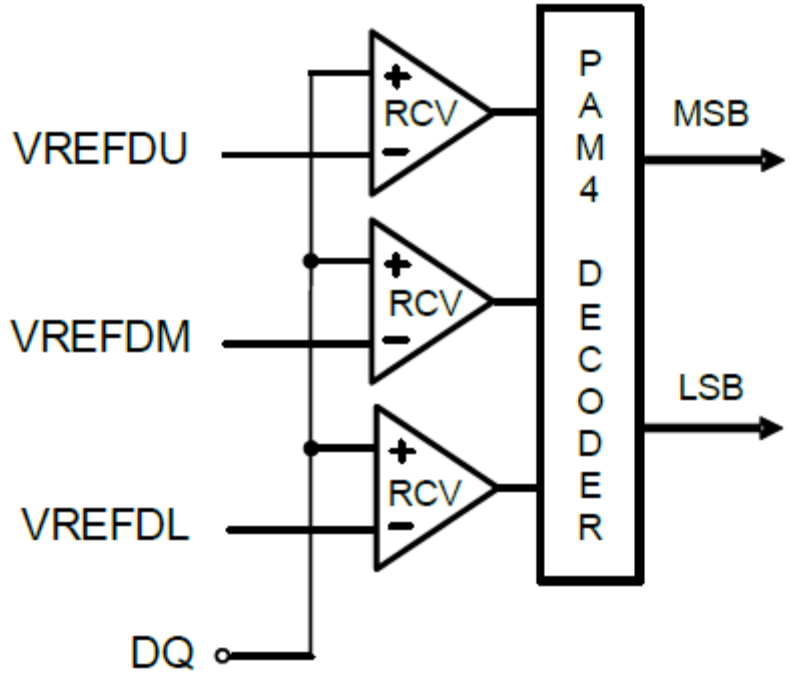


Figure 4: PAM4 Receiver

Tx Impedances

- Tx implemented with 60/120 Ohm PU/PD legs

Logical	Symbol	Physical
10	+3	
11	+1	
01	-1	
00	-3	

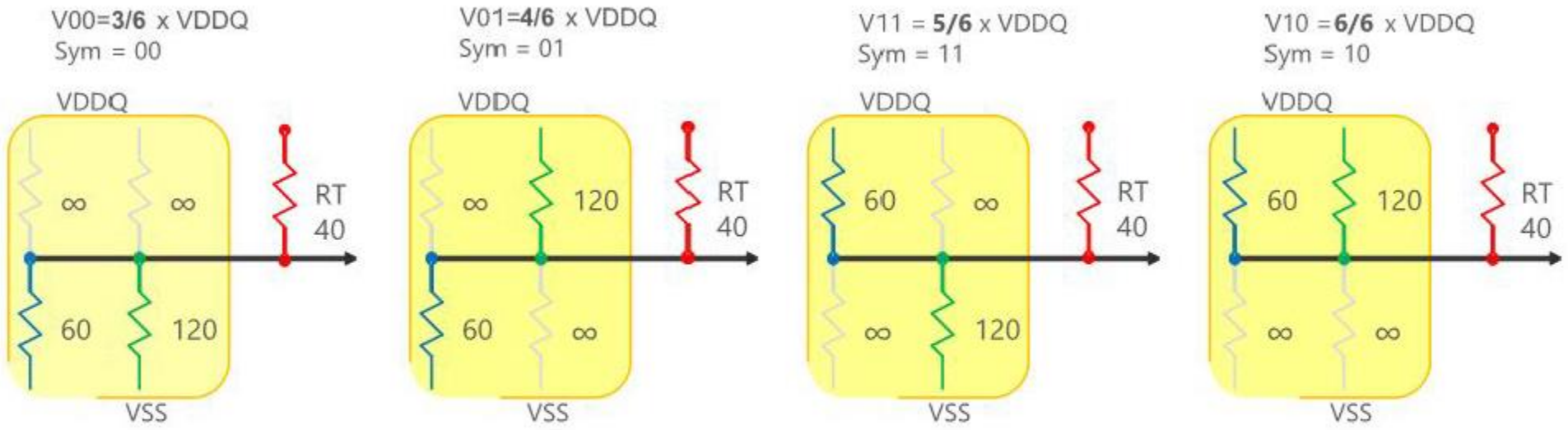
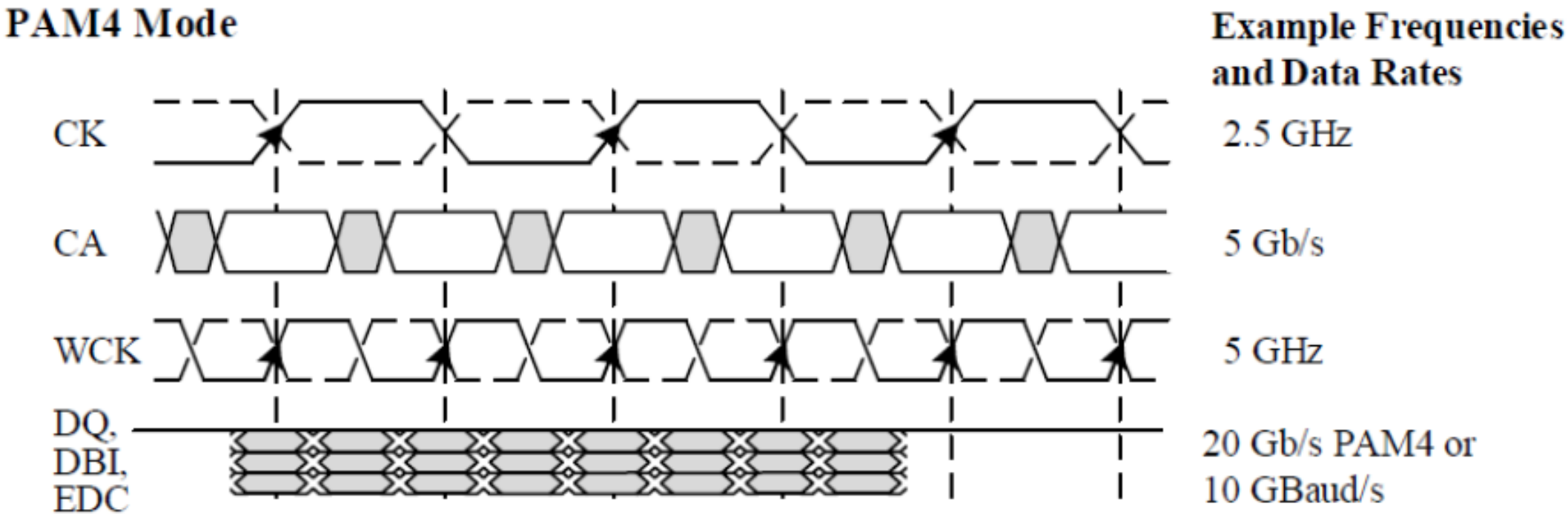


Figure 5: PAM4 Impedance Scheme

Clocking


PAM4 Mode
Example Frequencies and Data Rates
CK
2.5 GHz
CA
5 Gb/s
WCK
5 GHz
DQ, DBI, EDC
20 Gb/s PAM4 or 10 GBaud/s

What is needed from IBIS?

- IBIS
  - New Model_Types (I/O_PAM4, Input_PAM4, Output_PAM4)
    - MSB/LSB input stimuli
    - Multiple Pullup/Pulldown curves
    - 6 sets of V-t waveforms
    - [Driver Schedule]-like architecture?

- IBIS-AMI
  - EDA tools will need to support new IBIS buffer model for time-domain channel characterization
    - Multiple edge responses (more than single rise/fall edges)
    - Multiple bit responses for superposition techniques
  - PAM4_*Threshold levels are V_{REFD} levels. How to set these?
  - Any special handling of DC_Offset?
  - Revamp of IBIS Section 10.7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