**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 220.1

**ISSUE TITLE:** Pre-driver PSIJ Keyword

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**DATE REVISED:**

**DATE ACCEPTED:**

**DEFINITION OF THE ISSUE:**

Currently, power-aware IBIS models cannot account for pre-driver delay variations caused by power rail voltage noise. While the gate modulation effect is included, it is only a function of the power rail voltage variations at the final driver. Thus, the current model does not fully represent the timing jitter due to power rail noise, since the buffer’s propagation delay is also affected by the pre-driver stage.

To account for the pre-driver delay variations due to power rail noise, two new keywords [PreDrv PSIJ Rising\_edge] and [PreDrv PSIJ Falling\_edge] are proposed for a more accurate power supply induced jitter (PSIJ) simulation. IBIS summit presentations and papers (see references) show that utilizing the driver jitter sensitivity extracted with DC power supply voltage noise in the process of modifying the and coefficients can improve the PSIJ simulation accuracy. [PreDrv PSIJ Rising\_edge] and [PreDrv PSIJ Falling\_edge] will provide information on the driver DC jitter sensitivity for both rising and falling edges.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table : Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Provide the pre-driver output rising and falling edge DC PSIJ in s.
 |  |
| 1. The pre-driver should be in the same power domain as the buffer defined in the corresponding [Model].
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**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table : IBIS Keywords, Subparameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
| [PreDrv PSIJ Rising\_edge] and [PreDrv PSIJ Falling\_edge] | New |  |

**PROPOSED CHANGES:**

All page numbers refer to the PDF version of IBIS Version 7.2.

In IBIS version 7.2, insert the [PreDrv PSIJ Rising\_edge] and [PreDrv PSIJ Falling\_edge] keywords after the [Initial Delay] keyword on page 114.

*Keyword:* **[PreDrv PSIJ Rising\_edge] and [PreDrv PSIJ Falling\_edge]**

*Required:* No

*Description:* Used to describe the pre-driver output rising and falling edge DC power supply-induced jitter (PSIJ) related to the DC voltage variations between the Pullup\_ref and Pulldown\_ref terminals of a [Model]. Pre-driver DC PSIJ refers to the impact of DC power noise presents on the pre-driver’s power rail, on the overall driver output—an effect not captured in the IBIS model. The pre-driver PSIJ, extracted under different DC voltage deviations between the Pullup\_ref and Pulldown\_ref terminals, should be provided in the keyword table. Although the jitter in the keyword table is based on DC voltage deviations, the modified algorithm using this keyword can also predict driver behavior under AC noise conditions.

*Sub-Params:* NA

*Usage Rules:* The [PreDrv PSIJ Rising\_edge] and [PreDrv PSIJ Falling\_edge] keywords can be specified to consider the pre-driver PSIJ effect. Applying the DC power noise on the pre-driver stages while keeping the final driver power supply unchanged, the PSIJ measured at the final driver output reflects the pre-driver DC PSIJ. To ensure accuracy, this pre-driver DC PSIJ must be measured under the same load conditions as expected in the application. If the load conditions differ, the model’s accuracy cannot be guaranteed.

The pre-driver DC PSIJ contains both magnitude and polarity information, so the value entered could be either positive or negative. The pre-driver DC PSIJ within a large power supply voltage range could be included to capture the non-linear behavior.

Under each keyword, the first column indicates the power supply voltage deviation from the typical, minimum, and maximum voltage. The remaining three columns contain the typical, minimum, and maximum pre-driver DC PSIJ values. For the same voltage deviation, the entries of typical, minimum, and maximum must be placed on a single line, separated by at least one whitespace character. All four columns are required under each keyword. However, data is required only in the typical column. If minimum and/or maximum values are not available, the reserved word “NA” must be used to indicate the typical value by default. One keyword can be omitted if the DC jitter for the rising edge and falling edge are identical. During the modification process, the corresponding pre-driver jitter value is selected from the keyword table based on the time-averaged power noise during the driver’s propagation delay, and this value is then used to modify the switching coefficients.

The minimum and maximum values are used for specifying keyword values that track the min and max operating conditions of the [Model].

*Other Notes:* For the model implementation in simulation, the buffer transition behavior is mainly described by the and switching coefficients.

See Figure 21. To improve PSIJ simulation accuracy, the switching coefficients are modified as a function of the time-averaged power rail voltage noise and the pre-driver DC jitter.

The time-averaged power rail voltage noise is calculated with respect to the input switching events and is written as follows:

where

 is the elapsed time between the last input switching event and the current simulation time point,

 is the actual power rail voltage,

 is the ideal power rail voltage.

The pre-driver DC jitter at the current simulation time point is obtained from the keyword table according to the time-averaged power rail voltage noise, and can be written as .

The and switching coefficients are thus modified as:

where

 and are the and coefficients for the ideal power supply voltage case,

 is the elapsed time between the last input switching event and the current simulation time point,

 is the pre-driver PSIJ which can be obtained from the data provided in the [PreDrv PSIJ Rising\_edge] and [PreDrv PSIJ Falling\_edge] keywords,

 is the time-averaged power rail noise.

The information in [PreDrv PSIJ Rising\_edge] and [PreDrv PSIJ Falling\_edge] is applied by the above equations to the switching coefficients and , ultimately impacting the delay seen in the final output waveform

The and coefficients for the typical case and can be solved using the two equations and two unknowns’ algorithm under two different driver output voltage conditions:

The process of rising edge and falling edge and modification is identical.



**Figure 21 – Output Buffer in Simulation**

*Example:*

[PreDrv PSIJ Rising\_edge] |unit(s)

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|Voltage Deviation typ min max

|

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| ·

-0.2V 25p 26p 24p

-0.15V 18p 18.5p 17.5p

-0.1V 11p 12p 10p

-0.05V 5p 6p 4p

0V 0p 0p 0p

0.05V -4p -5p -3p

0.1V -8p -10p -7p

0.15V -11p -12p -10p

0.2V -15p -16p -14p

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[PreDrv PSIJ Falling\_edge] |unit(s)

|

|Voltage Deviation typ min max

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| ·

| ·

-0.2V 13p NA NA

-0.15V 8p NA NA

-0.1V 5p NA NA

-0.05V 2p NA NA

0V 0p NA NA

0.05V -0.8p NA NA

0.1V -1p NA NA

0.15V -1.5p NA NA

0.2V -2p NA NA

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**BACKGROUND INFORMATION/HISTORY:**

The concept and needs of including pre-driver PSIJ sensitivity were presented and discussed at several ATM meetings. Also, the concept and an example algorithm to simulate the timing variation using the proposed keyword were presented in the IBIS Summits at the IEEE Virtual Symposium on EMC+SIPI in 2020, 2021, 2022 and 2024.

[1] Y. Ding, R. Wolff, Z. Yang, and C. Hwang, “[Updates on BIRD220 (Improved Power Supply Induced Jitter Model for IBIS simulation)](https://ibis.org/summits/aug24/ding.pdf),” IBIS Summit at 2024 IEEE Symposium on EMC+SIPI, August 2024.

[2] Y. Ding, Y. Sun, R. Wolff, Z. Yang and C. Hwang, "[IBIS Model Simulation Accuracy Improvement by Including Power-Supply-Induced Jitter Effect](https://ieeexplore.ieee.org/document/10380728)," in IEEE Transactions on Signal and Power Integrity, vol. 3, pp. 21-29, 2024, doi: 10.1109/TSIPI.2023.3349229.

[3] Y. Ding, Y. Sun, R. Wolff, Z. Yang, and C. Hwang, “[IBIS Model Simulation Accuracy Improvement by Including PSIJ Effect](https://ibis.org/summits/aug22/),” IBIS Summit at 2022 IEEE Symposium on EMC+SIPI, August 2022.

[4] Y. Sun and C. Hwang, “[Improving Power Supply Induced Jitter Simulation Accuracy for IBIS Model](https://ibis.org/summits/aug20/sun.pdf),” IBIS Summit at 2020 IEEE Virtual Symposium on EMC+SIPI, August 2020.

[5] Y. Ding, Y. Sun, Z. Yang and C. Hwang, “[New Way to Improve Power Supply Induced Jitter Simulation Accuracy for IBIS Model](https://ibis.org/summits/aug21a/),” IBIS Summit at 2021 IEEE Virtual symposium on EMC+SIPI, August 2021.

[6] Y. Sun, J. Lee and C. Hwang, "[A Generalized Power Supply Induced Jitter Model Based on Power Supply Rejection Ratio Response](https://ieeexplore.ieee.org/document/9416294)," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 6, pp. 1052-1060, June 2021, doi: 10.1109/TVLSI.2021.3072799.

[7] Y. Sun and C. Hwang, “[Improving Power Supply Induced Jitter Simulation Accuracy for IBIS Model](https://ieeexplore.ieee.org/document/9559139),” 2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium, 2021, pp. 1127-1132, doi: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559139.

[8] R. Wolff, “[Output Buffer PSIJ Analysis](https://ibis.org/atm_wip/archive/20211026/randywolff/Output%20Buffer%20PSIJ%20Analysis/Micron_PSIJ_Analysis_for_IBIS_ATM.pdf),” IBIS ATM Task Group Meeting, October 2021.