**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 220

**ISSUE TITLE:** Pre-driver PSIJ Sensitivity Keyword

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**DATE ACCEPTED:**

**DEFINITION OF THE ISSUE:**

Currently, the power-aware IBIS model cannot account for pre-driver delay changes caused by power rail voltage noise. The gate modulation effect is considered but as only a function of power rail voltage at the final driver. Thus, the current model does not fully represent the timing jitter correctly due to power rail noise, since the propagation delay change is also affected by the pre-driver stage.

To account for the pre-driver delay change due to power rail noise, a new keyword [Pre-driver PSIJ Sensitivity] is proposed for more accurate power supply induced jitter (PSIJ) simulation. IBIS summit presentations and papers (see references) show that utilizing the driver DC jitter sensitivity in the process of modifying the Ku/Kd coefficients can improve the PSIJ simulation accuracy. [Pre-driver PSIJ Sensitivity] will provide the information on the driver DC jitter sensitivity for both rising and falling edges.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table : Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Provide the pre-driver output rising and falling edge DC PSIJ sensitivity in s/V. |  |
| 1. The pre-driver should be in the same power domain as the buffer defined in the corresponding [Model]. |  |

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table : IBIS Keywords, Subparameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
| [Pre-driver PSIJ Sensitivity] | New |  |
| “Rising\_edge” and “Falling\_edge” sub-parameters under [Pre-driver PSIJ Sensitivity] | New |  |

**PROPOSED CHANGES:**

All page numbers refer to the PDF version of IBIS Version 7.1.

In IBIS version 7.1, insert the [Pre-driver PSIJ sensitivity] keyword after the [Initial Delay] keyword on page 114.

*Keyword:* **[Pre-driver PSIJ Sensitivity]**

*Required:* No

*Description:* Used to describe the pre-driver output rising and falling edge DC power supply-induced jitter (PSIJ) sensitivity related to the changes in voltage of the Pullup\_ref terminal of a [Model].

*Sub-Params:* Rising\_edge, Falling\_edge

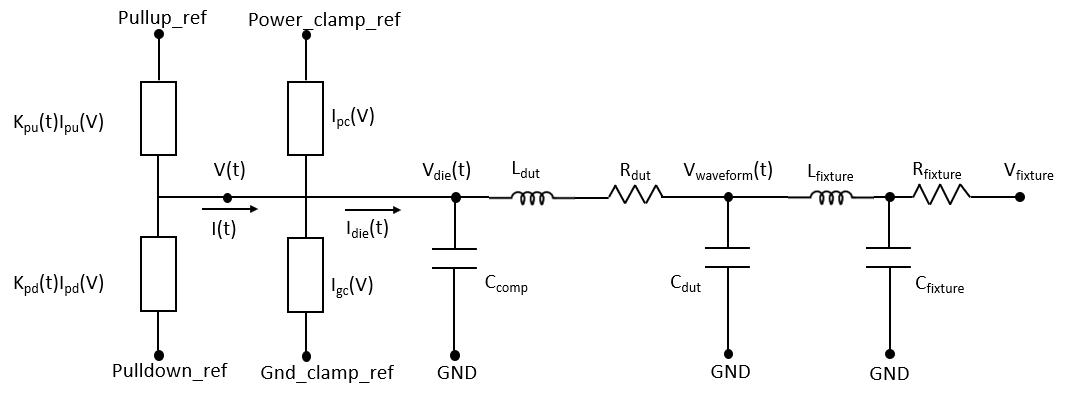
*Usage Rules:* The [Pre-driver PSIJ Sensitivity] keyword can be specified when the effect from the pre-driver should be considered in the model simulation. The DC PSIJ sensitivity contains both magnitude and polarity information, so the value entered could be either positive or negative.

For each subparameter contained in the first column, the remaining three hold its typical, minimum, and maximum values. The entries of typical, minimum, and maximum must be placed on a single line and must be separated by at least one whitespace character. All four columns are required under the [Pre-driver PSIJ Sensitivity] keyword. However, data are required only in the typical column. If minimum and/or maximum values are not available, the reserved word “NA” must be used to indicate the typical value by default.

The minimum and maximum values are used for specifying subparameter values that track the min and max operation conditions of the [Model].

*Other Notes:* For the model implementation in simulation, the buffer transition behavior is mainly described by the Kpu and Kpd switching coefficients. See Figure 21. To improve PSIJ simulation accuracy, the switching coefficients are modified as a function of time and the averaged power rail voltage as shown in the equations below:

where the and are the Kpu and Kpd coefficients for typical power supply voltage case, and are the linear and quadratic fitting coefficients, respectively, that account for the delay change due to the power rail noise voltage, and is the averaged power supply voltage since the last input switching event.



**Figure 21 – Output Buffer in Simulation**

The 6 unknown coefficients , , , , , and should be extracted before simulation. Steps in the solve process are shown below:

1) The Kpu and Kpd coefficients for typical case and can be solved using the two equations and two unknowns’ algorithm under two different driver output voltage conditions:

2) For the , , , and extraction, the two equations and two unknowns’ algorithm in the following format can be used:

3) are unknown terms in the above equations. To ensure the functions are purely related to the power supply voltage fluctuation and to avoid any effects from the process corners, the jitter sensitivity is introduced in this process to capture the supply voltage effect on delay for maximum and minimum supply voltage cases.

The jitter sensitivity based on the DC jitter sensitivity, the power supply rejection ratio response, and the frequency dependency due to the time averaged effect is given in the equation below:

where

is the DC jitter sensitivity,

is the power supply rejection ratio response,

and is the frequency dependency due to the time averaged effect.

The last term is already considered by taking the average of the Vcc. The second term is less important for the general inverter and inverter chain cases. As a result, only the DC jitter sensitivity is considered.

So, the Kpu/Kpd coefficients for max/min supply voltage cases can be represented by:

The added [Pre-driver PSIJ Sensitivity]information can be used in this process to affect the final output waveform delay change. The can include the pre-driver and actual final driver PSIJ effects while excluding other effects for the final driver such as from gate modulation.

With the jitter sensitivity-based modification, the Kpu/Kpd coefficients for maximum and minimum supply voltage cases can be obtained, and the and coefficients can be solved accordingly. After the modification, the improved model can be simulated.

*Example:*

[Pre-driver PSIJ Sensitivity]

|unit(s/V) typ min max

Rising\_edge 50p 52p 48p

Falling\_edge -40p NA NA

**BACKGROUND INFORMATION/HISTORY:**

The concept and needs of including pre-driver PSIJ sensitivity was presented and discussed at several ATM meetings. Also, the concept and an example algorithm to simulate the timing variation using the proposed keyword was presented in the IBIS Summits at IEEE Virtual Symposium on EMC+SIPI in 2020, 2021, and 2022.

[1] Y. Ding, Y. Sun, R. Wolff, Z. Yang and C. Hwang, “[IBIS Model Simulation Accuracy Improvement by Including PSIJ Effect](https://ibis.org/summits/aug22/),” IBIS Summit at 2022 IEEE Symposium on EMC+SIPI, August 2022.

[2] Y. Sun and C. Hwang, “[Improving Power Supply Induced Jitter Simulation Accuracy for IBIS Model](https://ibis.org/summits/aug20/sun.pdf),” IBIS Summit at 2020 IEEE Virtual Symposium on EMC+SIPI, August 2020.

[3] Y. Ding, Y. Sun, Z. Yang and C. Hwang, “[New Way to Improve Power Supply Induced Jitter Simulation Accuracy for IBIS Model](https://ibis.org/summits/aug21a/),” IBIS Summit at 2021 IEEE Virtual symposium on EMC+SIPI, August 2021.

[4] Y. Sun, J. Lee and C. Hwang, "[A Generalized Power Supply Induced Jitter Model Based on Power Supply Rejection Ratio Response](https://ieeexplore.ieee.org/document/9416294)," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 6, pp. 1052-1060, June 2021, doi: 10.1109/TVLSI.2021.3072799.

[5] Y. Sun and C. Hwang, “[Improving Power Supply Induced Jitter Simulation Accuracy for IBIS Model](https://ieeexplore.ieee.org/document/9559139),” 2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium, 2021, pp. 1127-1132, doi: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559139.

[6] R. Wolff, “[Output Buffer PSIJ Analysis](https://ibis.org/atm_wip/archive/20211026/randywolff/Output%20Buffer%20PSIJ%20Analysis/Micron_PSIJ_Analysis_for_IBIS_ATM.pdf),” IBIS ATM Task Group Meeting, October 2021.