**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER: 198.2**

**ISSUE TITLE:** Keyword Additions for On-Die PDN (Power Distribution Network) Modeling

**REQUESTOR:**  Kazuki Murata; Sony LSI Design Inc.;

Miyoko Goto; Ricoh Co., Ltd.;

Kazuyuki Sakata; Renesas Electronics Corporation;

Kazunori Yamada; Renesas Electronics Corporation;

Kouji Ichikawa; Denso Corporation;

Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation;

Takashi Hasegawa; Sony LSI Design Inc.;

Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.;

Toshiki Kanamoto; Hirosaki University

Megumi Ono; Socionext Inc.

**DATE SUBMITTED:** March 11, 2019

**DATE REVISED:** April 3, 2020, June 23, 2020

**DATE ACCEPTED:**

**DEFINITION OF THE ISSUE:**

To resolve the power-supply noise issue, especially high frequency range, an on-die decoupling capacitor should be taken into account in the simulation. With current IBIS versions, an on-die decoupling capacitance PDN model can be defined by using the keyword [Series Pin Mapping] and “Model\_type Series”.

However, this method seems not to be widely recognized, because the keyword [Series Pin Mapping] and “Model\_type Series” don’t remind one of descriptions of the on-die decoupling capacitance PDN Model. To ease usage of an on-die decoupling capacitance PDN model in the IBIS model, this BIRD proposes to add the new keywords [PDN Domain], [End PDN Domain], [PDN Model], and [End PDN Model] for an on-die decoupling capacitance PDN model.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Provide on-die decoupling capacitor model including series resistance and leakage current |  |
| 1. Describe power terminal and ground terminal at die pad |  |

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table 2: IBIS Keywords, Sub-parameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
| [PDN Domain] and [End PDN Domain] scoped under [Component] | New |  |
| “Signal\_name” and “Bus\_label” sub-parameters under [PDN Domain] | New |  |
| [PDN Model] and [End PDN Model] scoped under [PDN Domain] | New |  |
| “C\_pdn”, “R\_pdn” and “R\_leak” sub-parameters under [PDN Model] | New |  |

**PROPOSED CHANGES:**

All page numbers refer to the PDF version of IBIS Version 7.0.

1. In IBIS version 7.0, insert the [PDN Domain], [End PDN Domain], [PDN Model] and [End PDN Model] keywords after [End Interconnect Model Group] keyword on page 37.

*Keyword:* [PDN Domain]

*Required:* No

*Description:* Marks the beginning of a PDN Domain description that is used to specify two Pad\_Rail terminals connected by an on-die decoupling capacitance PDN model.

*Sub-Params:* Bus\_label, Signal\_name

*Usage Rules:* [PDN Domain] has a single argument, which is the name of the associated PDN Domain. The length of the PDN Domain name shall not exceed 40 characters. Blank characters are not allowed. DomainDomain [Component] may contain zero or more [PDN Domain] keywords (each identified by a unique name).

Each [PDN Domain] keyword shall contain one or more [PDN Model] keywords and two sub-parameters consisting of two Bus\_labels, two Signal\_names, or one Bus\_label and one Signal\_name. See the [PDN Model] keyword section for a description of the content of each PDN Model.

Bus\_label rules:

The Bus\_label sub-parameter is followed by the name of a bus\_label declared in the [Pin], [Pin Mapping], [Bus Label], or [Die Supply Pads] section of the .ibs file. If there are two or more die pads associated with the bus\_label, the die pads shall be considered as shorted only when a PDN Model in the PDN Domain is enabled.

Signal\_name rules:

The Signal\_name sub-parameter is followed by the name of a signal\_name declared in the [Pin] section of the .ibs file. Only a signal\_name associated with POWER or GND can be used. If there are two or more die pads associated with the signal\_name, the die pads shall be considered as shorted. In addition, if there are two or more die pads associated with the signal\_name and the signal\_name is associated with two or more bus\_labels, the die pads shall be considered as shorted only when a PDN Model in the PDN Domain is enabled.

A bus\_label and a signal\_name may appear on more than one entry under different [PDN Domain] keywords. This allows for multiple unique on-die decoupling capacitance PDN models to be placed between any arbitrary Pad\_Rail pair combinations.  It is not permitted to include the same pin in both terminals in a PDN Domain to avoid shorting the two terminals.

Note that it is allowed for two or more PDN Domains to be placed between the same two terminals. In this case, all PDN Domains are connected in parallel in a simulation. However, only one PDN Model from a PDN Domain is used, even though multiple PDN Models can be defined within one [PDN Domain]/[End PDN Domain] keyword section.

Note that it is possible to have a bus\_label or signal\_name listed under the [PDN Domain] keyword that does not have a path to the buffer rail terminals. In this case, the on-die decoupling capacitance PDN models can be used for power integrity (PI) analysis such as core power.

*Example:*

|

| PDN 1

[PDN Domain] PDN\_X

Bus\_label VCC1 | assume the bus\_label VCC1 includes B1 and B2 pins

Signal\_name VSS | assume the signal\_name VSS includes C1 pin

[PDN Model] PDN\_model\_A

…

[End PDN Model]

[End PDN Domain]

| PDN 2

[PDN Domain] PDN\_Y

Signal\_name VCC2 | assume the signal\_name VCC2 includes A1, B1, and B2 pins

Signal\_name VSSA | assume the signal\_name VSSA includes C2 pin

[PDN Model] PDN\_model\_B

…

[End PDN Model]

|

| Note: Bus\_label VCC1 and Signal\_name VCC2 shall not be defined as terminals

| under the same PDN Domain, because B1 and B2 pins are associated with

| both terminals and the terminals are shorted.

|

| Note: Even though A1, B1 and B2 pins are associated with two

| bus\_labels VCC1 and VCC2, these pins are considered as shorted at the die

| pads in a simulation when the PDN Model under PDN\_Y is enabled.

|

| Note: Even though PDN\_Y and PDN\_X have different power terminal names VCC1

| and VCC2, PDN Models in these PDN Domains are shorted together at die power

| pads when the PDN Models under PDN\_X and PDN\_Y are both enabled.

| This is because the power terminal of PDN\_Y is signal\_name VCC2 associated

| with bus\_label VCC1.

|

| Figure: PDN\_X and PDN\_Y

|

| pin(signal\_name) pad(bus\_label)

| A1(VCC2) ---------(VCC2)---------+

| | shorted by PDN\_model in PDN\_Y

| B1(VCC2) ---------(VCC1)+--------+

| | | shorted by PDN\_models in PDN\_X and PDN\_Y

| B2(VCC2) ---------(VCC1)+--------+

| | |

| PDN\_X PDN\_Y

| | |

| C1(VSS) ---------(VSS) + |

| |

| C2(VSSA) ---------(VSSA)---------+

|

[End PDN Domain]

| PDN 3

[PDN Domain] PDN\_for\_VCC1\_MIM

Bus\_label VCC1 | assume the bus\_label VCC1 includes B1 and B2 pins

Signal\_name VSS | assume the signal\_name VSS includes C1 pin

[PDN Model] PDN\_model\_MIM

…

[End PDN Model]

| Note: This [PDN Domain] has the same terminals as PDN\_X. In this case,

| a simulation may contain multiple on-die decoupling capacitance PDN models

| between bus\_label VCC1 and signal\_name VSS when the PDN Models under PDN\_X

| and PDN\_for\_VCC1\_MIM are both enabled.

[End PDN Domain]

*Keyword:* [End PDN Domain]

*Required:* Yes, for each instance of the [PDN Domain] keyword

*Description:* Indicates the end of the PDN Domain data.

*Example:*

[End PDN Domain]

*Keyword:* [PDN Model]

*Required:* Yes, for each instance of the [PDN Domain] keyword

*Description:* Marks the beginning of a PDN Model description that is used to define an on-die decoupling capacitance PDN model consisting of three RC values. These values represent MOS capacitor, MIM capacitor, metal resistance, parasitic RC, leakage current, etc. An on-die decoupling capacitance PDN model connects between the two terminals specified by the [PDN Domain] keyword.

*Sub-Params:* R\_pdn, C\_pdn, R\_leak

*Usage Rules:* [PDN Model] has a single argument, which is the name of the associated PDN Model. The length of the PDN Model name shall not exceed 40 characters in length. Blank characters are not allowed. PDN ModelPDN ModelDomain/[End PDN Domain]s PDN Domain shall contain one or more [PDN Model] keywords (each identified by a unique name).

Each PDN Model shall contain R\_pdn, C\_pdn and R\_leak sub-parameters. If any one of these sub-parameters are missing, the [PDN Model] keyword is illegal.

The EDA tool may disable all PDN Models that are contained in a PDN Domain. If two or more PDN Models are contained in one PDN Domain, the EDA tool may select one of them. The first [PDN Model] keyword entry under the [PDN Domain] keyword shall be considered the default by the EDA tool.

For each of the sub-parameters, the three columns contain values whose order does not depend on magnitude. The three entries shall be placed on a single line and shall be separated by at least one whitespace character. All three values are required for these sub-parameters. C\_pdn and R\_pdn shall be non-negative numbers (positive or zero). R\_leak shall be a positive number (zero is not allowed). If a value of C\_pdn is zero, the EDA tool may ignore it. “NA” is allowed for the second and third column only. If the second and/or third column value is NA, then the EDA tool shall use the first column value for simulation.

The electrical circuit model for the three sub-parameters is shown in Figure XX. Terminal 1 is defined by the first Bus\_label or Signal\_name sub-parameter under the [PDN Domain] keyword. Terminal 2 is defined by the second Bus\_label or Signal\_name sub-parameter under the [PDN Domain] keyword. If two or more die pads are associated with a terminal, the PDN Model shorts the die pads when it is enabled. When the EDA tool disables all PDN Models in a PDN Domain, the [PDN Domain] keyword and its [PDN Model] keywords will not short die pads associated with the terminal.

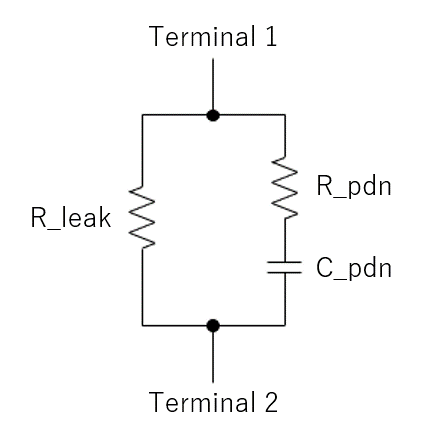


Figure XX – [PDN Model] circuit

Note that in simulation, the EDA tool may select one column from the typical, minimum or maximum data of the buffer models from the same .ibs file. At the same time, the EDA tool may select the same column of PDN Model. However, the on-die decoupling capacitance PDN model characteristics do not necessarily depend on the same variations of the buffer such as voltage, temperature and process. For example, a MIM capacitor variation may have little dependence on the same process, voltage, and temperature conditions. In such cases, the model maker may list the same three values for the entry of the PDN Model sub-parameters. In addition, the on-die decoupling capacitance PDN model characteristics can vary depending on many other factors unrelated to the variation of the buffer. For example, the on-die capacitance of a gated power supply can vary due to the state of the gate. In such cases, the model maker may include multiple PDN Models in one PDN Domain. Based on the condition chosen by the user, the EDA tool may select one of them for simulation.

Note that the Interconnect Model and Series Model can also be used to represent on-die decoupling capacitance PDN characteristics and can co-exist with PDN Model. The model maker should ensure that on-die decoupling capacitance PDN characteristics are not double counted.

Note that when a PDN Model is used together with an Interconnect Model that does not have die pad (pin to buffer, pin only or buffer only) interfaces, there is no connection between them at the die pads. For example, when an Interconnect Model is intended for use in the pin to buffer rail path and a PDN Model is intended for use as the die pad to die pad decoupling of the rail, the PDN Model does not affect the I/O buffer in an unintended manner.

*Example:*

[PDN Domain] PDN\_for\_VDDQ

Bus\_label VDDQ | VDDQ is an IO power supply for a DDR3/4 combo PHY

Signal\_name VSS

[PDN Model] DDR3

|VDDQ Voltage Range 1.5 1.425 1.575

|Temperature    25    125   -40

|MOS Process Corner TT   SS    FF

C\_pdn 5n 4n 6n

R\_pdn 20m 30m 10m

R\_leak 15k 17k 11k

[End PDN Model]

|

[PDN Model] DDR4

|VDDQ [Voltage Range] 1.2 1.14 1.26

|Temperature    25    125   -40

|MOS Process Corner TT   SS    FF

C\_pdn 1.5n 1n 1.8n

R\_pdn 20m 30m 10m

R\_leak 15k 17k 11k

[End PDN Model]

[End PDN Domain]

[PDN Domain] MOS\_capacitor\_for\_VCC

Bus\_label VCC

Signal\_name VSS

[PDN Model]

|VCC Voltage Range 0.9 0.84 0.96

|Temperature    25    125   -40

|MOS Process Corner TT   SS    FF

C\_pdn     200n 150n 250n

R\_pdn      3m 4m 1m

R\_leak     5k 8k 2k

[End PDN Model]

[End PDN Domain]

[PDN Domain] MIM\_capacitor\_for\_VCC

Bus\_label VCC

Signal\_name VSS

| MIM cap does not depend on MOS PVT variations,

| but instead varies with intermetal dielectric and metal.

[PDN Model] Medium\_MIM

|VCC Voltage Range 0.9 0.84 0.96

|Temperature    25    125   -40

|MOS Process Corner TT   SS    FF

C\_pdn     70n 70n 70n

R\_pdn      0 0 0 | R\_pdn: Short

R\_leak     1G 1G 1G | R\_leak: Open

[End PDN Model]

|

[PDN Model] Large\_MIM

|VCC Voltage Range 0.9 0.84 0.96

|Temperature    25    125   -40

|MOS Process Corner TT   SS    FF

C\_pdn     72n 72n 72n

R\_pdn      0 0 0 | R\_pdn: Short

R\_leak     1G 1G 1G | R\_leak: Open

[End PDN Model]

|

[PDN Model] Small\_MIM

|VCC Voltage Range 0.9 0.84 0.96

|Temperature    25    125   -40

|MOS Process Corner TT   SS    FF

C\_pdn     67n 67n 67n

R\_pdn      0 0 0 | R\_pdn: Short

R\_leak     1G 1G 1G | R\_leak: Open

[End PDN Model]

[End PDN Domain]

[PDN Domain] Gated\_area\_for\_VCC

Bus\_label VCC

Signal\_name VSS

[PDN Model] Gate\_off

|VCC Voltage Range 0.9 0.84 0.96

|Temperature    25    125   -40

|MOS Process Corner TT   SS    FF

C\_pdn     0n 0n 0n | C\_pdn: zero (ignored)

R\_pdn      0 0 0 | R\_pdn: Short

R\_leak     1G 1G 1G | R\_leak: Open

[End PDN Model]

|

[PDN Model] Gate\_on

|VCC Voltage Range 0.9 0.84 0.96

|Temperature    25    125   -40

|MOS Process Corner TT   SS    FF

C\_pdn     21n 18n 22n

R\_pdn      15m 18m 11m

R\_leak     17k 20k 14k

[End PDN Model]

[End PDN Domain]

*Keyword:* [End PDN Model]

*Required:* Yes, for each instance of the [PDN Model] keyword

*Description:* Indicates the end of the PDN Model data.

*Example:*

[End PDN Model]

**BACKGROUND INFORMATION/HISTORY:**

This proposal has been discussed in JEITA LPB-SC Modeling WG.

Kazuki Murata (Ricoh) proposed in IBIS summit Japan 2017.

Kazuki Murata (Ricoh) presented in LPB Forum 2018.

Megumi Ono (Socionext) proposed in DesignCon 2019 IBIS summit.

Atsushi Tomishima (Toshiba Electronic Devices & Storage Corporation) proposed in DesignCon 2020 IBIS summit.

BIRD198.1 contains significant edits to the original proposal.

BIRD198.2 contains additional editorial changes.