This document lists all lines (or paragraphs) that contain the string GND. I eliminated occurrences of “[GND …]” and “GND Pulse …”. The (n): at the beginning of each line is an artifact of the way I did this extraction, but us useful to identify each GND occurrence.

This does not include GND in graphics and the ground symbol in graphics.

Items in Red are not covered by the following proposed language I recommend added to the beginning of the IBIS Spec:

GND is used in many places in this document as the signal\_name of Pins that have Model Name GND. GND in many “buffer example schematics” use this name GND as a signal name such as VCC, VDD, VSS. The string GND in this document shall refer to either a Model Name in the Pin list or a signal name on one or more pins that coincidently also have Model Name GND. GND shall never be interpreted as the reference node in many SPICE simulators that is often called Node 0. Since IBIS defines signal\_name as a component Data Book Name, we must assume that all Pins that have Model Name POWER or GND and have the same\_signal name are assumed to be connected together on the components board or module. Each buffer can have one or two ground terminals (pdref and/or gcref) that are local nodes of the of the power distribution circuit of Pins that has Model Name GND. [Pin Mapping] is required to determine which signal\_name is the local ground nodes of each Buffer.

Note that in IBIS, when GND is used with POWER it refers to the Model\_name usage of GND. When GND is used with VDD or Vtt it refers to the signal\_name usage of GND. This can easily be inferred from the IBIS text. We can either state this assumption and make few changes to IBIS, Change all occurrences of GND (and gnd) to VSS (and vss) and eliminate the confusion in IBIS, or add to many occurances of GND a note that this GND is a signal\_name, or a model name.

(260):GND - reserved model name, used with ground pins

(667):Usage Rules: All pins on a component must be specified. The first column must contain the pin name. The second column, signal\_name, gives the data book name for the signal on that pin. The third column, model\_name, maps a pin to a specific I/O buffer model or model selector name. Each model\_name must have a corresponding model or model selector name listed in a [Model] or [Model Selector] keyword below, unless it is a reserved model name (POWER, GND, or NC).

(689): 10 GND GND 297.0m 6.7nH 3.4pF

(691): 12 GND GND 270.0m 5.3nH 4.0pF

(733):Usage Rules: The [Pin Mapping] keyword names the connections between POWER and/or GND pins and buffer and/or terminator voltage supply references using unique bus labels. All buses with identical labels are assumed to be connected with an ideal short. Each label must be associated with at least one pin whose model\_name is POWER or GND. Bus labels must not exceed 15 characters.

(740):The usage of the columns changes for GND and POWER pins. For GND pins, the pulldown\_ref column contains the name of the bus to which the pin connects; the pullup\_ref column in this case must contain the reserved word NC. Similarly, for POWER (including external reference) pins, the pullup\_ref column contains the name of the bus to which the pin connects; the pulldown\_ref column in this case must contain the reserved word NC.

(801):11 VSS1 GND

(802):12 VSS1 GND

(803):13 VSS1 GND

(804):21 VSS2 GND

(805):22 VSS2 GND

(806):23 VSS2 GND

(813):51 VSSCLAMP GND | Power connections for clamps

(864):Usage Rules: Enter only series pin pairs. The first column, [Series Pin Mapping], contains the series pin for which input impedances are measured. The second column, pin\_2, contains the other connection of the series model. Each pin must match the pin names declared previously in the [Pin] section of the .ibs file. The third column, model\_name, associates models of type Series or Series\_switch, or model selectors containing references to models of type Series or Series\_switch for the pair of pins in the first two columns. Each model\_name must have a corresponding model or model selector name listed in a [Model] or [Model Selector] keyword below. The usage of reserved model names (POWER, GND, or NC) within the [Series Pin Mapping] keyword is not allowed. The fourth column, function\_table\_group, contains an alphanumeric designator string to associate those sets of Series\_switch pins that are switched together.

(970):Usage Rules: Each model type must begin with the keyword [Model]. The model name must match the one that is listed under a [Pin], [Model Selector] or [Series Pin Mapping] keyword and must not contain more than 40 characters. A .ibs file must contain enough [Model] keywords to cover all of the model names specified under the [Pin], [Model Selector] and [Series Pin Mapping] keywords, except for those model names that use reserved words (POWER, GND and NC).

(1491):Description: The data points under these keywords define the I-V tables of the pulldown and pullup structures of an output buffer and the I-V tables of the clamping diodes connected to the GND and the POWER pins, respectively. Currents are considered positive when their direction is into the component.

(1574):The effective current table for the Isso\_pd current is extracted by the following process. The buffer is set to “logic zero.” A Vtable voltage source is inserted between the [Pulldown Reference] node and the buffer as shown in Figure 7. This Vtable voltage is swept from -Vcc (typical) to +Vcc (typical) and is relative to the [Pulldown Reference] typ/min/max values for the corresponding columns. The output is connected to the GND (typical) value as shown in Figure 7.

(1579):The effective current table for the Isso\_pu current is extracted by the following process. The buffer is set to “logic one”. A Vtable voltage source is inserted between the [Pullup Reference] node and the buffer as shown below. This Vtable voltage is swept from -Vcc (typical) to +Vcc (typical) and is relative to the [Pullup Reference] typ/min/max values for the corresponding columns. The output is connected to the GND (typical) value as shown in Figure 8.

(1609):For example, for a typ/min/max [Voltage Range] of 5.0V, 4.5V and 5.5V, and with the negative reference set to GND, the Isso\_pu(0) and Isso\_pd(0) values for typ/min/max should be equal to the column values as shown in Table 3.

(1663):Description: The data for these keywords define the resistance values of Rgnd and Rpower connected to GND and the POWER pins, respectively, and the resistance and capacitance values for an AC terminator. See Figure 11.

(1918):Figure 16 illustrates a general configuration from which a [Rising Waveform] or [Falling Waveform] is extracted. The DUT die shows all of the available power and ground pin reference voltage terminals. For many buffers, only one power pin and one common ground pin terminal are used. The absolute GND is the reference for the V\_fixture voltage and the package model equivalent network. It can also serve as a reference for C\_comp, unless C\_comp is optionally split into component attached to the other reference voltages.

(1925):Other Notes: Figure 17 documents some expected internal paths for a useful special case where only one common power pin (VDDQ) and one common ground exists (GND).

(1943):The power reference terminal (VDDQ) is usually the [Pullup Reference], or the default [Voltage Range] terminal. The [Pulldown Reference] terminal is usually at the GND connection.

(1945):In most cases six [Composite Current] tables are recommended for accurate modeling. The first four tables correspond to the recommended fixture conditions for [Rising Waveform] and [Falling Waveform] tables (normally 50 ohm loads to Vdd and GND). Two additional waveforms for no load conditions (such as with an R\_fixture of 1.0 Megaohm) are useful. However, some EDA tools process only the first four waveforms. So the additional open load waveforms for I-T tables should be in [Rising Waveform] and [Falling Waveform] tables that are positioned after the other V-T tables to maintain the best output response simulation accuracy.

(1948):The [Composite Current] table can be derived from currents measured at the [Pulldown Reference] (GND) node, but adjusted for the current flowing through the output pin and at other terminals.

(3395):Ports vcc gnd io1 io2

(3420):Ports vcc gnd io1 io2

(3442):Ports vcc gnd io1 io2

(3460):Ports vcc gnd io1 io2

(3580):Port\_map gnd pad\_11 | Port to explicit pad connection

(3852):Usage Rules: This keyword may optionally be used when the [Model Data] keyword is present in the [Define Package Model] section. When used, it must be placed after the end of the pin list defined by the [Pin Numbers] keyword and before the [Model Data] keyword. The keyword must be followed by one pin name (the merging pin) on the same line on which the keyword appears, separated by at least one white space. This pin name must be listed under the [Pin Numbers] keyword, it must be listed as a POWER or GND pin under the [Pin] keyword and it must also be a member of a power or ground bus defined by the [Pin Mapping] keyword. This is the pin whose package model contains the merged package model data for a group of power or ground pins.

(3854):Each pin name in the list of merged pins must match the name of a POWER or GND pin in the [Pin] keyword and must also be a member of the same power or ground bus as the merging pin (pin name that follows the [Merged Pins] keyword). Pin names in this list must not be present in the pin list under the [Pin Numbers] keyword. The list must include the names of all those pins which are to be connected to the merging pin that follows the [Merged Pins] keyword due to merged modeling. No pin name may appear more than once under all [Merged Pins] keywords.

(3861):[Description] FBGA Package Model for x4 Data Pins and POWER/GND

(4173):Usage Rules: Following the [Pin List] keyword are two columns. The first column lists the pin name while the second lists the data book name of the signal connected to that pin. There must be as many pin\_name/signal\_name rows as there are pins given by the preceding [Number Of Pins] keyword. Pin names must be the alphanumeric external pin names of the part. The pin names cannot exceed eight characters in length. Any pin associated with a signal name that begins with “GND” or “POWER” will be interpreted as connecting to the boards ground or power plane. In addition, NC is a legal signal name and indicates that the Pin is a “no connect”. As per the IBIS standard “GND,” “POWER,” and “NC” are case insensitive.

(4178): A1 GND

(4194):Description: This keyword allows the user to describe the connection between the user accessible pins of a board level component and other pins or pins of the ICs mounted on that board. Each pin to node connection is divided into one or more cascaded “sections,” where each section is described in terms of its L/R/C per unit length. The Fork and Endfork subparameters allow the path to branch to multiple nodes, or another pin. A path description is required for each pin whose signal name is not “GND,” “POWER,” or “NC.”

(4202):Usage Rules: Each individual connection path (user pin to node(s)) description begins with the [Path Description] keyword and a path name, followed by the subparameters used to describe the path topology and the electrical characteristics of each section of the path. The path name must not exceed 40 characters, blanks are not allowed, and each occurrence of the [Path Description] keyword must be followed by a unique path name. Every signal pin (pins other than POWER, GND or NC) must appear in one and only one path description per [Begin Board Description]/[End Board Description] pair. Pin names do not have to appear in the same order as listed in the [Pin List] table. The individual subparameters are broken up into those that describe the electrical properties of a section, and those that describe the topology of a path.

(4397):[Pulldown] GND – POWER POWER + POWER

(4398):[Pullup] GND – POWER POWER + POWER

(4401):[Series Current] GND – POWER GND + POWER

(4402):[Series MOSFET] GND GND + POWER

(4417):Then: Attach a 50 ohm resistor to GND to derive the rising edge ramp. Attach a 50 ohm resistor to POWER to derive the falling edge ramp.

(4423):Then: Attach either a 50 ohm resistor or the semiconductor vendor suggested termination resistance to either GND or the suggested termination voltage. Use this load to derive both the rising and falling edges.