BY BONNIE BAKER

IBIS and Spice timing mismatches

Growing up, I was a station-wagon kid. My parents sat in the front to see where we were going. The rest of us (six kids) took over the back, where we had a beautiful view of where we had been. Being in back wasn't bad, but input from the outside world was limited.

Similar to my parents up front, IBIS (I/O-buffer-information-specification) simulation models have a strong handle on the outside world. They model the performance of the buffer's interaction with the PCB (printed-circuit board) but omit interactions with nodes inside the chip. IBIS models simulate the system level of PCB behavior, specifically modeling the connection from the outside world to the I/O buffer. On the other hand, Spice models simulate all of the transistors inside the chip. Spice transistor-level simulations analyze the path through the output buffer but have a limited view of the PCB inductive, resistive, and capacitive parasitics.

IBIS models are high-speed and system-based. They define the elements of an IC that interact with outside, "real-world" elements. At high speeds, interactions between IC-package and PCB-trace parasitics have a strong impact on signal behavior. For instance, all models have pin and package resistive, capacitive, and inductive parasitic elements (**Figure 1**).

Why do engineers use IBIS models? Speed. IBIS models simulate 10 times faster than transistor-level models do. IBIS models offer system designers reduced analysis times and allow IC manufacturers to avoid disclosing a transistor-level netlist of the buffer, which may contain proprietary data.

Concerning accuracy, current IBIS 3.2- and 4.0-model types accurately reflect CMOS-buffer impedances and switching times. Current models are ill-suited for power-delivery simulations, although improvements are coming. Otherwise, the model is as accurate as its source. If you generate an IBIS model from benchtesting the silicon, it can't simulate maximum and minimum statistical borders. The Spice-generated model is most accurate when IC designers carefully revisit their transistor models after collecting silicon bench data.

Simulating an IBIS model alongside its transistor-level Spice counterpart creates a mismatch between the IBIS- and Spice-simulation waveforms. A difference may exist between the initial delay of the waveforms—the time the output begins to switch minus the initial start time, t_0, of the simulation output curves. This scenario can occur even when IBIS and Spice models use the same excitation signals and load. This concept may be disconcerting at first, but closer inspection shows a shift in time between the two sets of waveforms. Why? Because the IBIS model is the "front-seat driver." As the backseat kid, the Spice model includes the entire delay through the output buffer, and the IBIS model represents only the buffer's external behavior. The difference in initial delays between the Spice and IBIS models doesn't matter, because the model user always "normalizes" delays to a reference condition.

The correlation between IBIS and Spice models may not be 100%, but speed advantages make IBIS models useful tools for system analysis. EDN

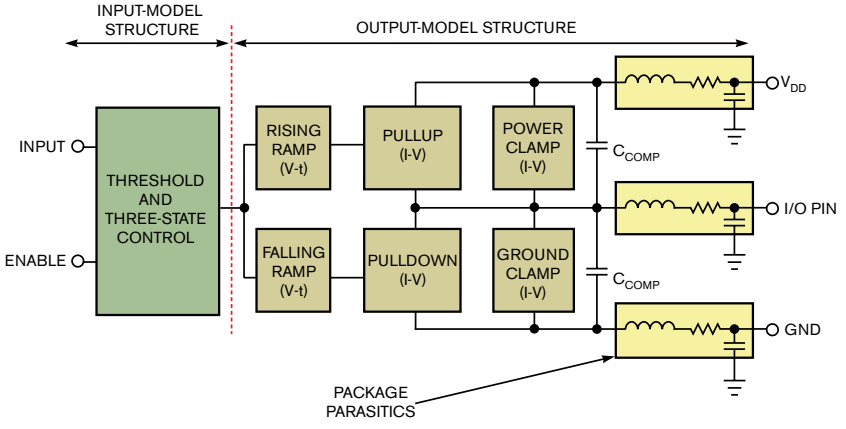

Figure 1 An IBIS model includes pin and package parasitic elements.

REFERENCES

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Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.