Test Cases and Results using BIRD 95 Composite Current Method

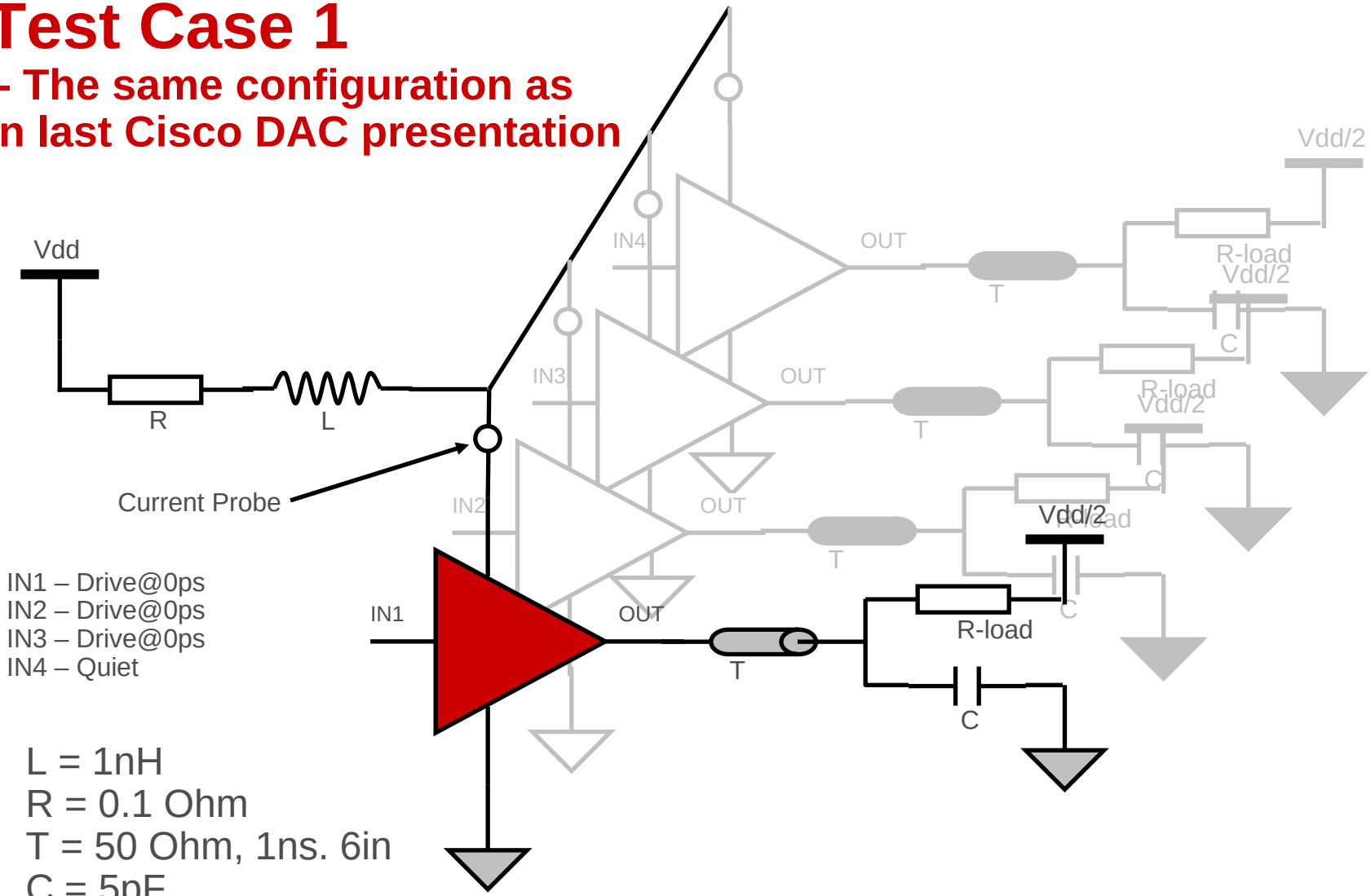
- August 4, 2005 – IBIS Future's Meeting

Test Initializations

- Model preparations
  - HSpice Transistor-level model
  - IBIS Model for it with 50ohm to Vdd and Ground VT curves
  - Very good overlaid by using 50ohm load to Vdd and ground with Idea Power Network
- Extract I/T tables from HSpice transistor model with 50ohm load to Vdd and Ground
- Extract ZVDDQ with Input High/Low
- Used the preferred method from Cisco BIRD 95 presentations
- Used for the same load condition tests (Best-Condition Tests)
- Used Input Stimulus 50ps Rising and Falling, 0-1.8v

Test Case 1

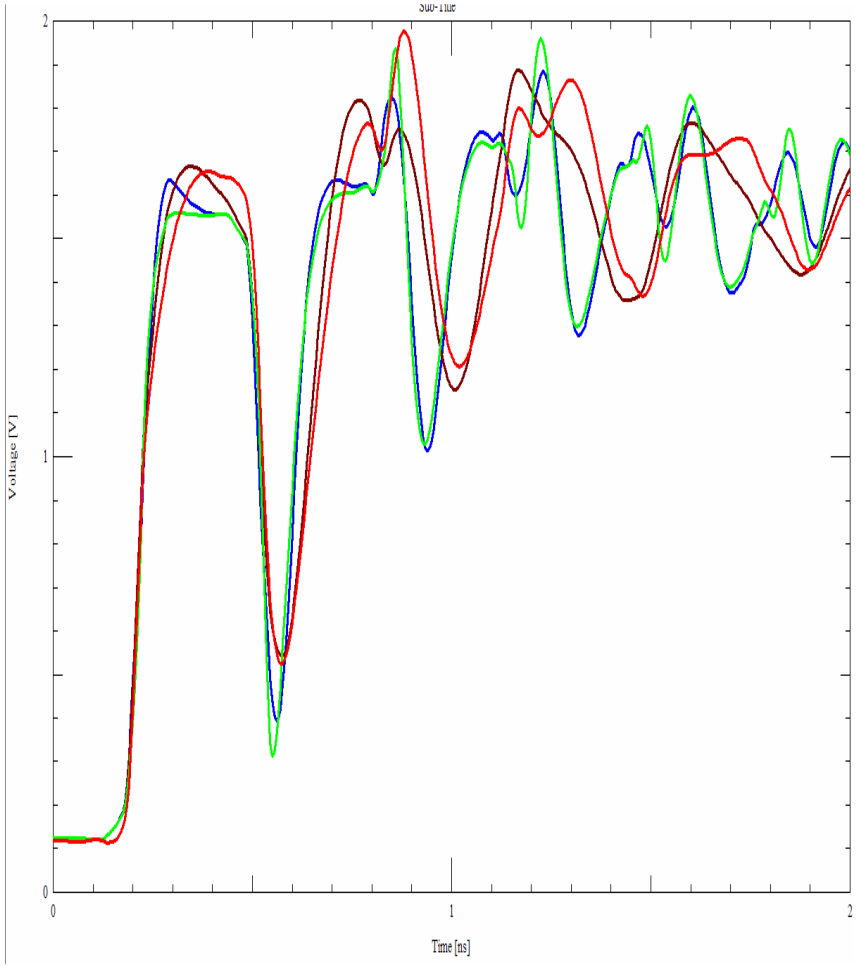
– The same configuration as in last Cisco DAC presentation



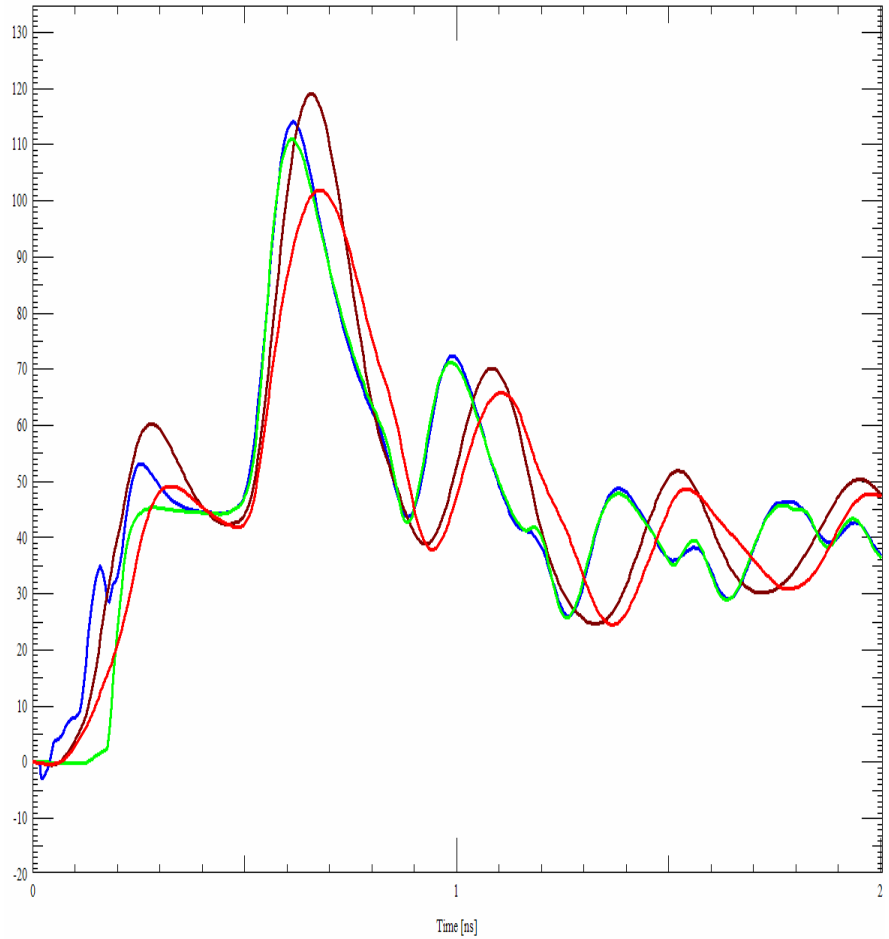
L = 1nH
R = 0.1 Ohm
T = 50 Ohm, 1ns. 6in
C = 5pF
R_load = 50 Ohm
Vdd = 1.8v

Test Case 1 – Rising – DDDQ – Driver

Output Voltage (v)



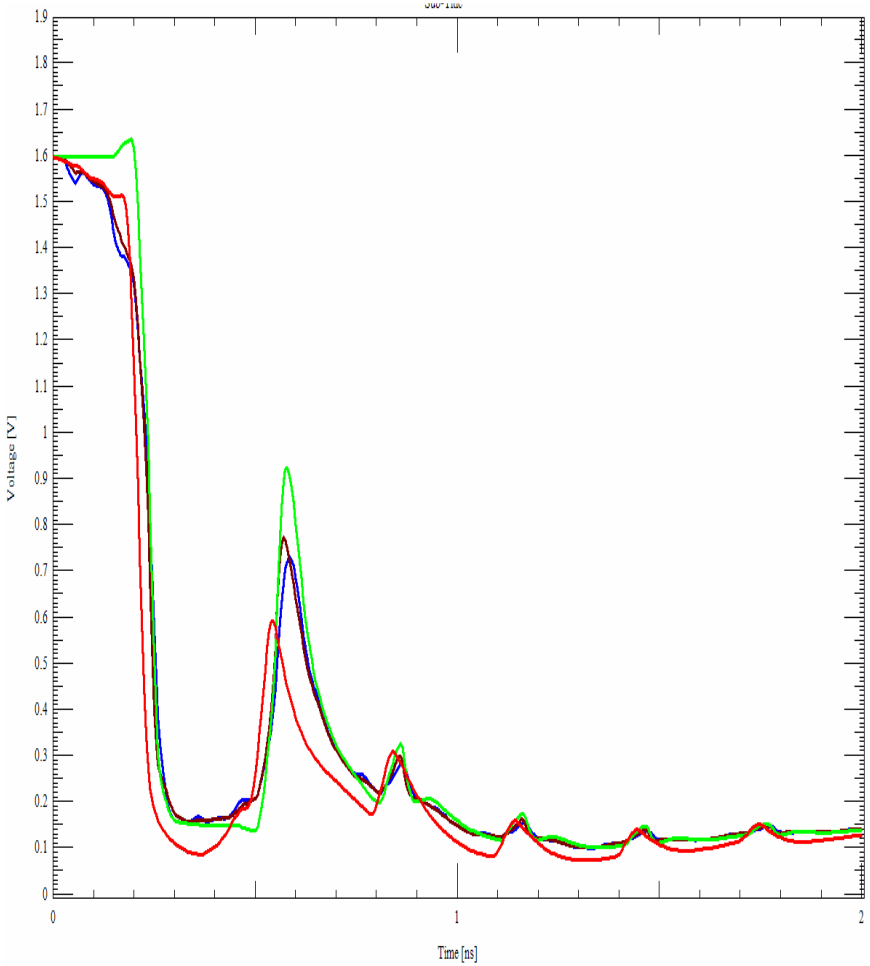
Current Probe (mA)



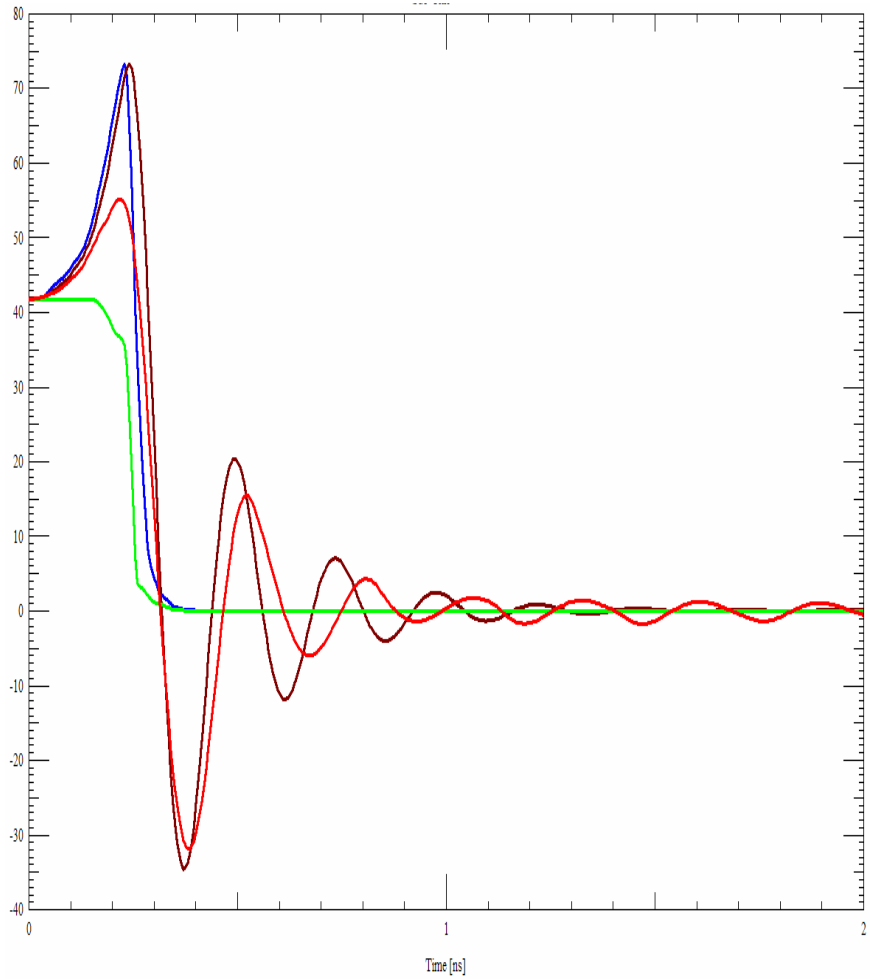
Red:Transistor, Blue:IBIS+I/T, Green:IBIS only, Brown:IBIS+I/T+ZVDDQ

Test Case 1 – Falling – DDDQ – Driver

Output Voltage (v)



Current Probe (mA)



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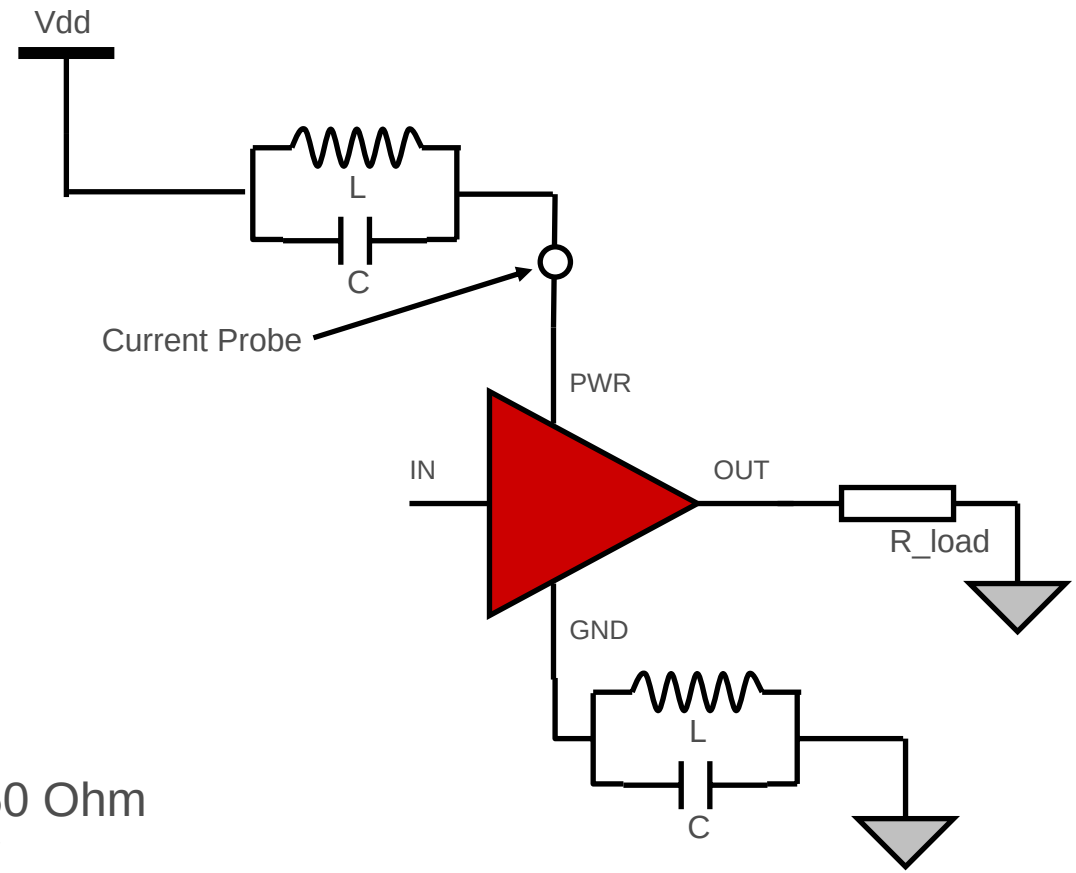
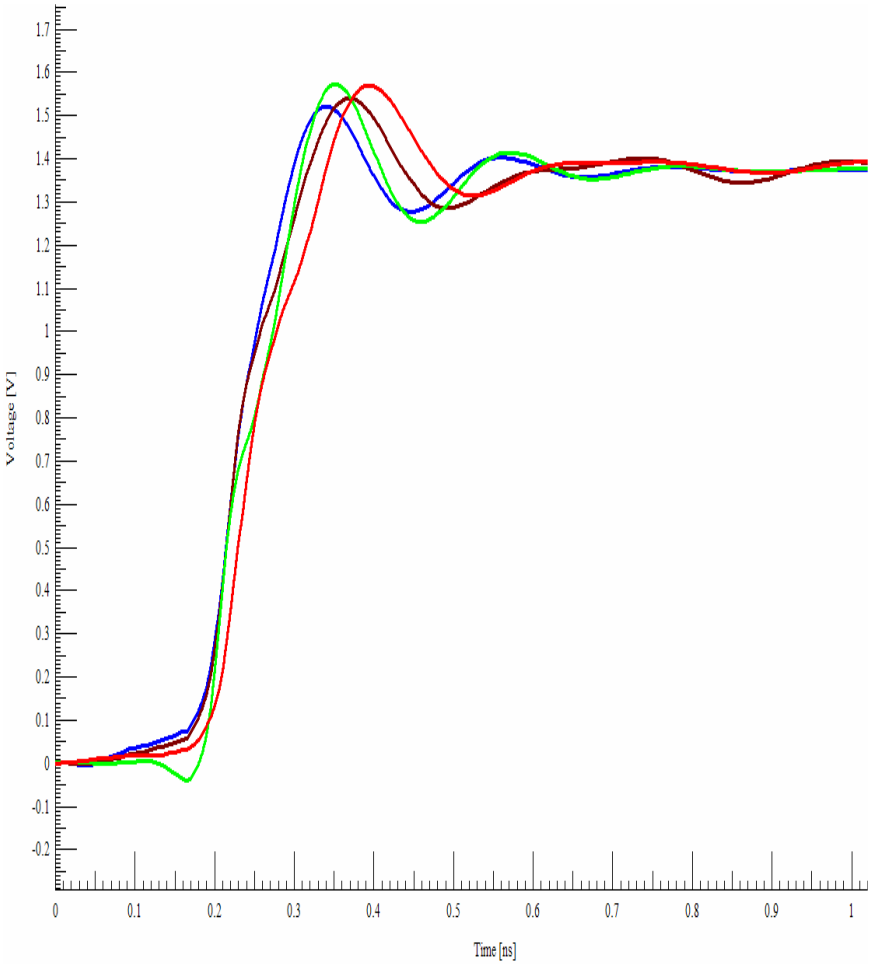
Test Case 2



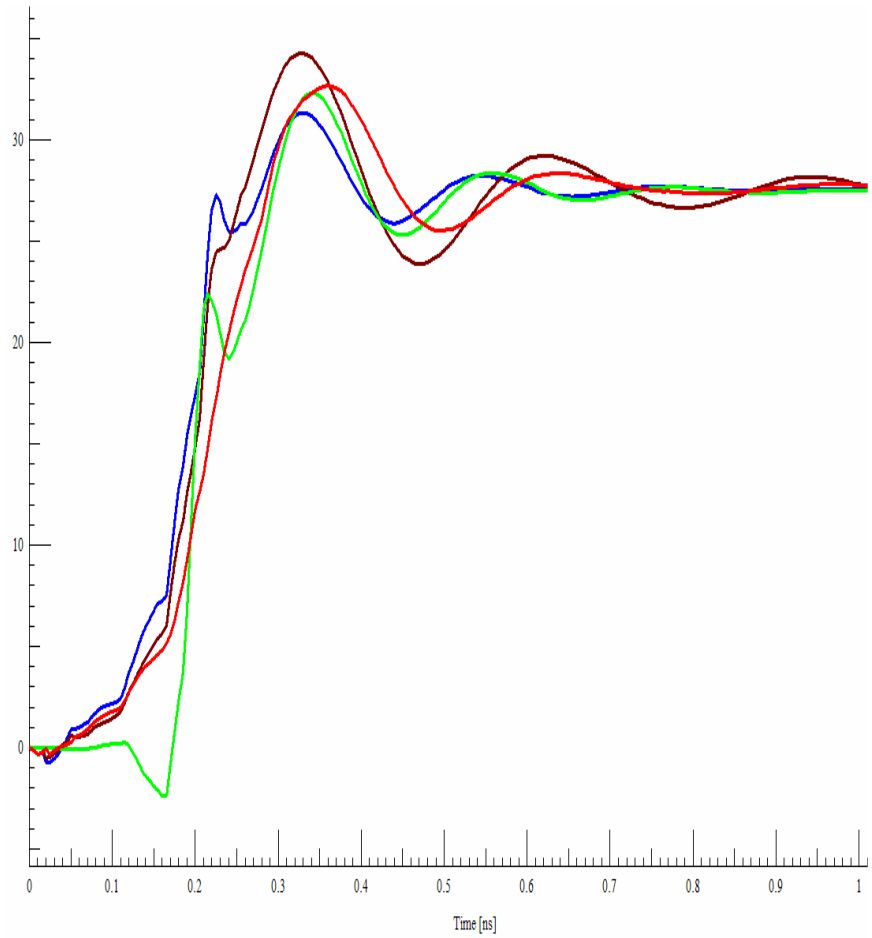
L = 1nH
C = 1pF
R_load = 50 Ohm
Vdd = 1.8v

Test Case 2 – Rising

Output Voltage (v)



Current Probe (mA)



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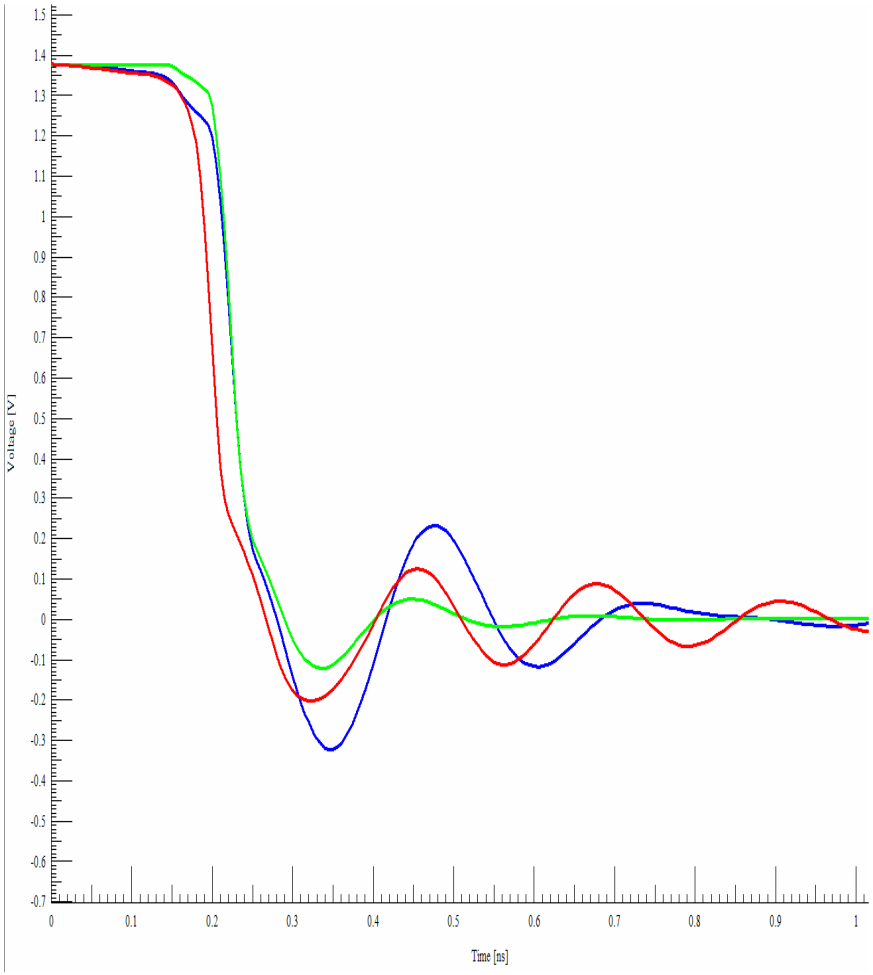
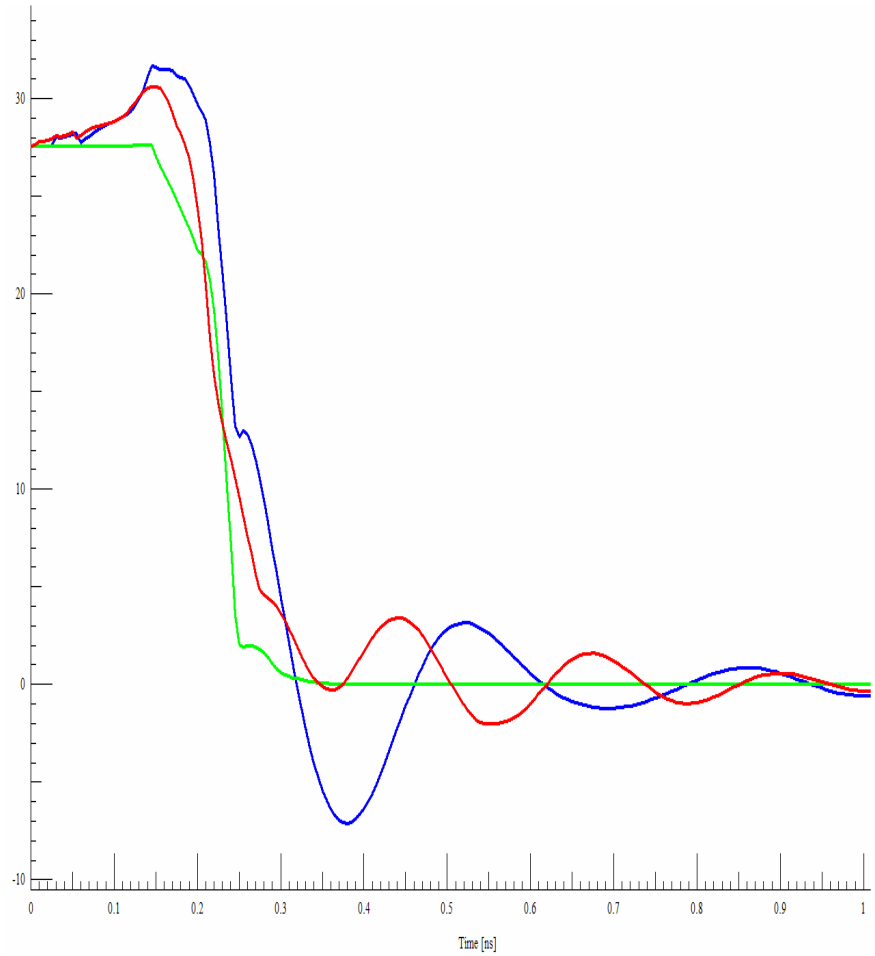
Test Case 2 – Falling

Output Voltage (v)

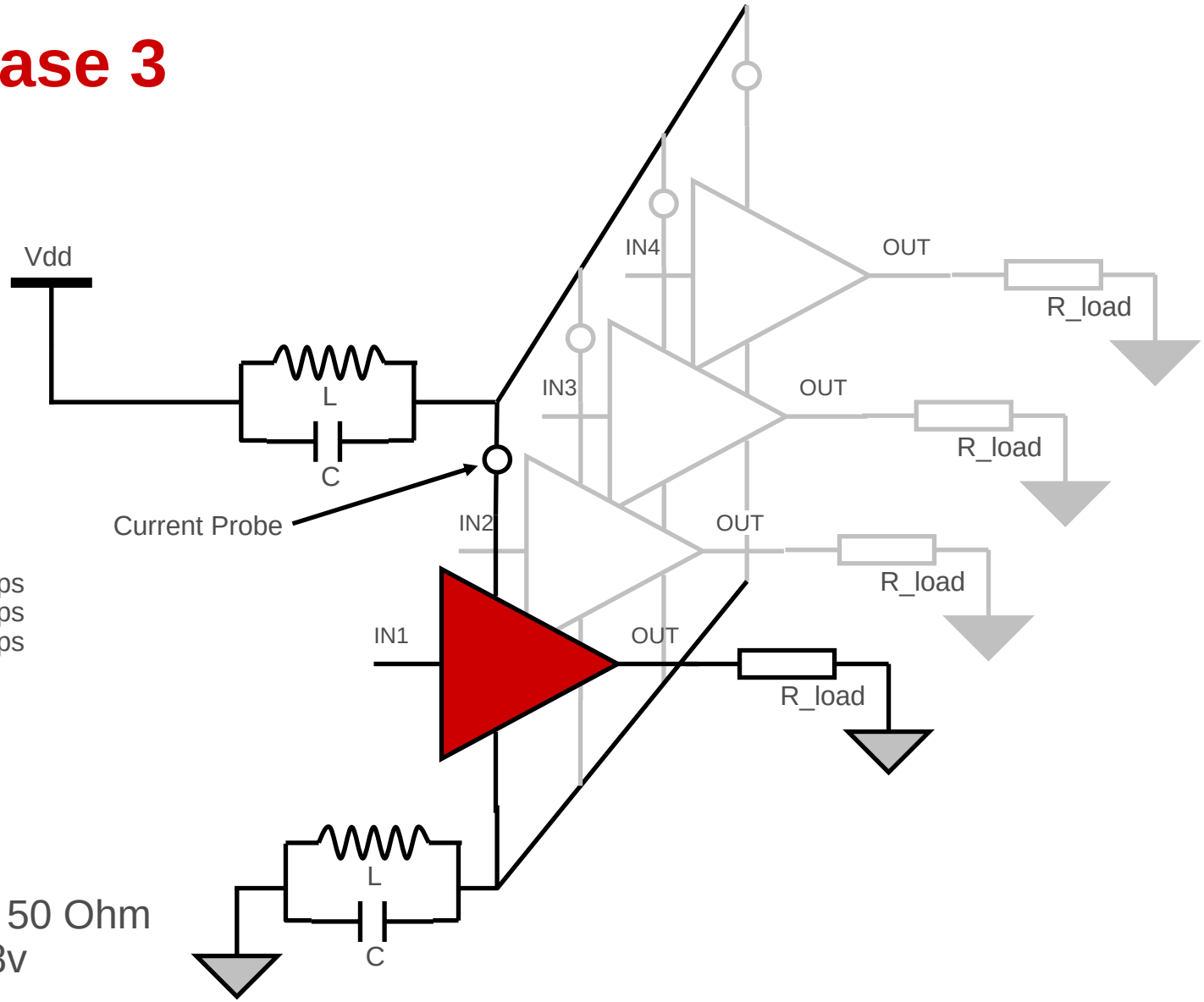


Current Probe (mA)



Red:Transistor, Blue:IBIS+I/T+ZVDDQ, Green:IBIS

Test Case 3

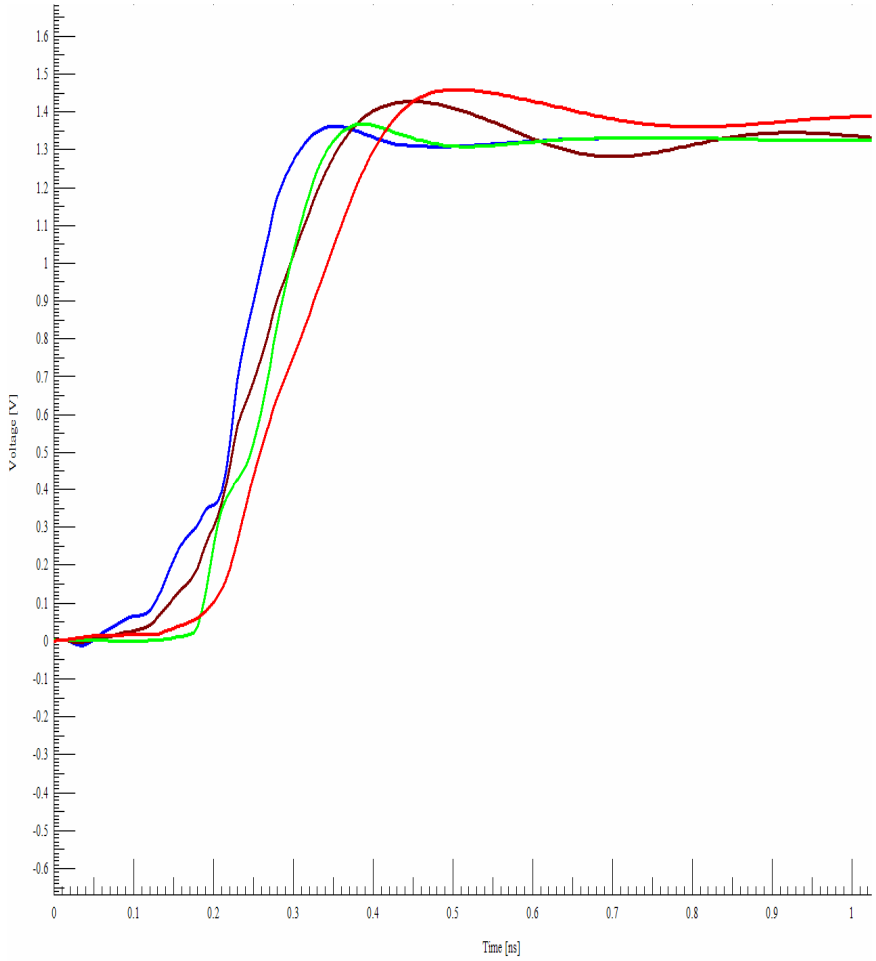


IN1 – Drive@0ps
IN2 – Drive@0ps
IN3 – Drive@0ps
IN4 – Quiet

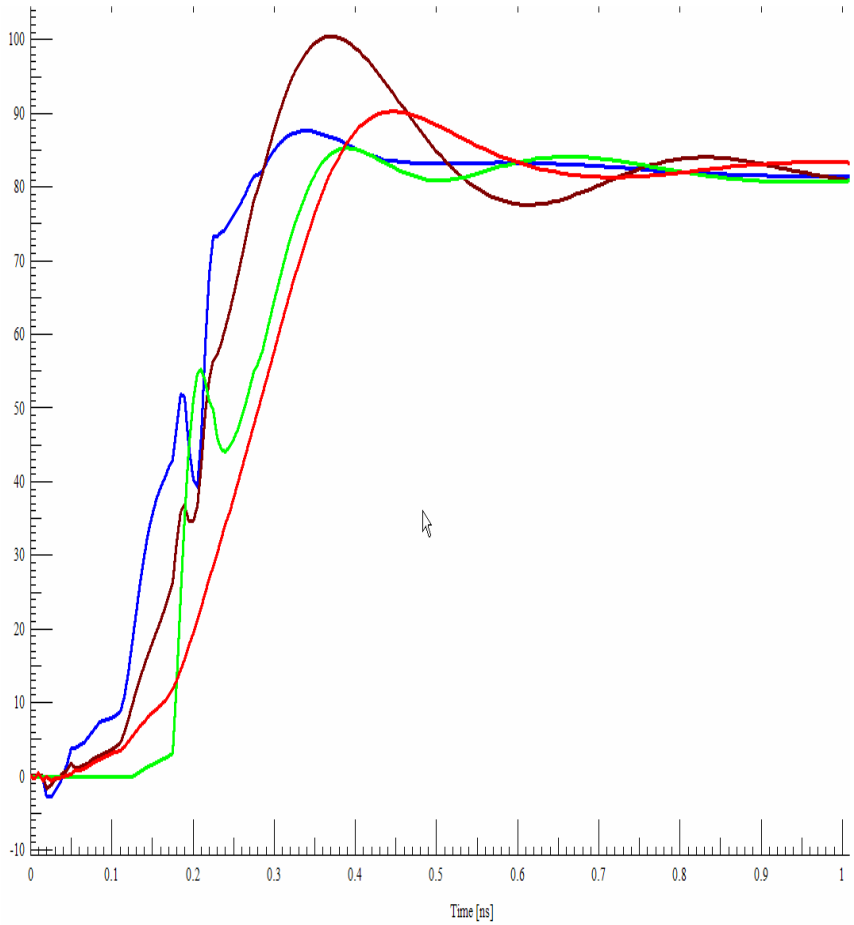
L = 1nH
C = 1pF
R_load = 50 Ohm
Vdd = 1.8v

Test Case 3 – Rising – DDDQ – Driver-IN1

Output Voltage (v)



Current Probe (mA)



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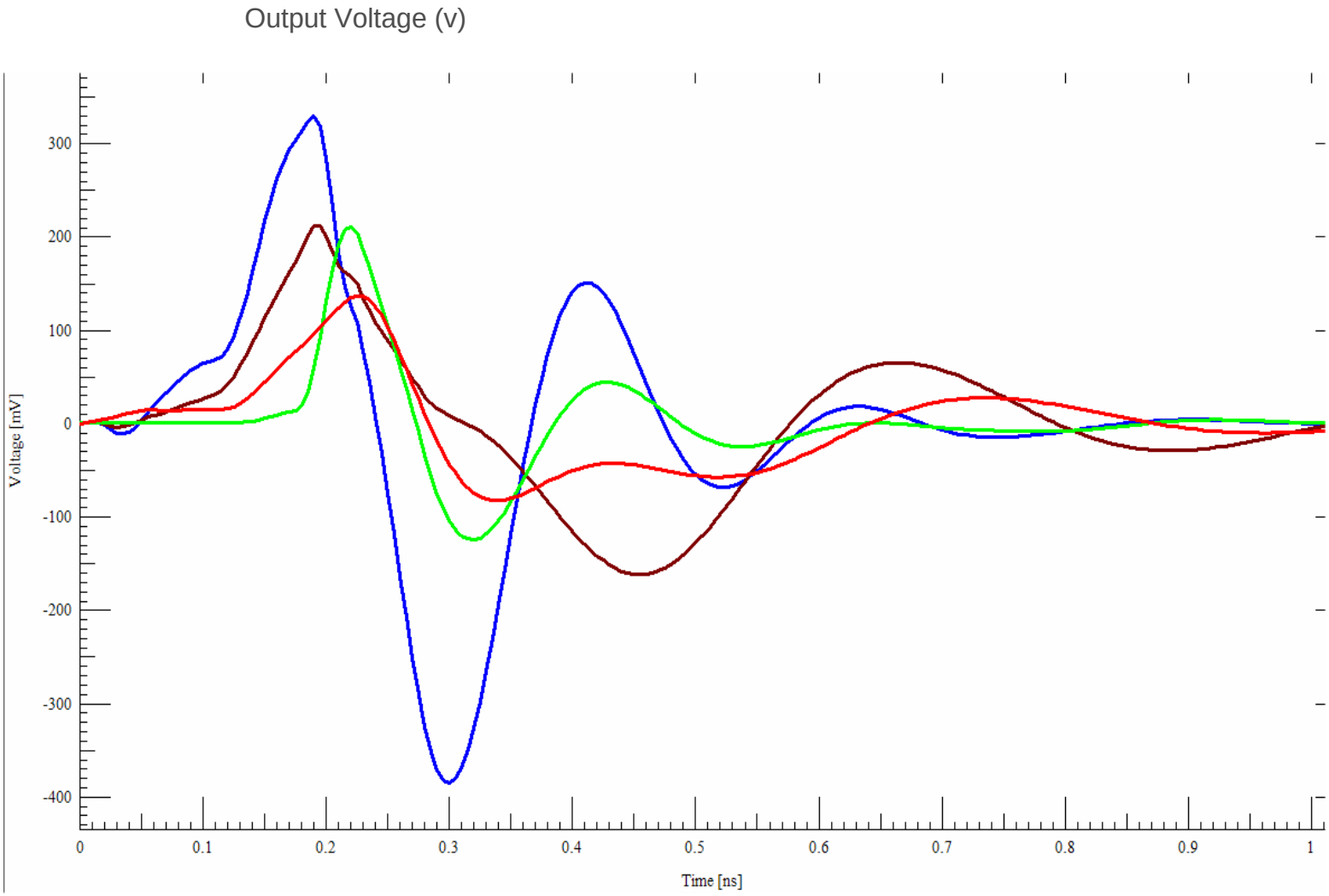
Test Case 3 – Rising – DDDQ – Quiet Line



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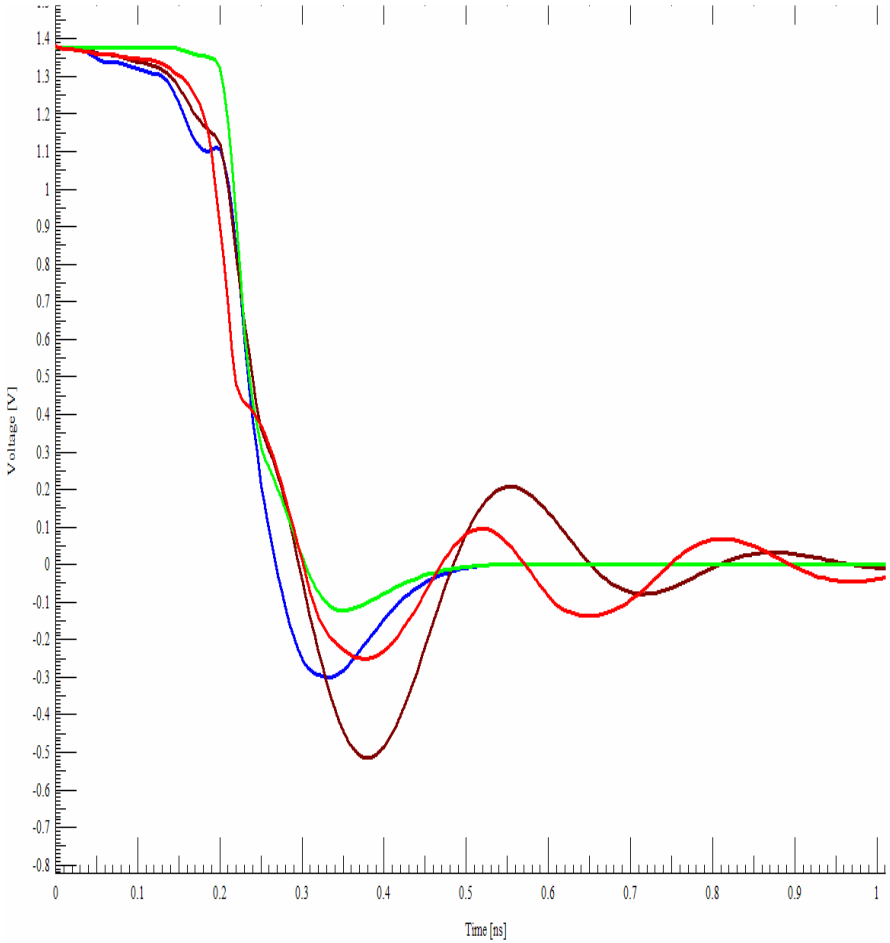
Test Case 3 – Falling – DDDQ – Driver-IN1

Output Voltage (v)



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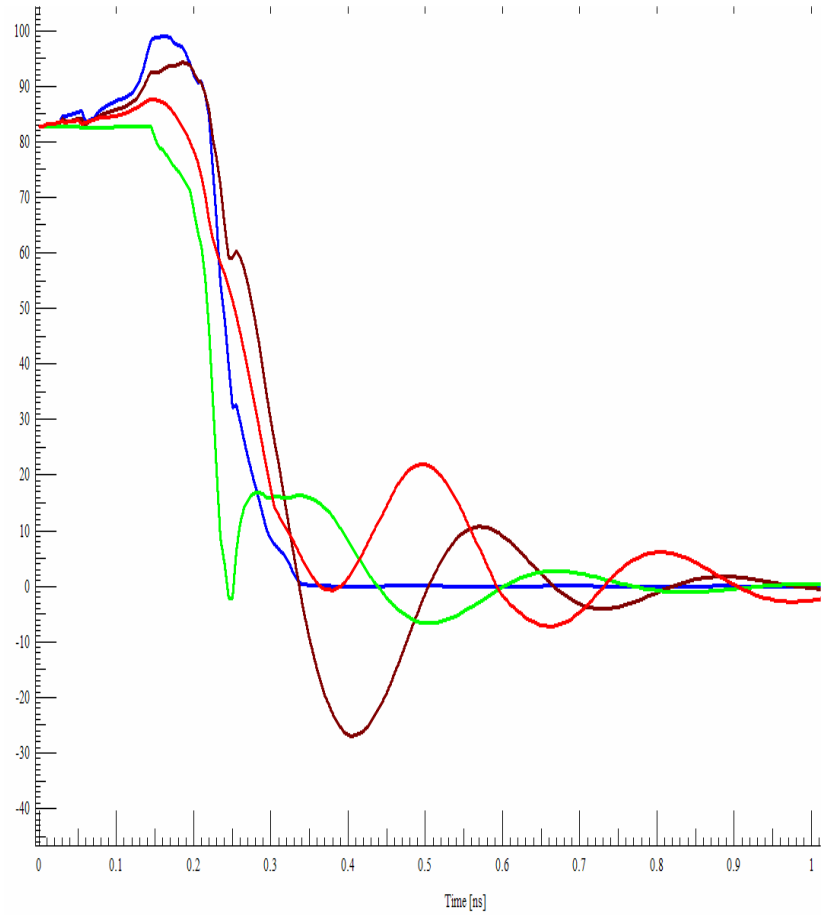

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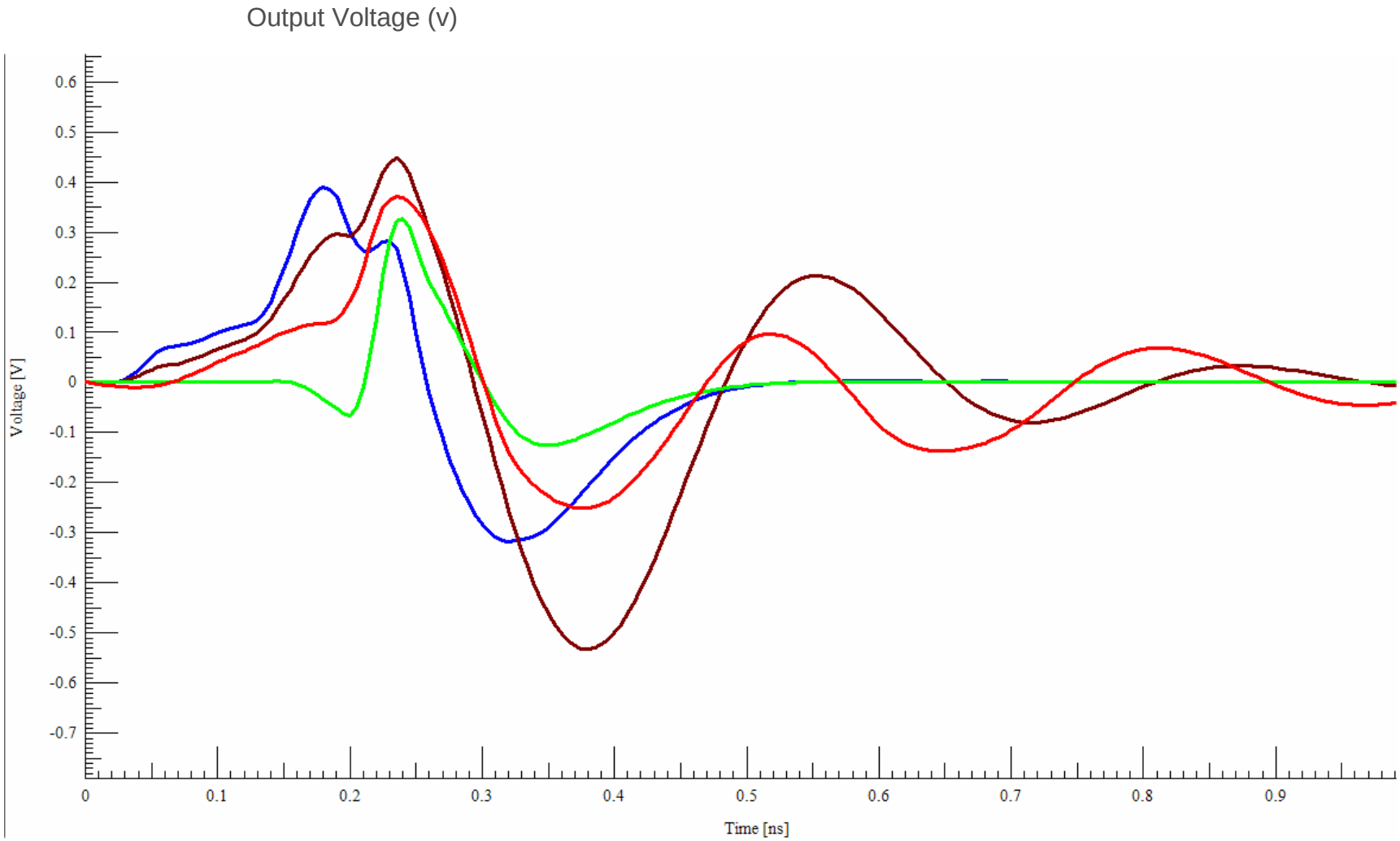
Test Case 3 – Falling – DDDQ – Quiet Line



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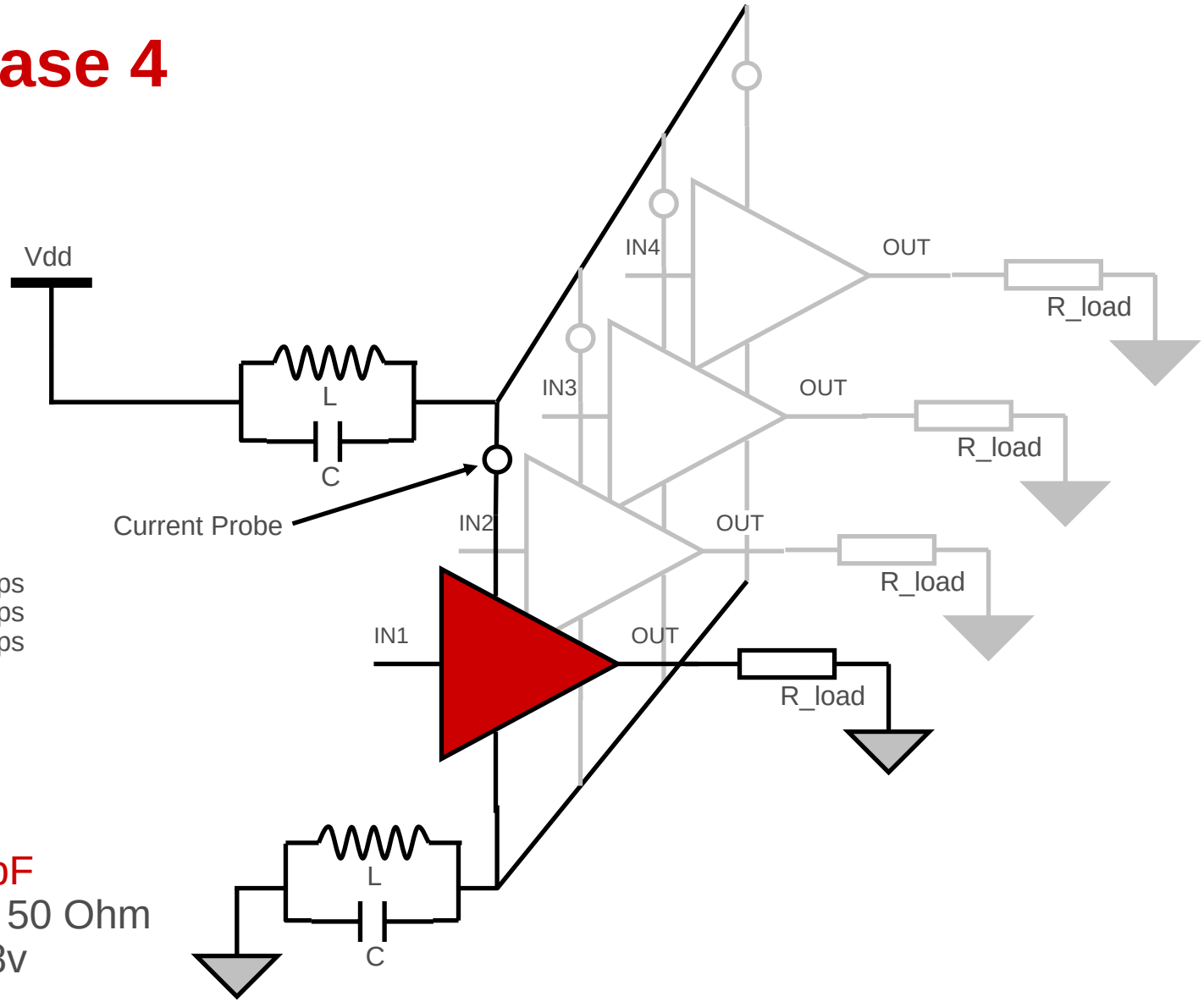
Test Case 4

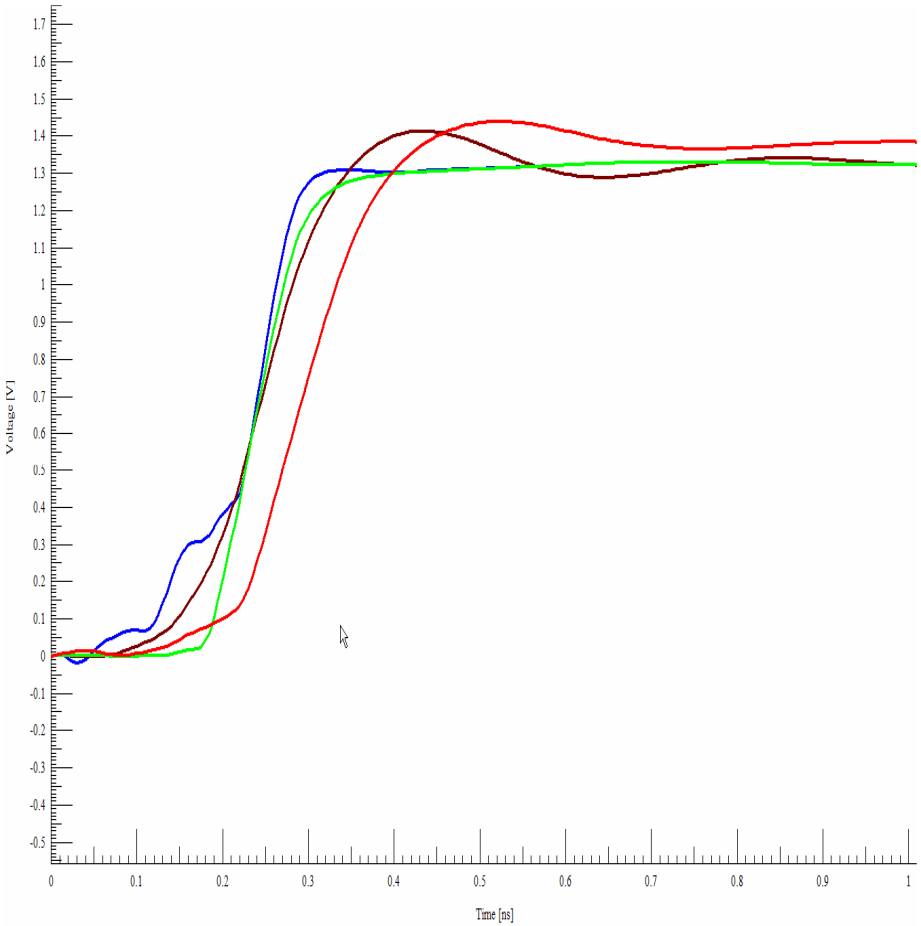


IN1 – Drive@0ps
IN2 – Drive@0ps
IN3 – Drive@0ps
IN4 – Quiet

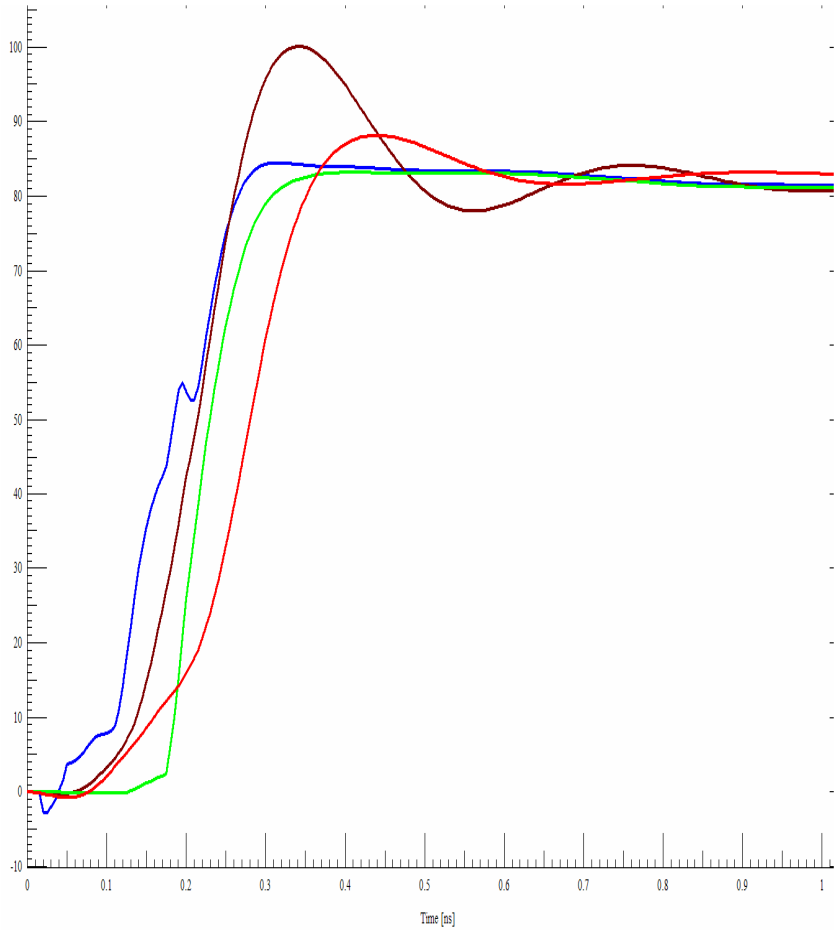
L = 1nH
C = 0.01pF
R_load = 50 Ohm
Vdd = 1.8v

Test Case 4 – Rising – DDDQ – Driver-IN1

Output Voltage (v)



Current Probe (mA)



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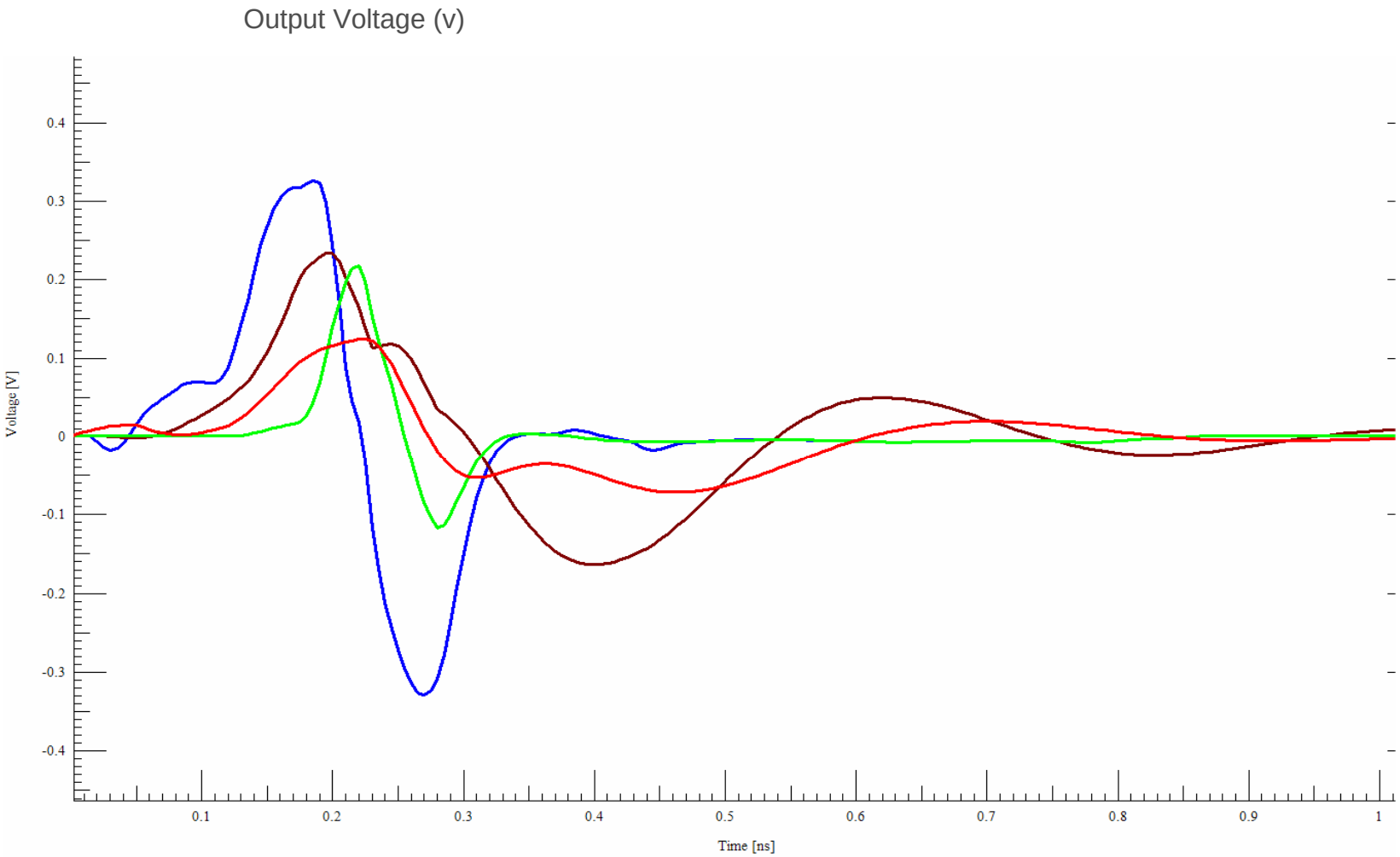
Test Case 4 – Rising – DDDQ – Quiet Line



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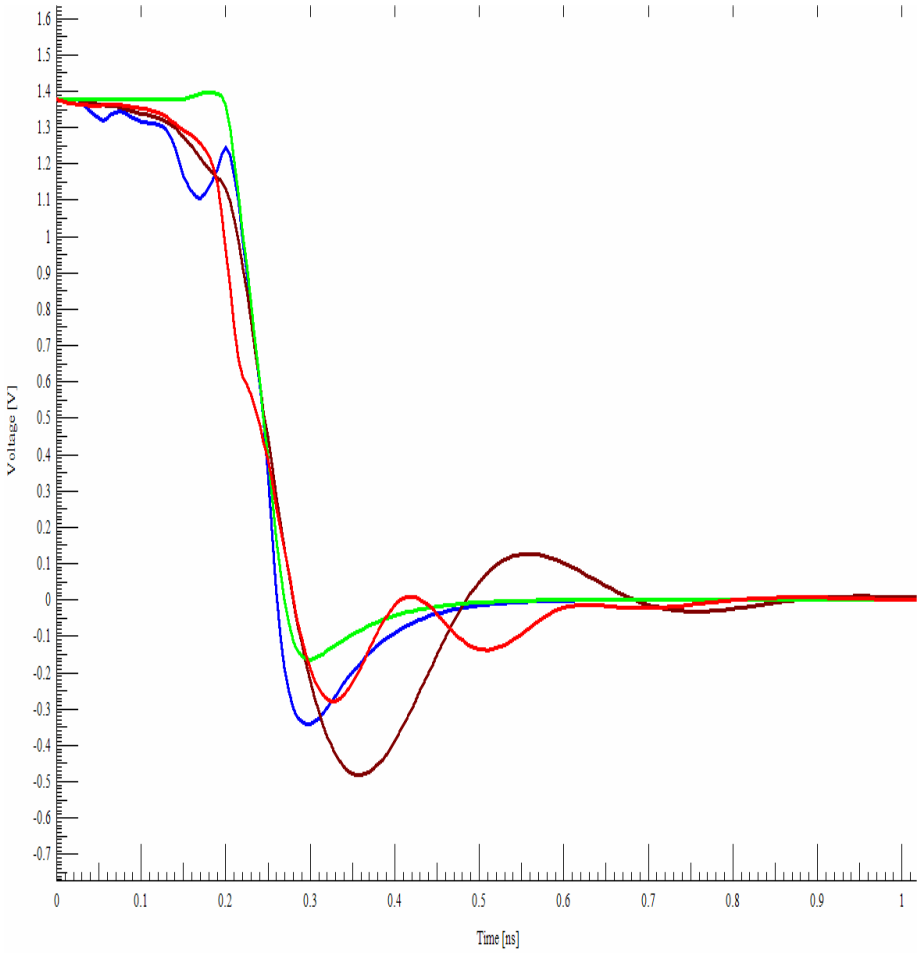
Test Case 4 – Falling – DDDQ – Driver-IN1

Output Voltage (v)



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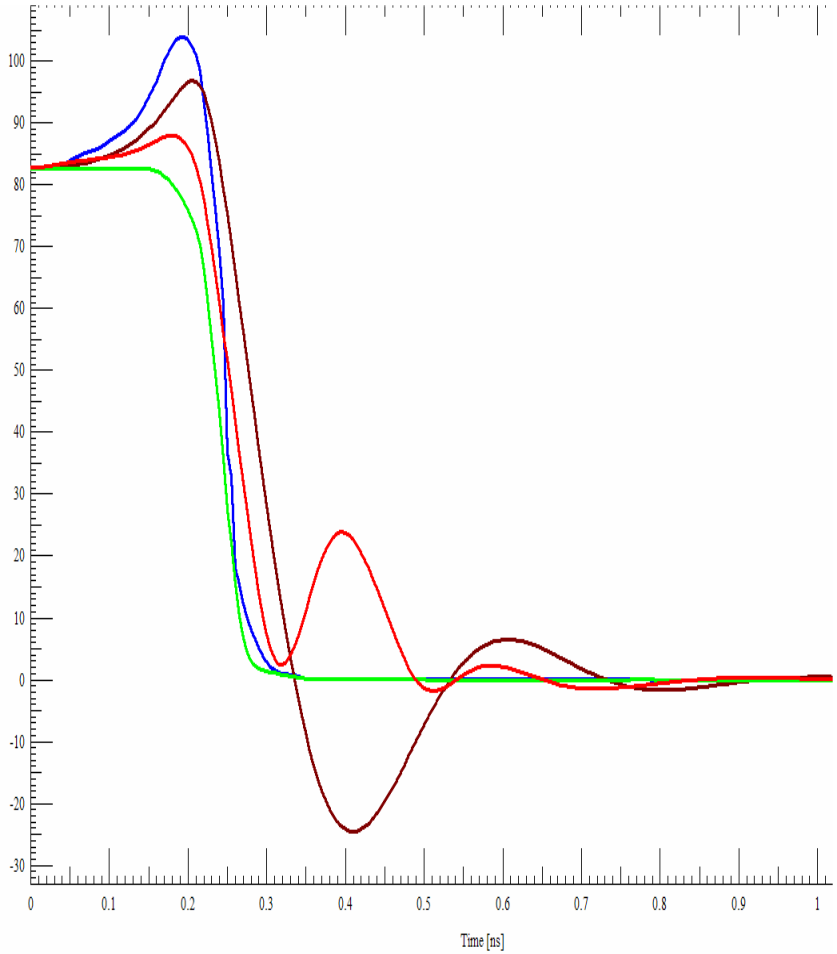

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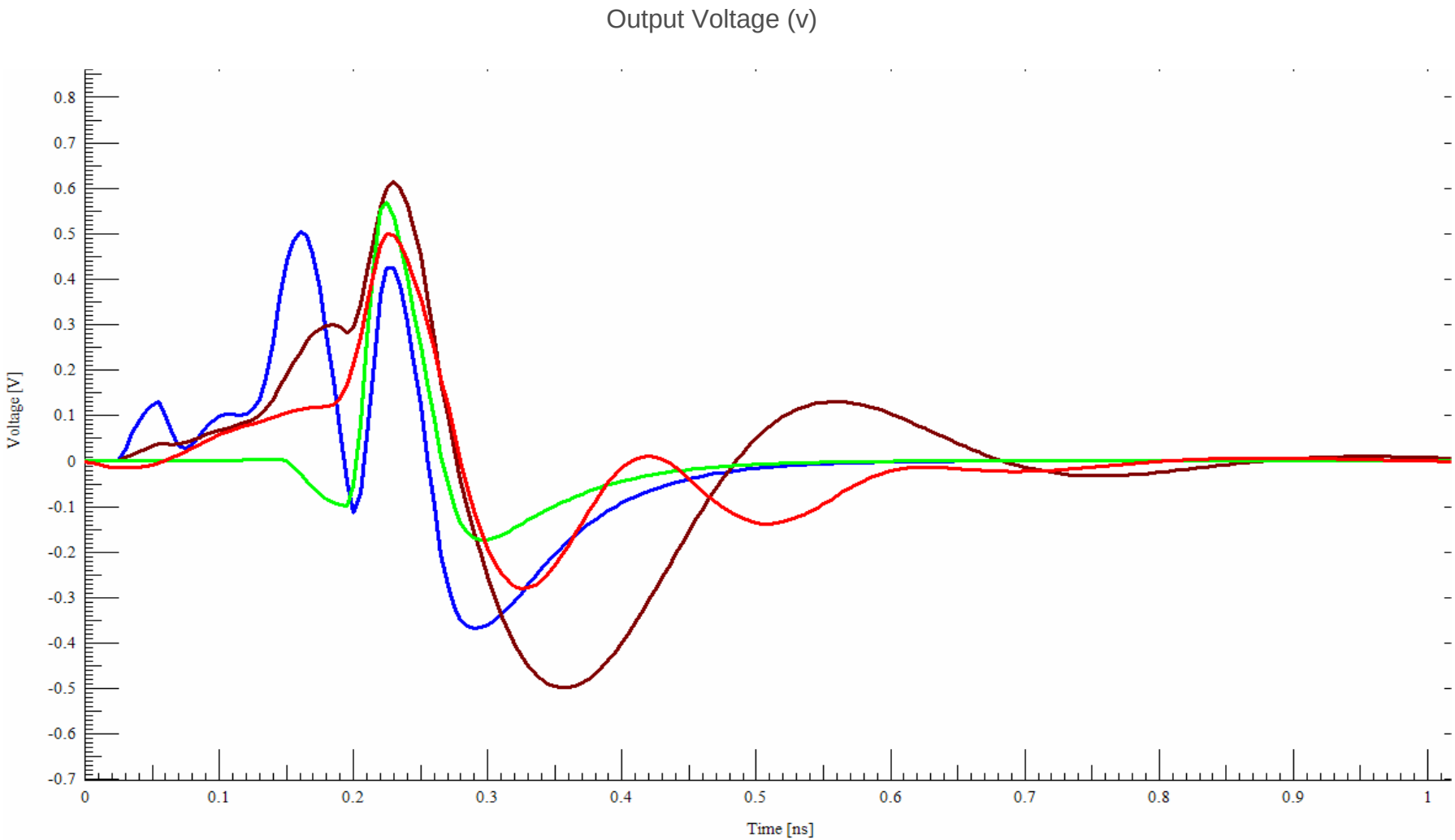
Test Case 4 – Falling – DDDQ – Quiet Line



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Conclusions and Suggestions

- Quiet line results (Magnitudes and Phases) do not meet our minimum expectations yet
  - Suggest CISCO to do such tests as well
- BIRD 95 method is getting worse when loop between Power/Ground and Output is established
- Cisco's test configuration in DAC presentation is one of many test cases only
- Time References (T) in the "Composite Current" are changed when Network is changing. It is network dependant.
- ZVDDQ played big role in our test cases. We believe it should be highlighted very strongly in the BIRD95 text.
- The HSpice Transistor-Level model and its IBIS Model that used in presented results are available for all committee members and technical experts to do the tests.
  - Send the request to Lance Wang (lwang@cadence.com)