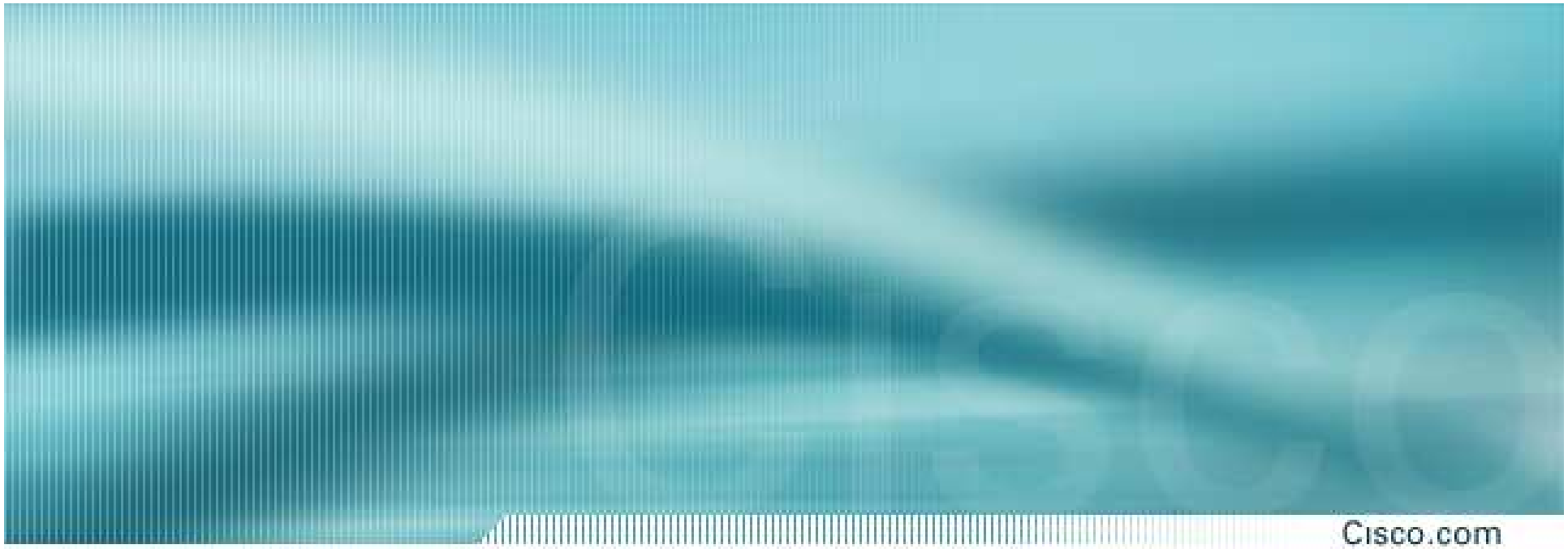

BIRD95 validation with Micron Output Buffer

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Cisco Systems, Inc.

IBIS cookbook/future meeting on 8/30/05

(04/06/2005)

Acknowledgement

- Special thanks to Randy Wolff from Micron for providing the I/O buffer and valuable helps
- Arpad Muranyi from Intel to share the slides on C_comp extraction and split

Content

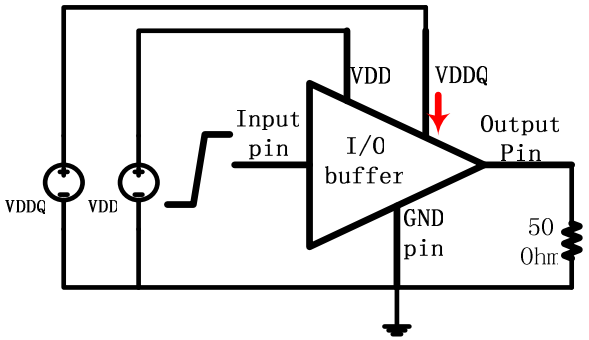
- Assumption and some findings with Micro buffer
- Extraction of IvsT under ideal voltage
- Extraction of Zvddq information and improvement
- Multi-buffer simulation conditions
- Multi-buffer simulation results
- Q&A

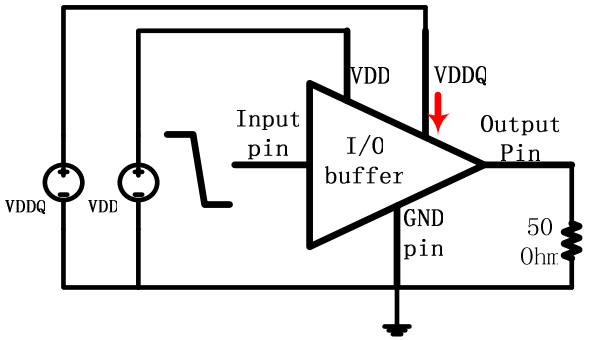
Micron Output Buffer

- Micron buffer needs several powers and control signals. They are Vccq (1.8V), Vcc(1.8V), Vccp(3.3V), Vref(0.9V), Vtt(0.9V) and other control signals
- Micron IBIS model removed some data points at the beginning of VT tables. In order to match IBIS and HSPICE in time delay, additional delay time is added to IBIS input signals
- For TYPICAL corner, Micron IBIS model has C_comp of 2.67pF. By additional studies, we change the value to 2.28pF (0.57pF to Vccq and 1.71pF to ground).
- 4, 8 or 16 Micron buffers could share a decap of 300pF with 3ohm series resistance. For this study, 8 buffers are assumed, so 37.5pF capacitance with 24ohm series resistance is added to each individual HSPICE buffer model.
- The full-drive strength buffer at typical corner is studied.

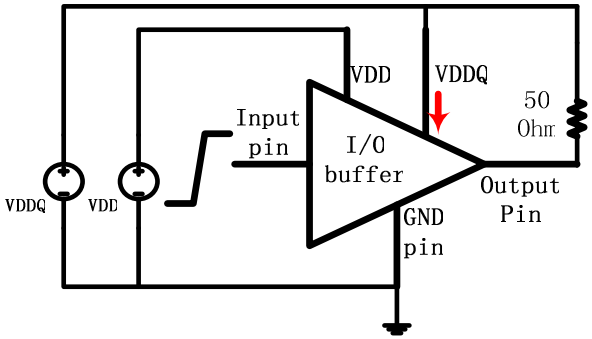
Extraction of IvsT

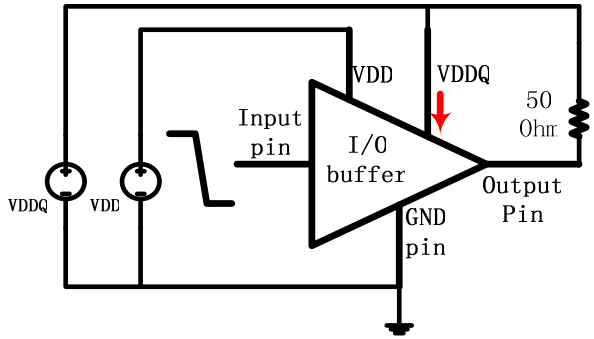
50 Ohm to GND



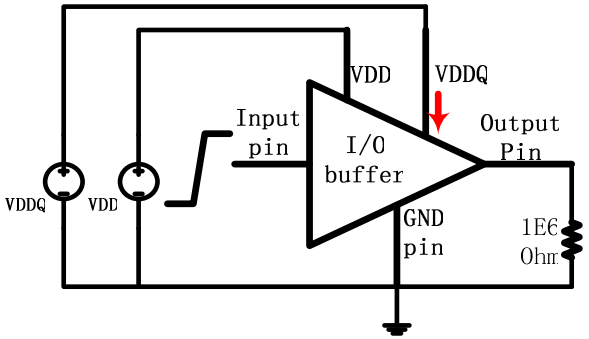


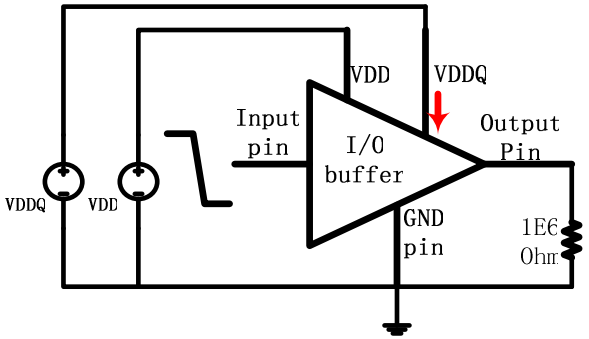
50 Ohm to VDDQ



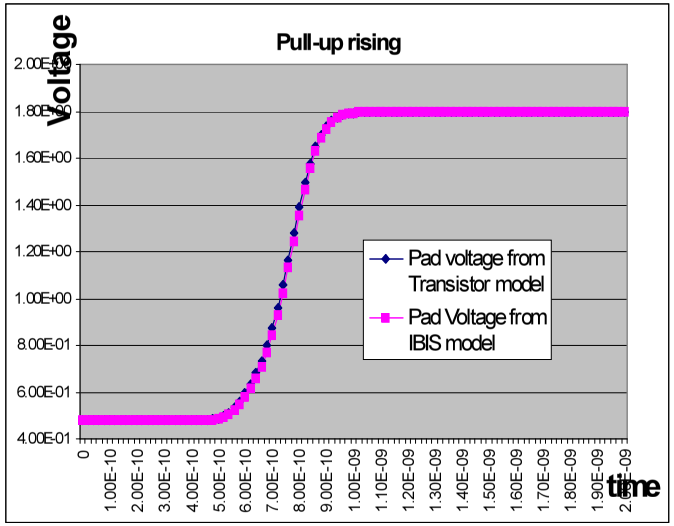


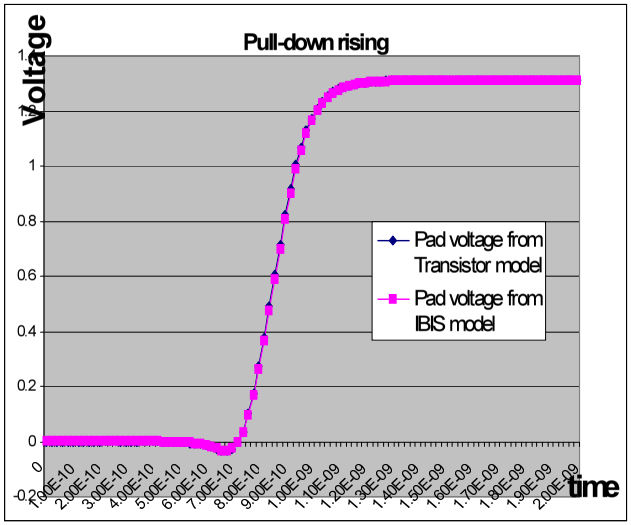
Open Load

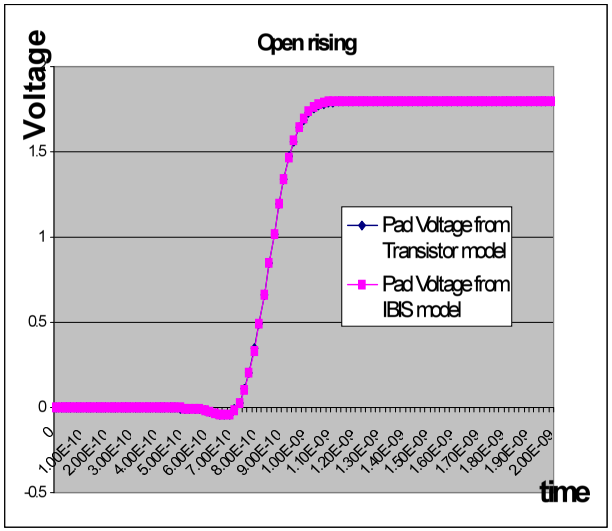


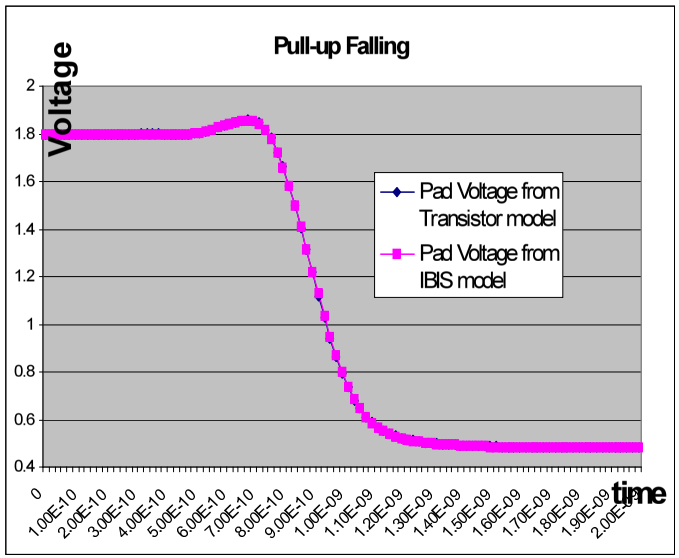


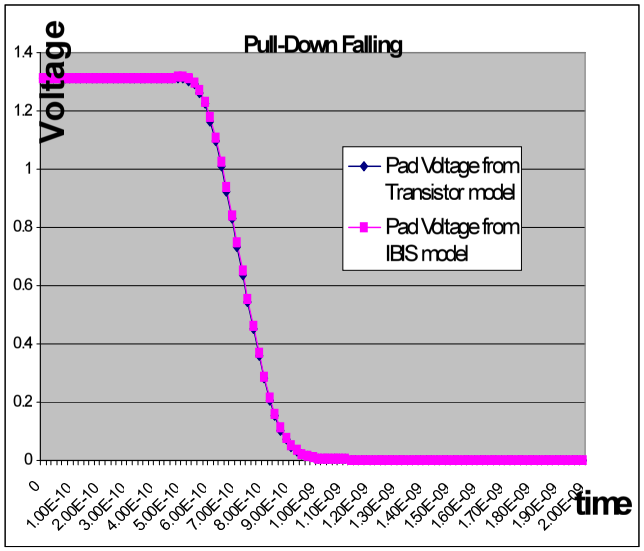
Voltage waveforms under ideal power conditions

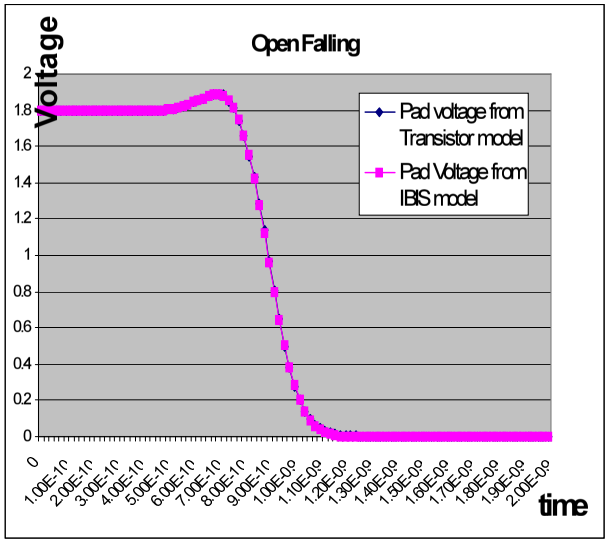




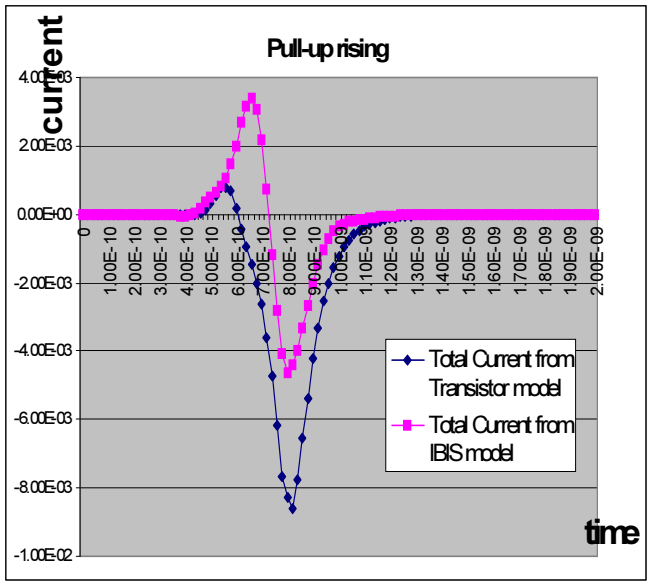


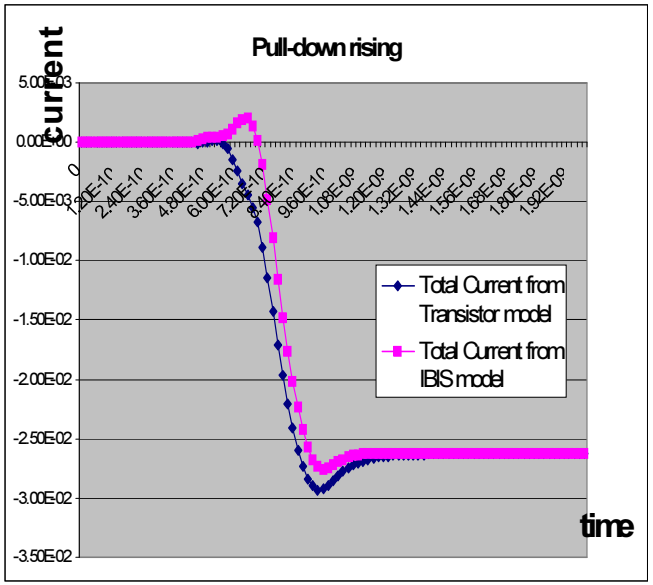


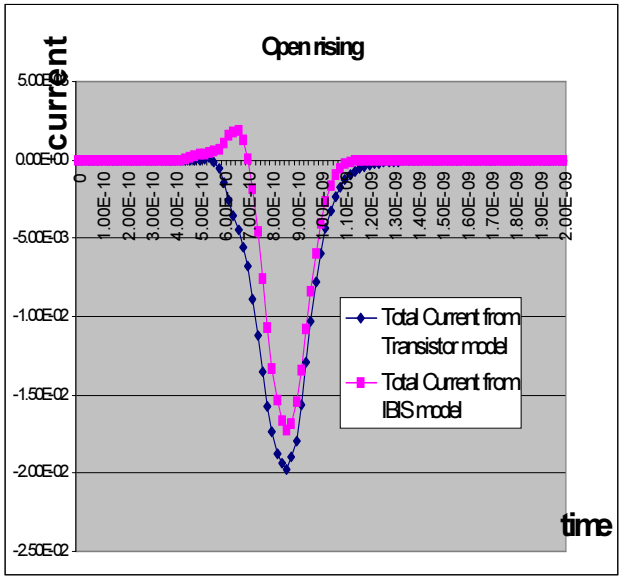


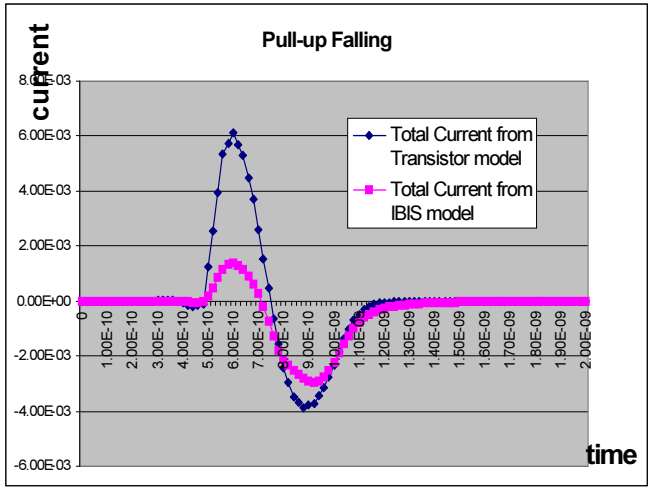


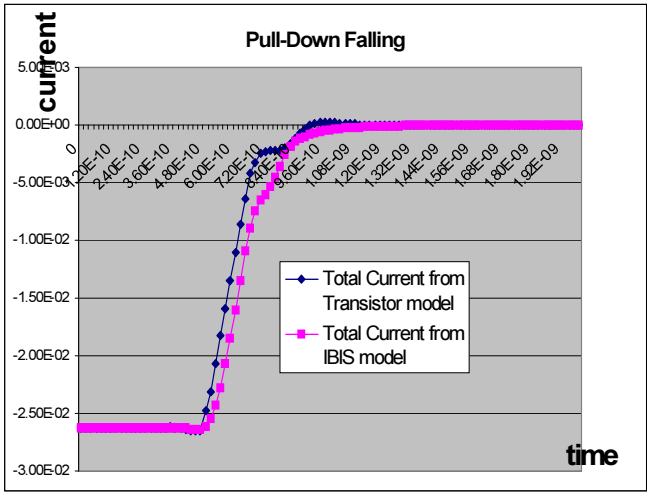
Current waveforms under ideal power conditions

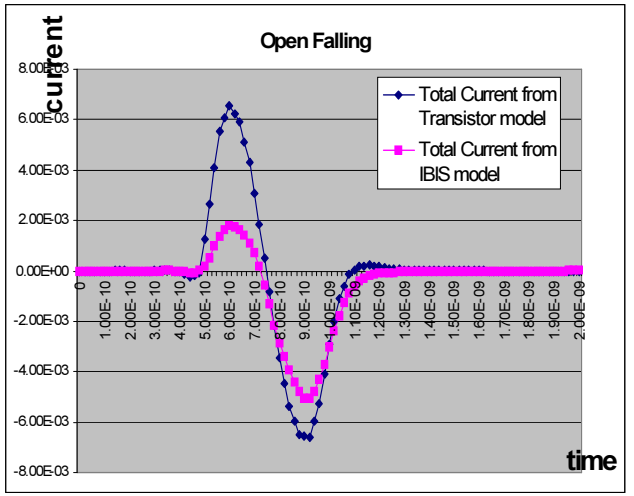




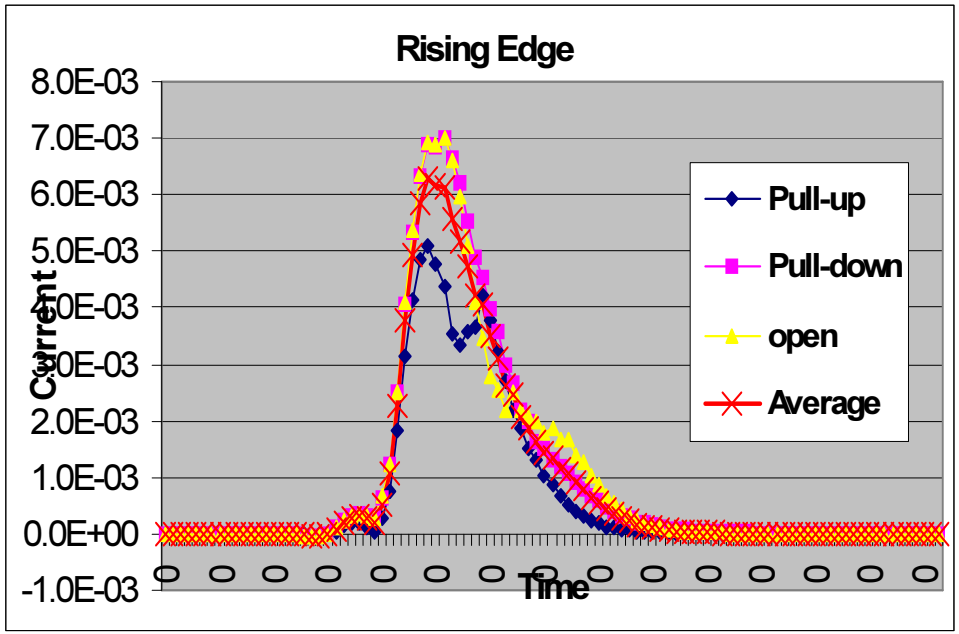


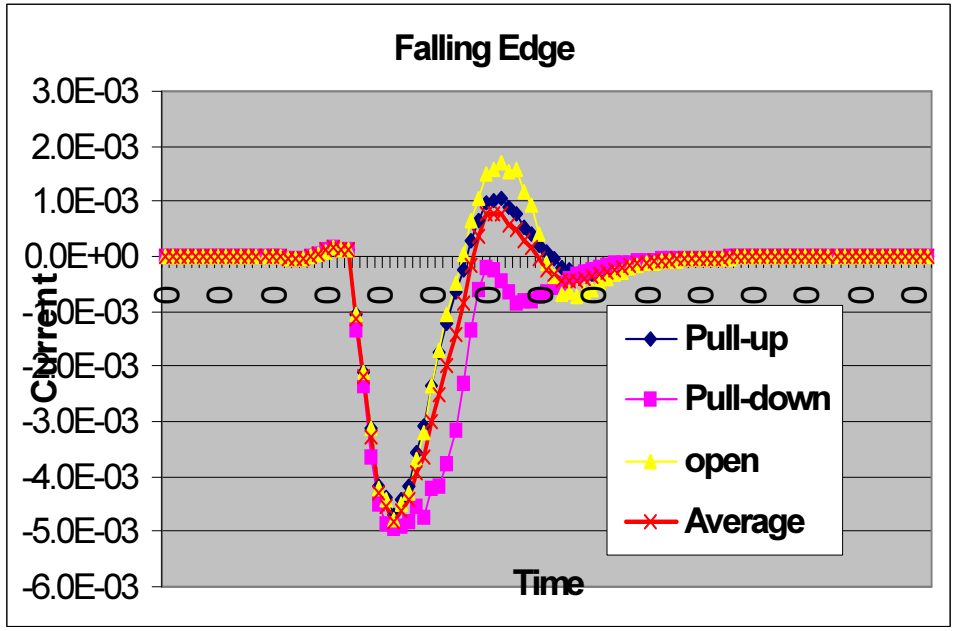




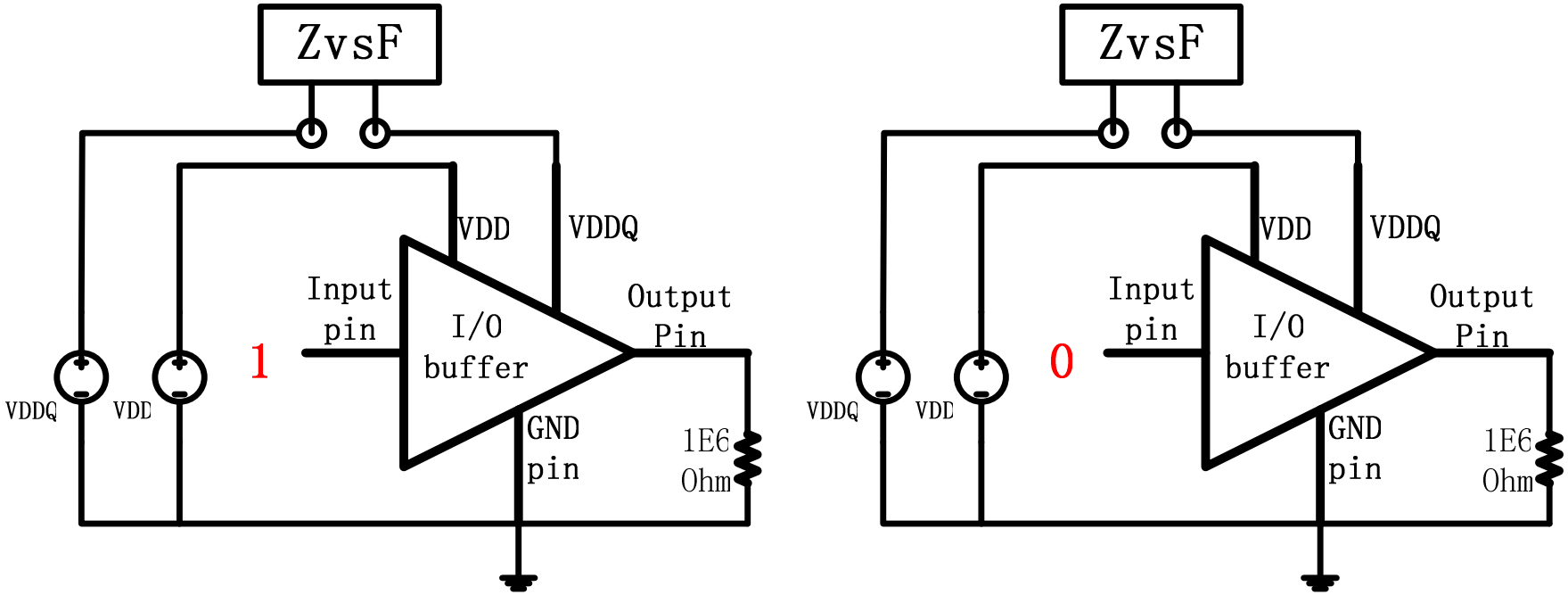


Compensation current waveforms





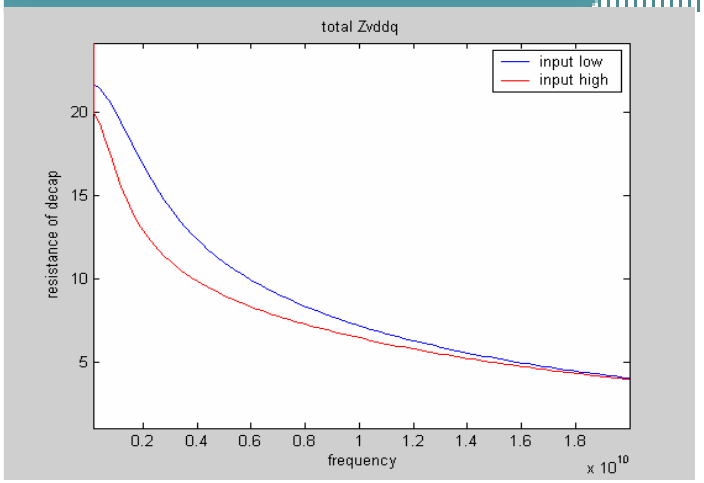
Extraction of Zvddq

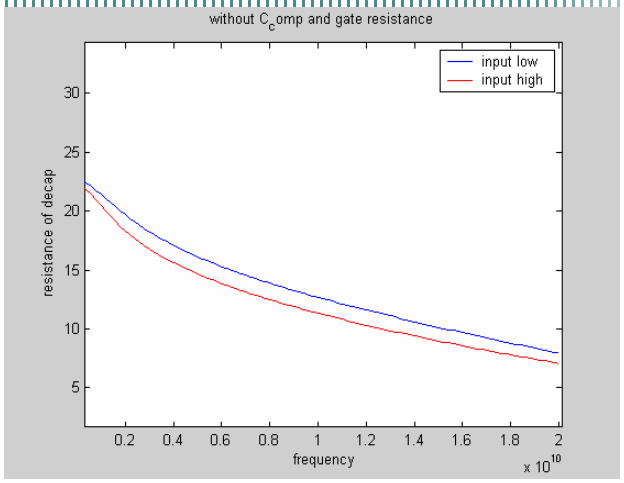


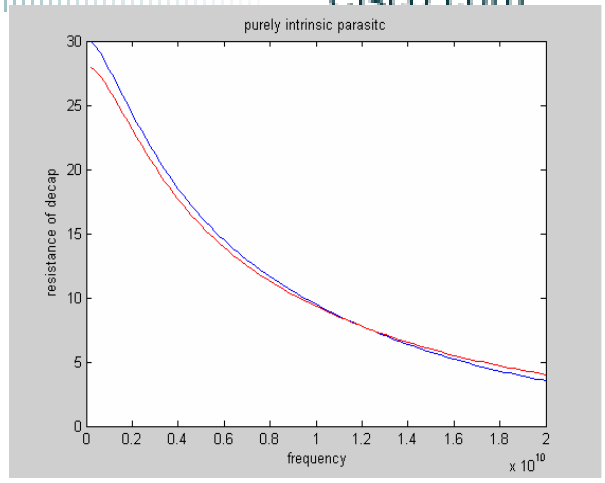
Improvement on Zvddq implemenation

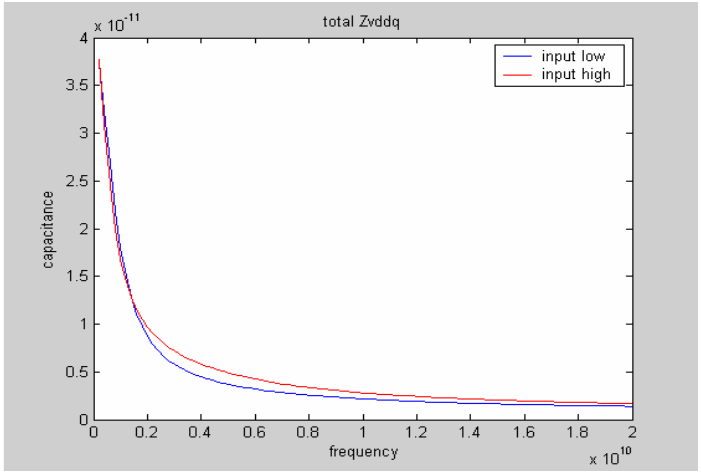
- Removed the C_comp effect from Zvddq. C_comp and gate resistance should not be double counted since they are already included in HSPICE B-element
- Separated the intrinsic parasitic from additional decap cell

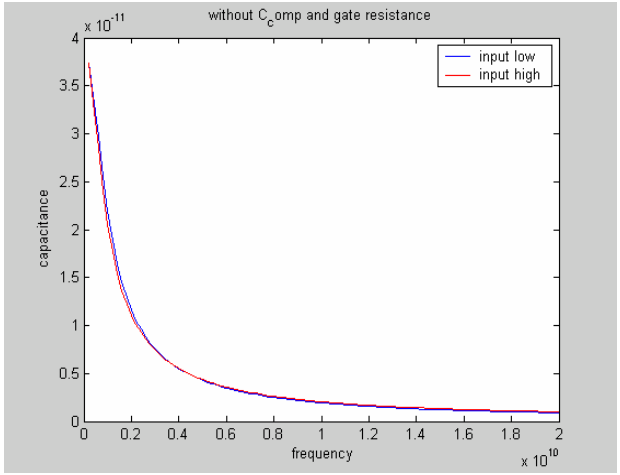
Zvddq results

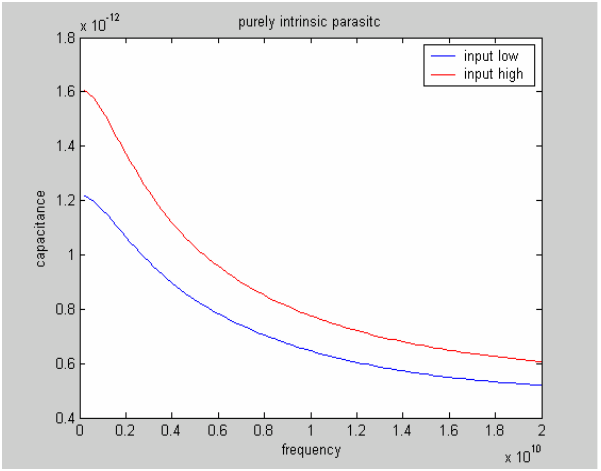










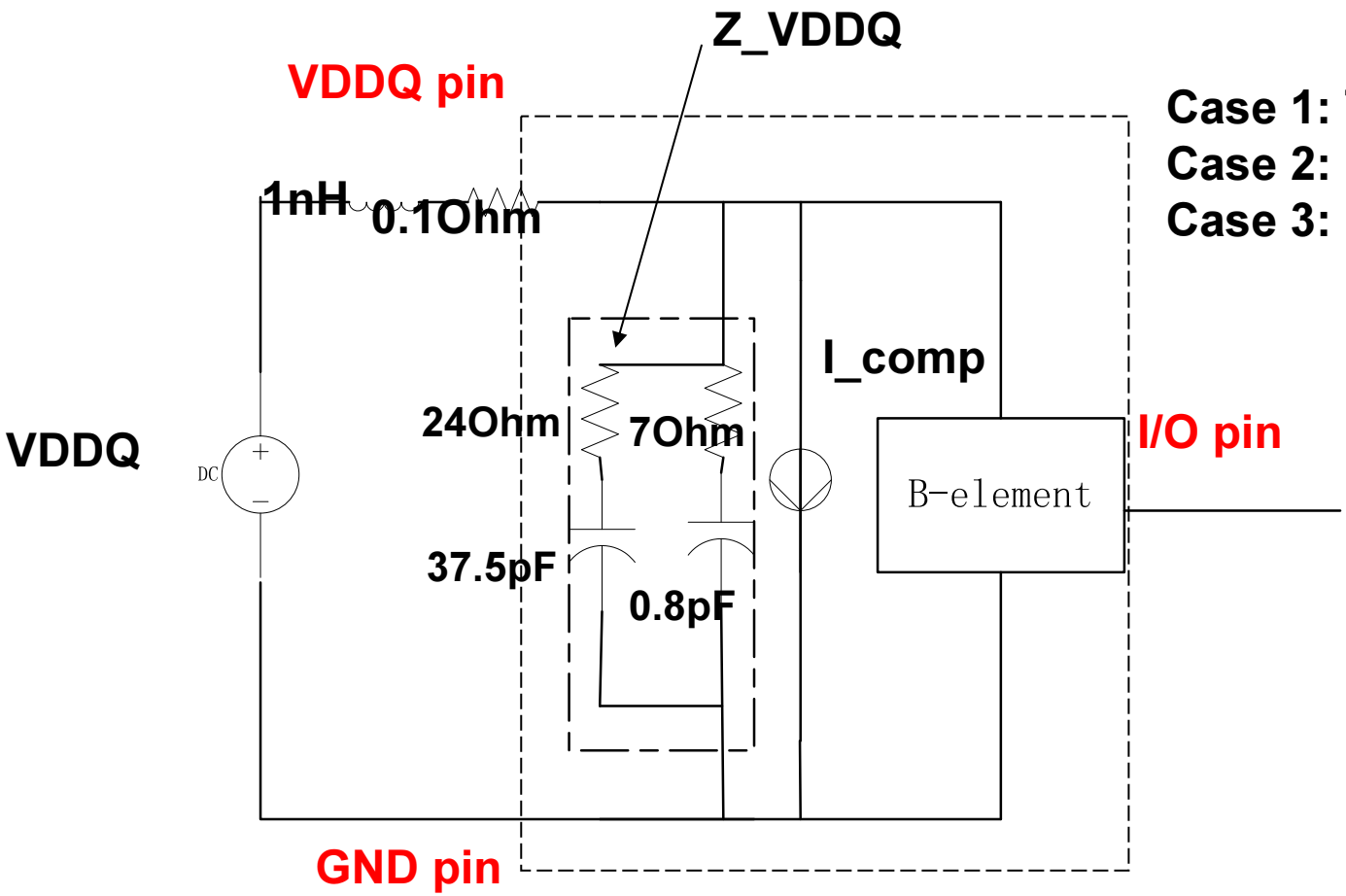


Z_total from Vddq and gnd pins

Zvddq after removing C_comp and pu and pd effects

Z_vddq from intrinsic parasitic only

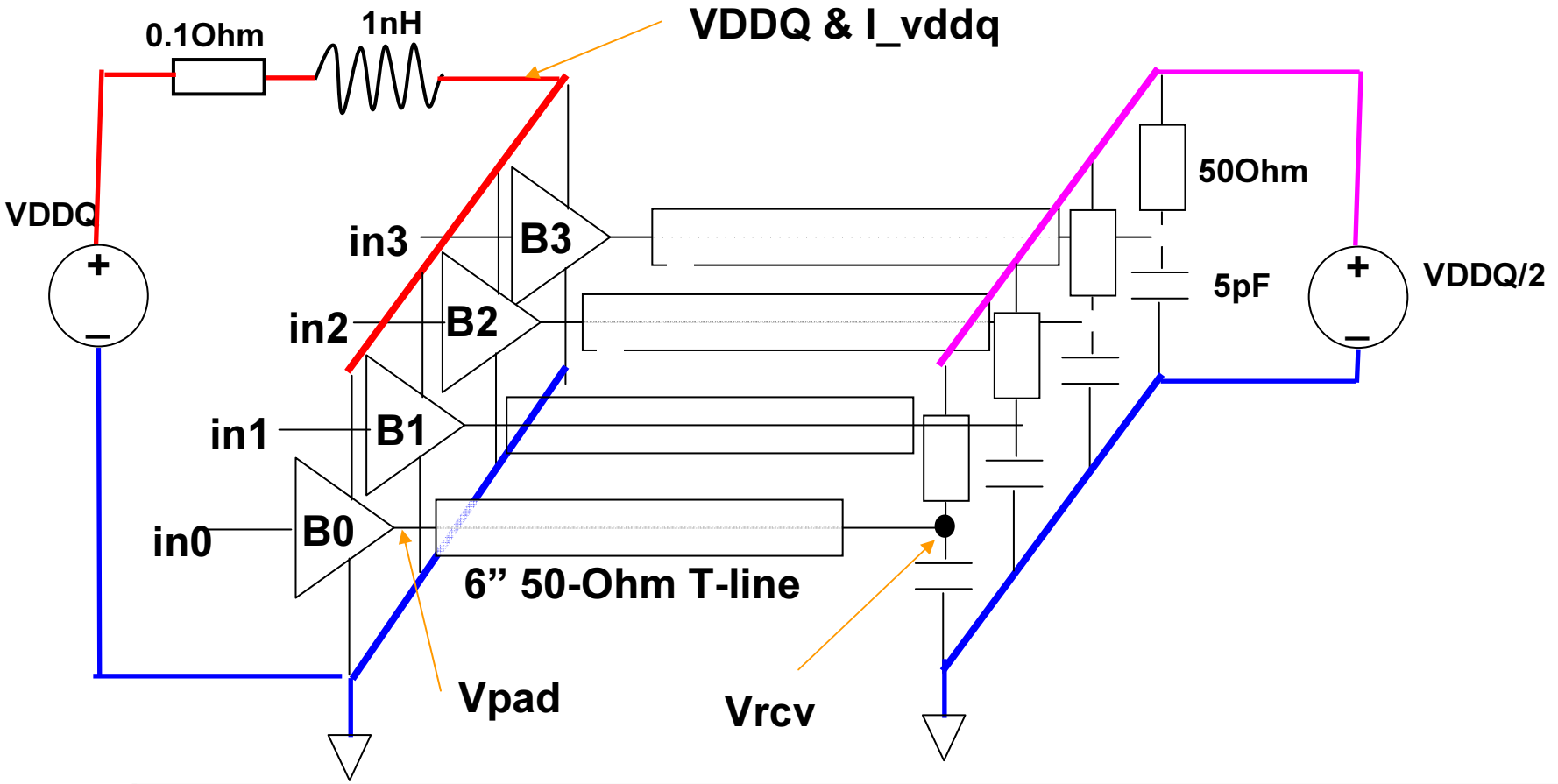
Implementation of *BIRD95* in HSPICE



Case 1: Transistor level model
Case 2: IBIS only
Case 3: IBIS with BIRD95

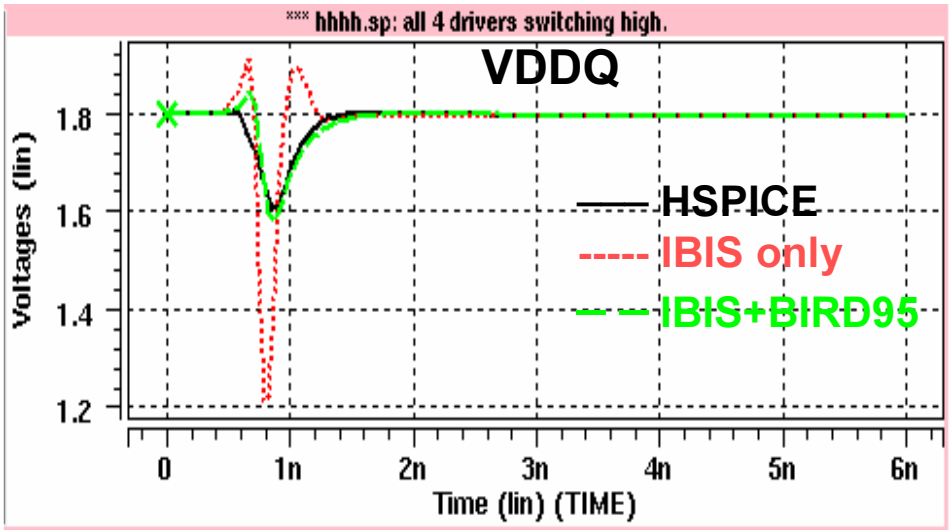
Note: IvsT* is different with IvsT table in BIRD95, but it is derived from IvsT table

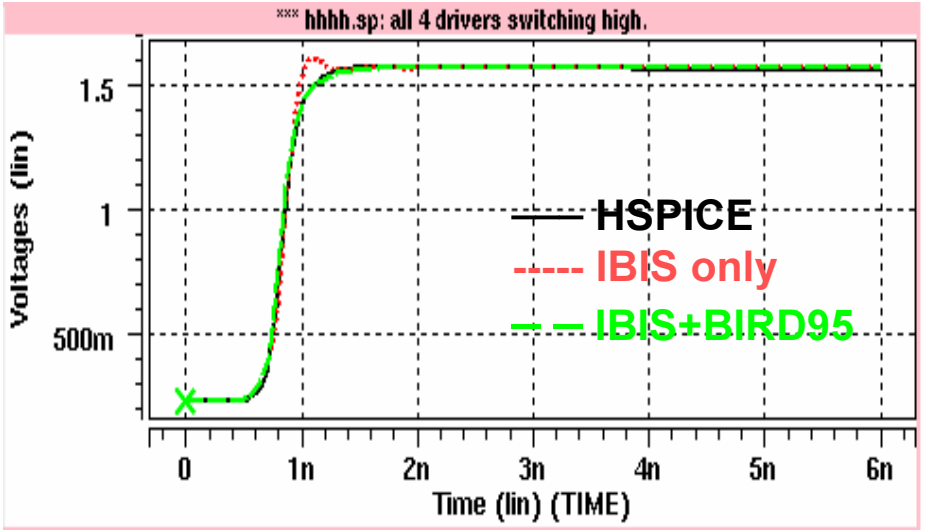
Simulation schematics

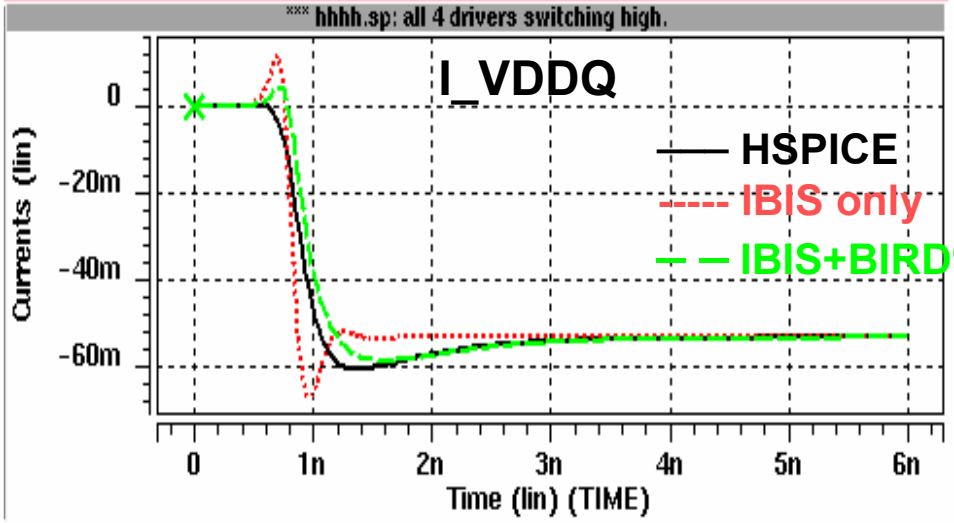


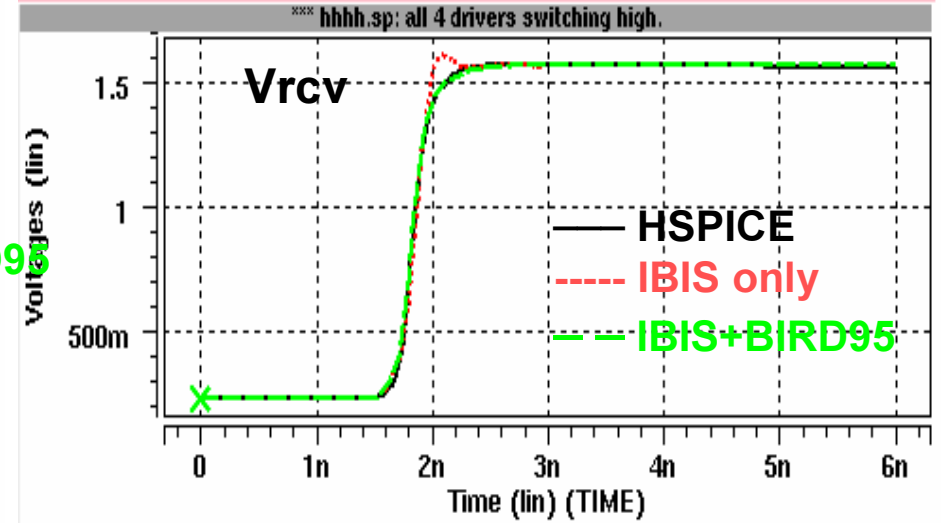
	Input date pattern					
in3210	HHHH	HHH(QH)	HHH(QL)	LLL(QH)	LLL(QL)	LLLL

Case with input pattern of HHHH

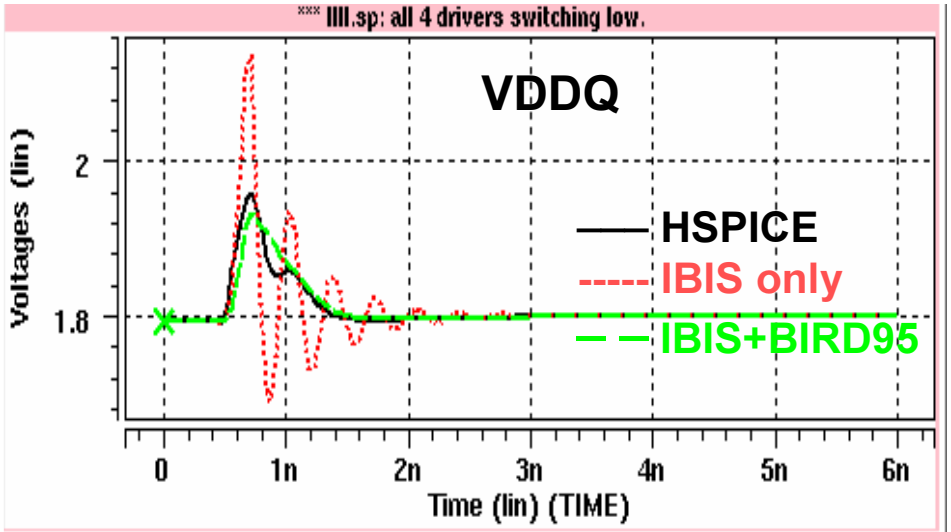


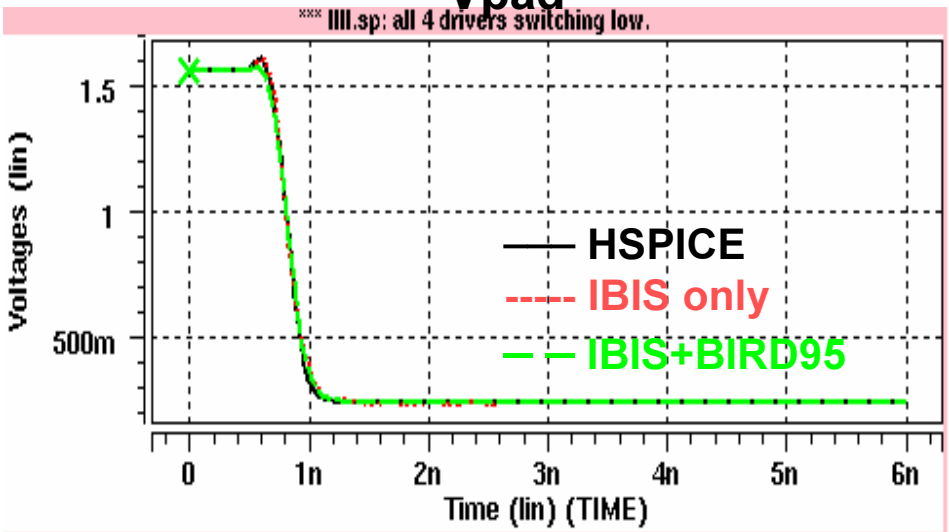


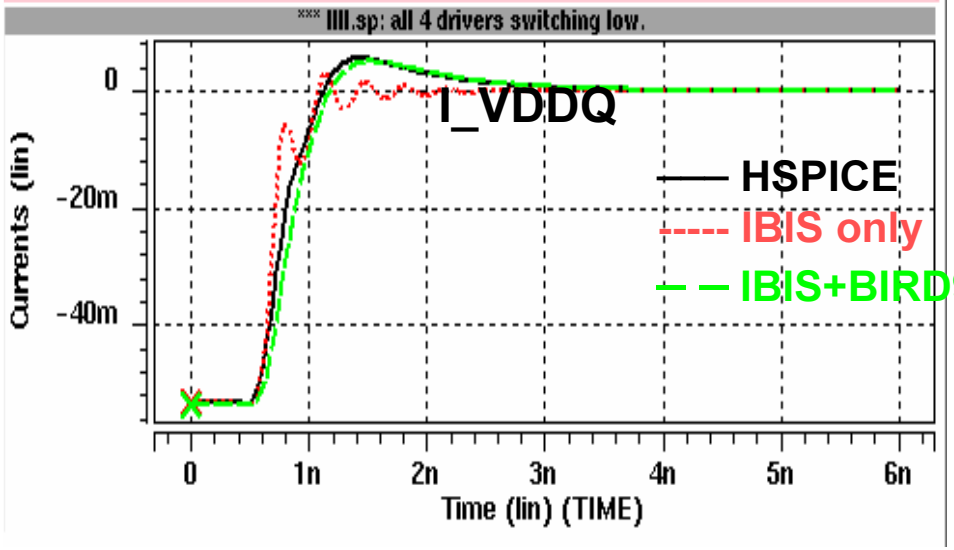


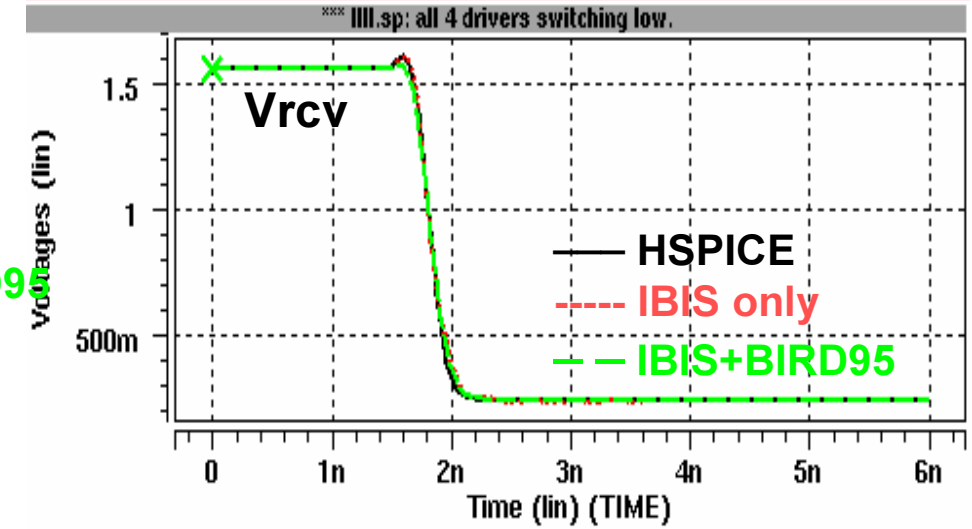


Case with input pattern of LLLL

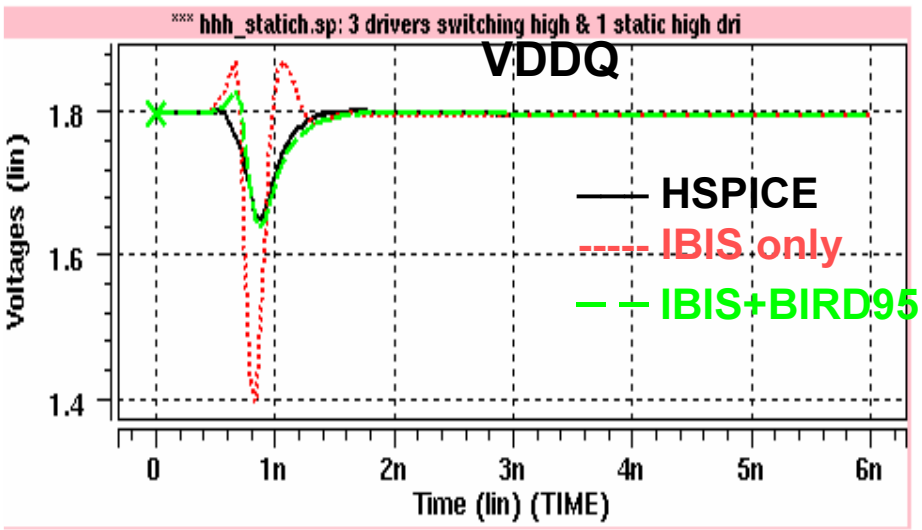


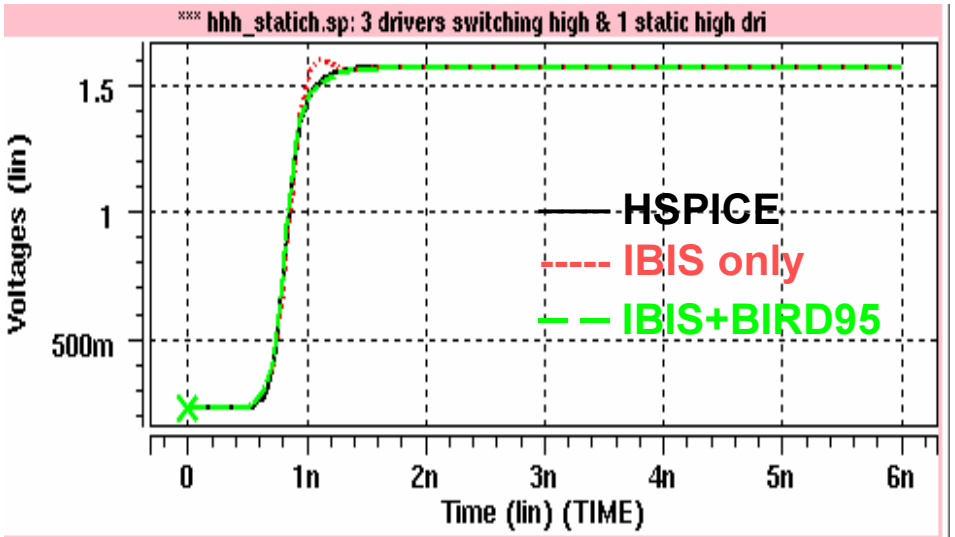


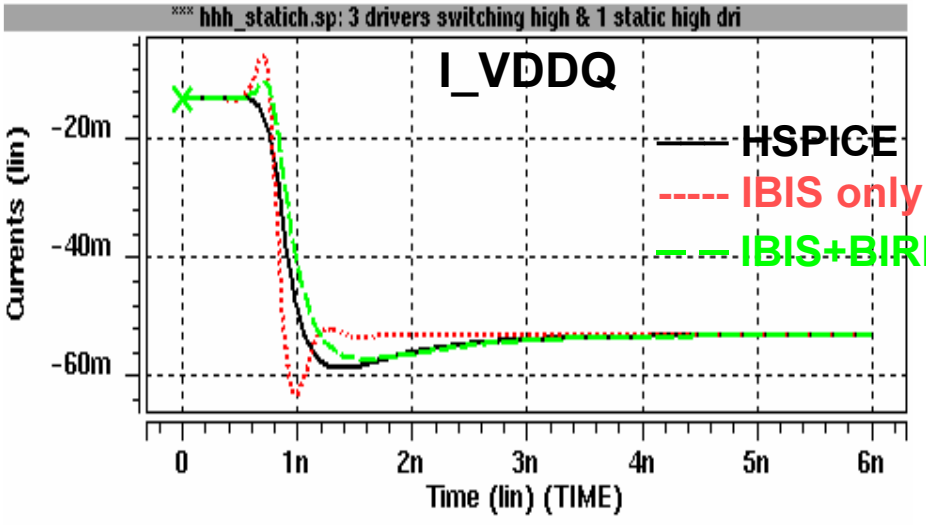


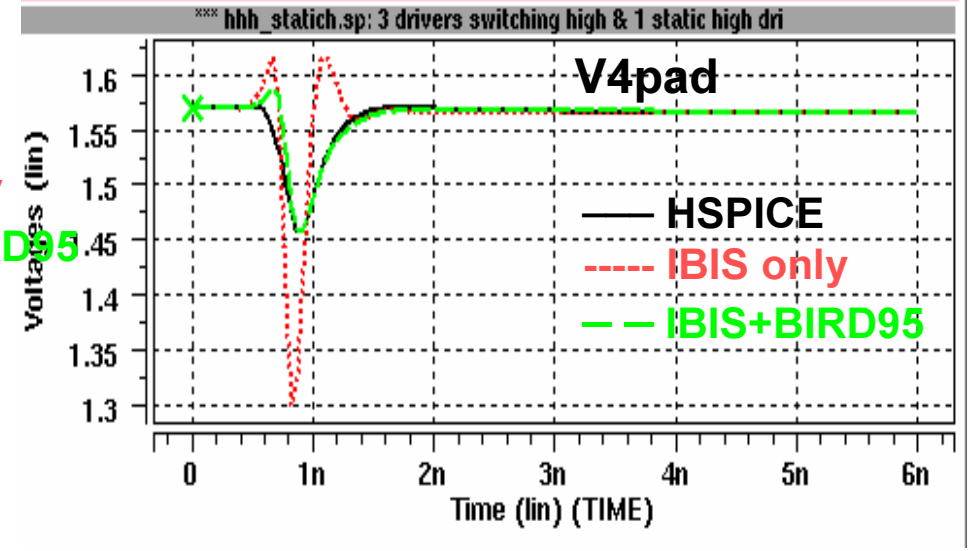


Case with input pattern of HHH(QH)

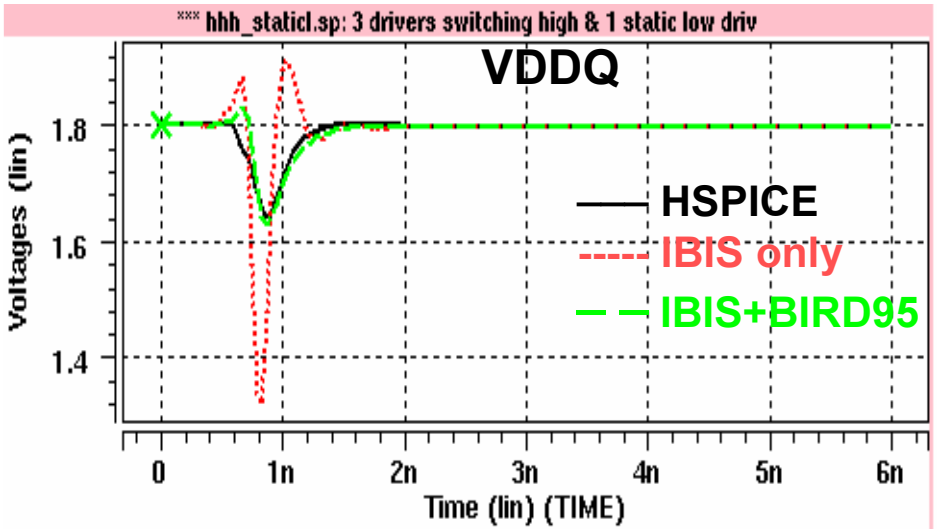


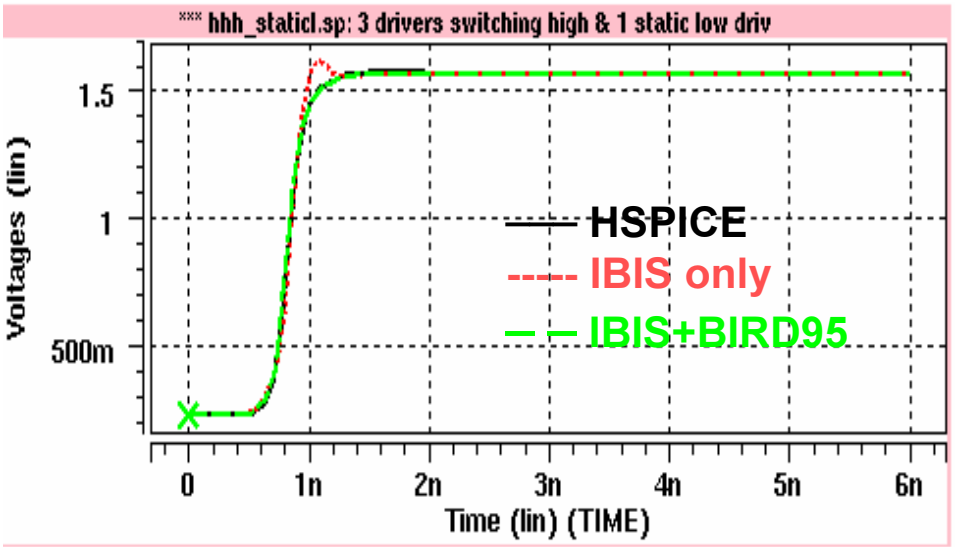


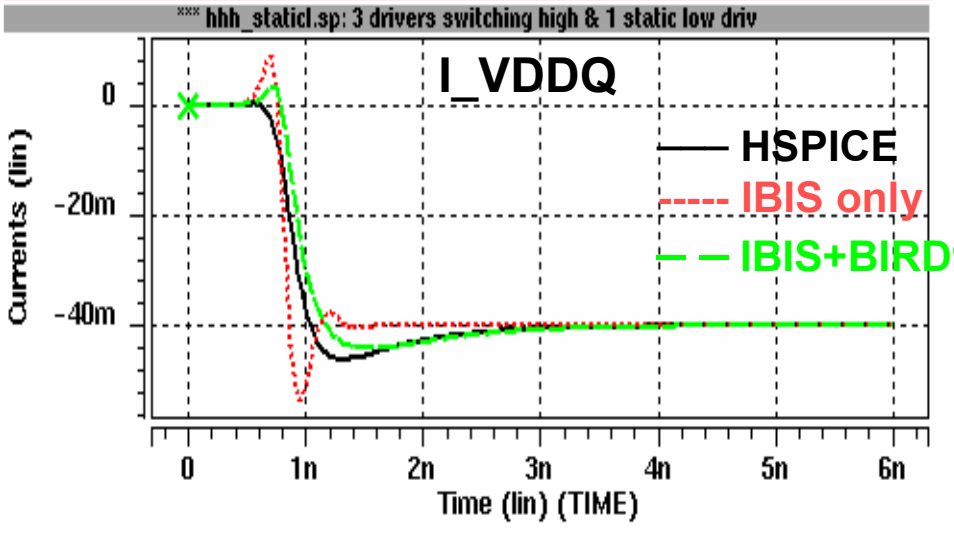


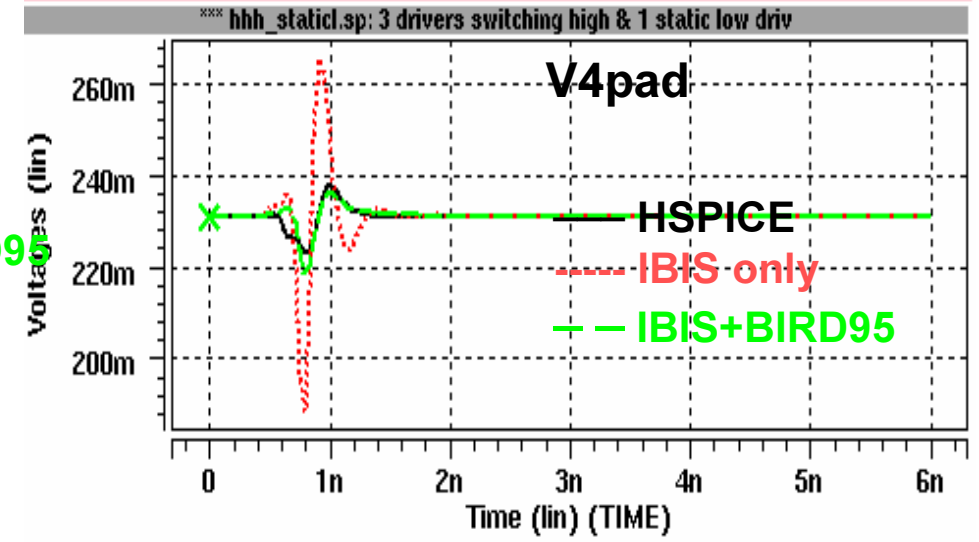


Case with input pattern of HHH(QL)

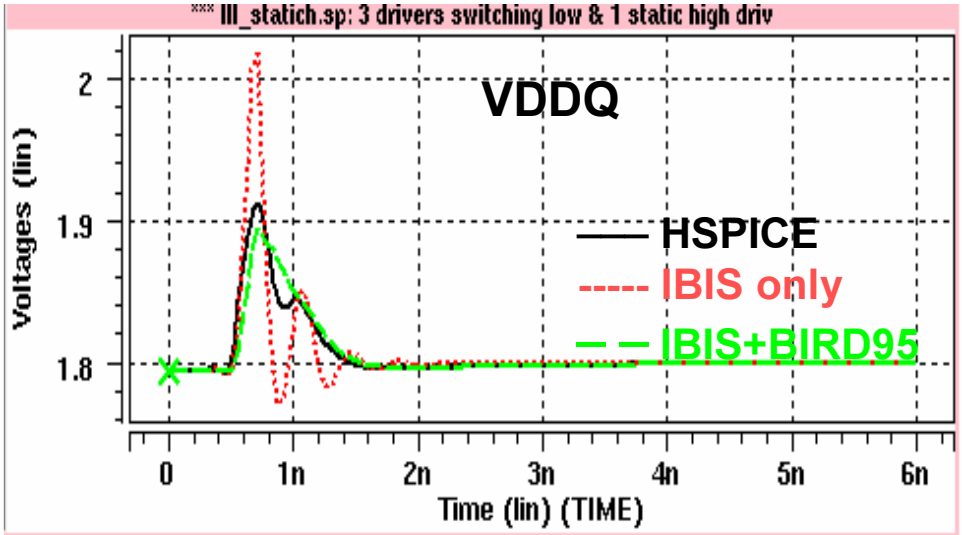


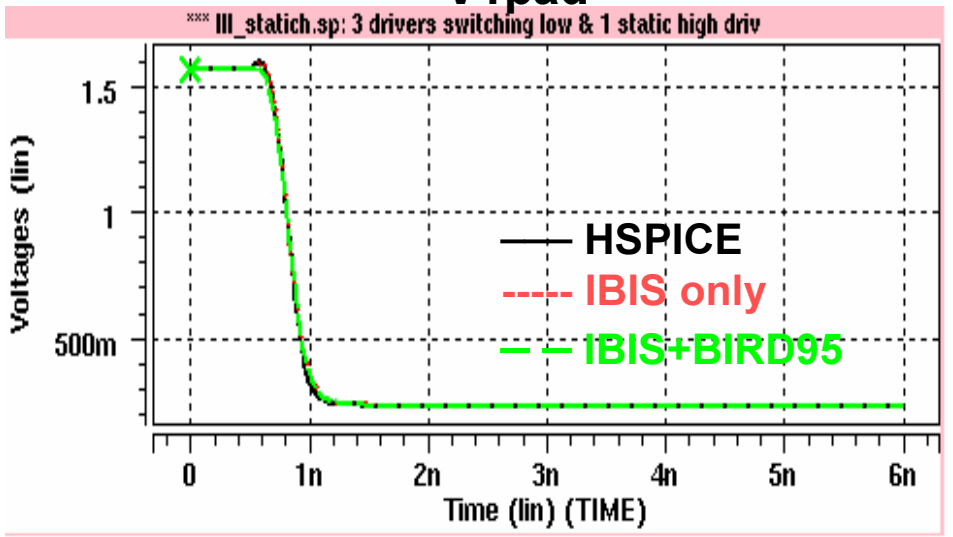


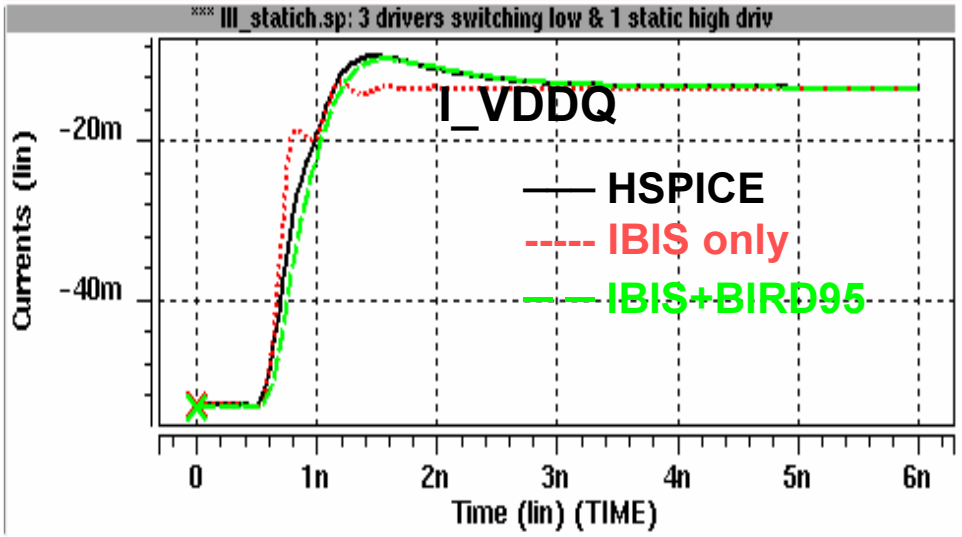


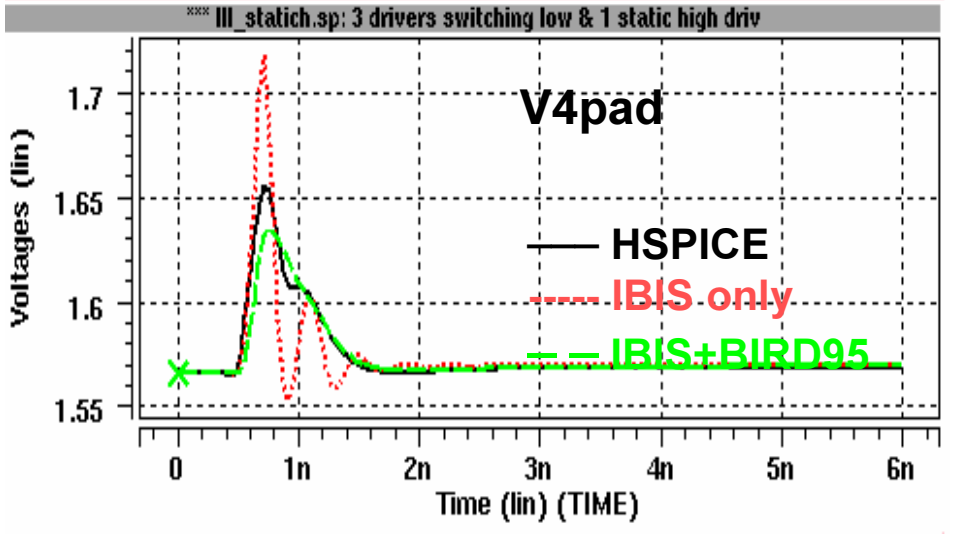


Case with input pattern of LLL(QH)

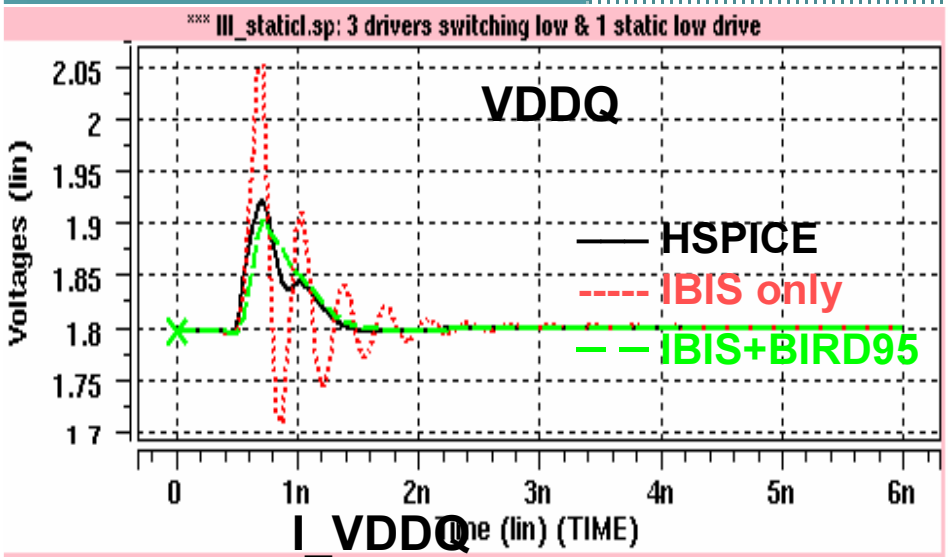


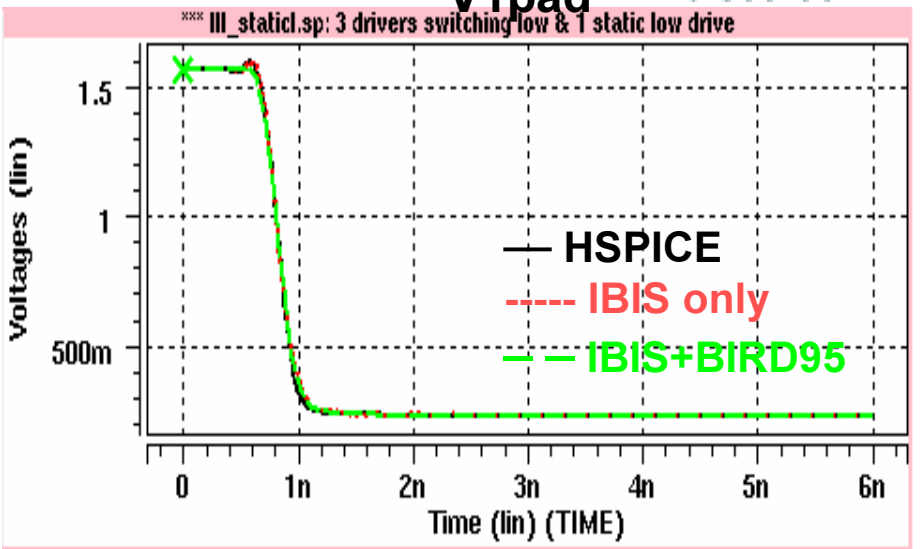


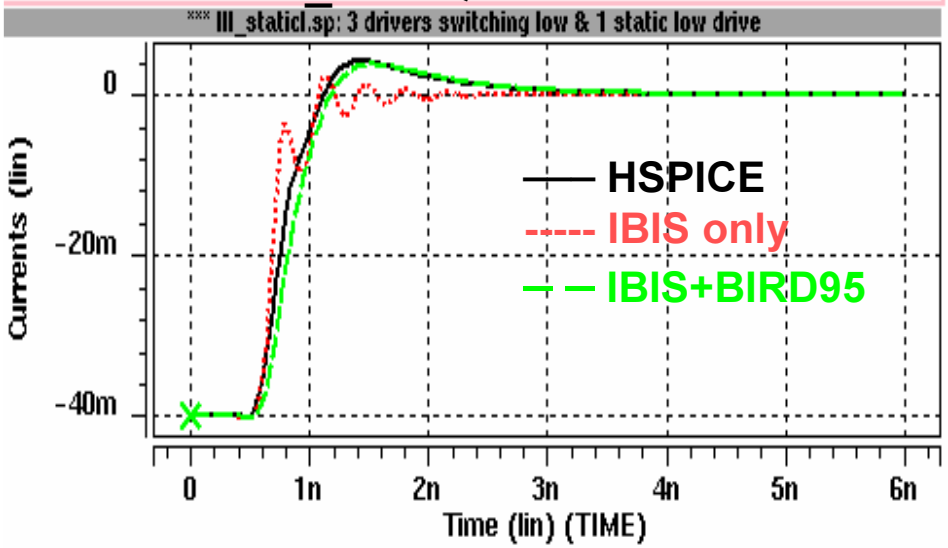


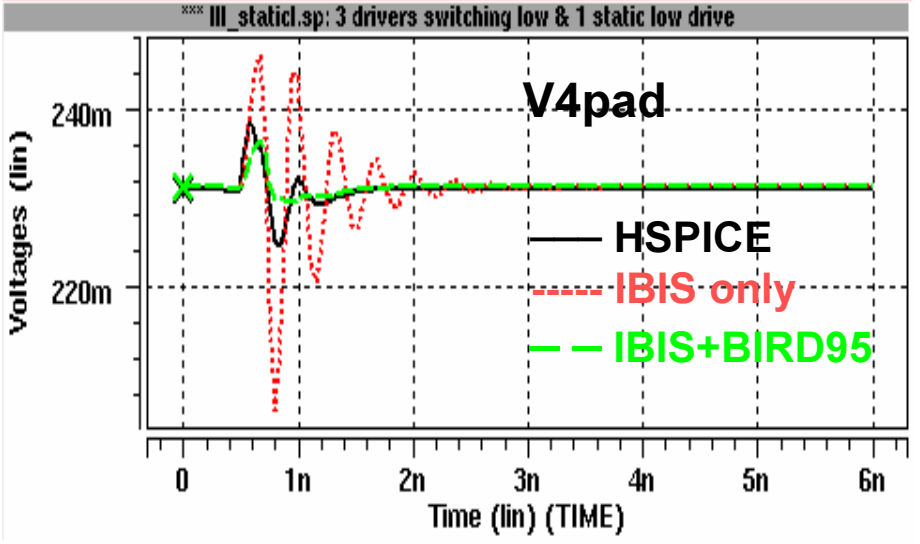


Case with input pattern of LLL(QL)









Q&A