Quiet-Line simulation results with Power or Ground changes using IBIS and HSpice transistor-level models

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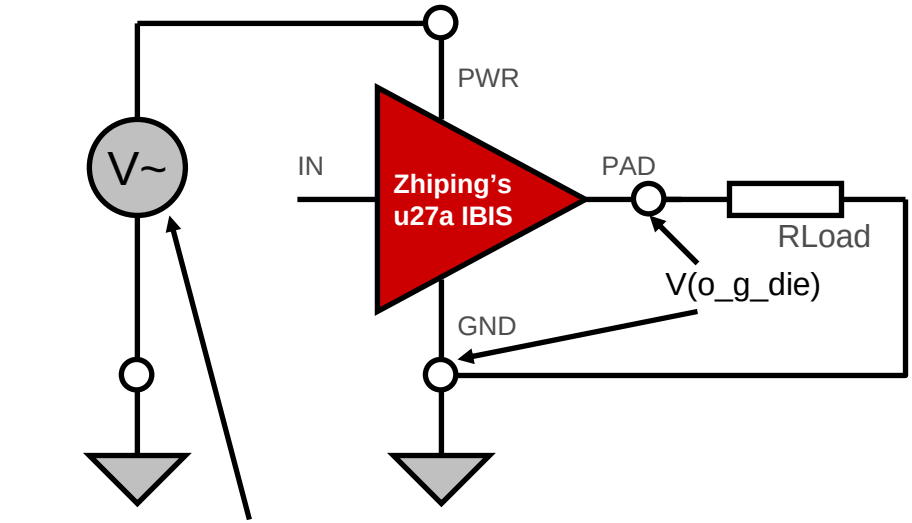
Purpose and Setting

- Model Only Power changes and Only Ground changes, but Keep Power Supply ($V_{pwr} – V_{gnd}$) as the same in both cases.
- To get whether the results (voltage between buffer output and buffer ground) are the same.
- Check both for IBIS and HSpice transistor-level models

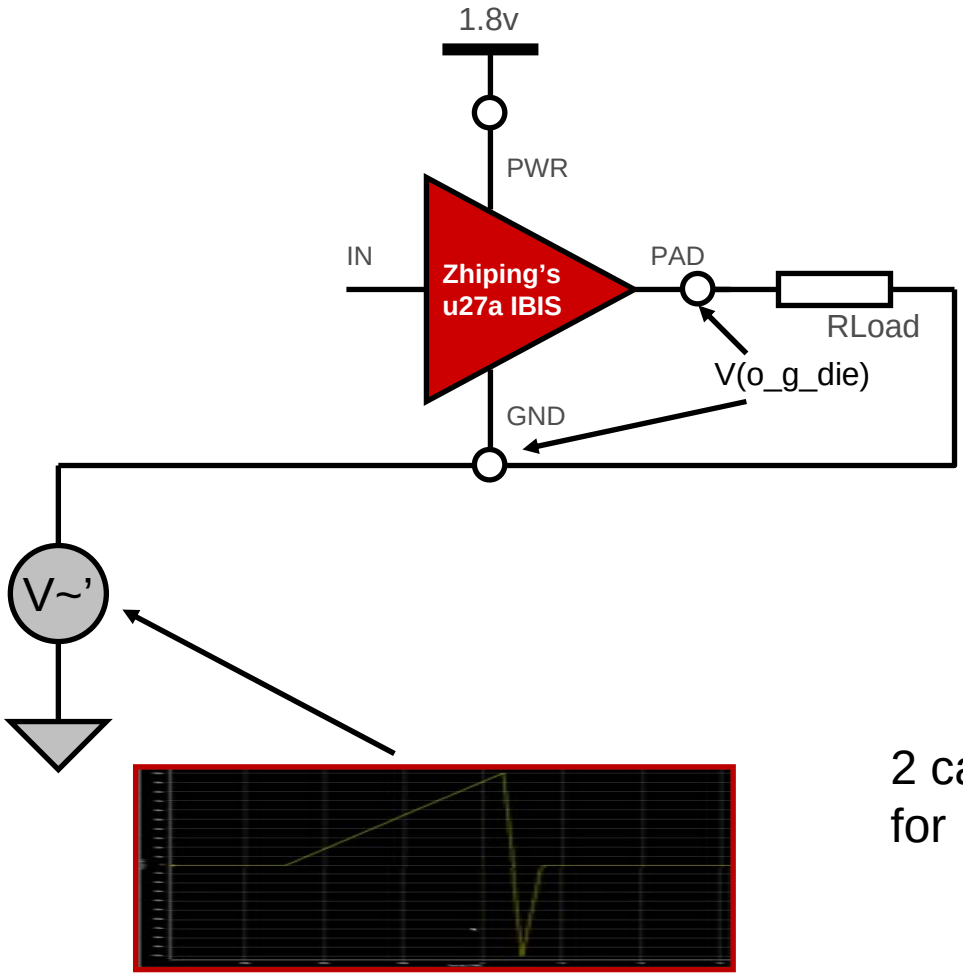
Test Results - IBIS
- Test Schematic – Power changes



2 case for Input High-static and 2 case for Input Low-static:

C_comp_pu=0.5	C_comp_pu=0.25
C_comp_pd=0.5	C_comp_pd=0.75

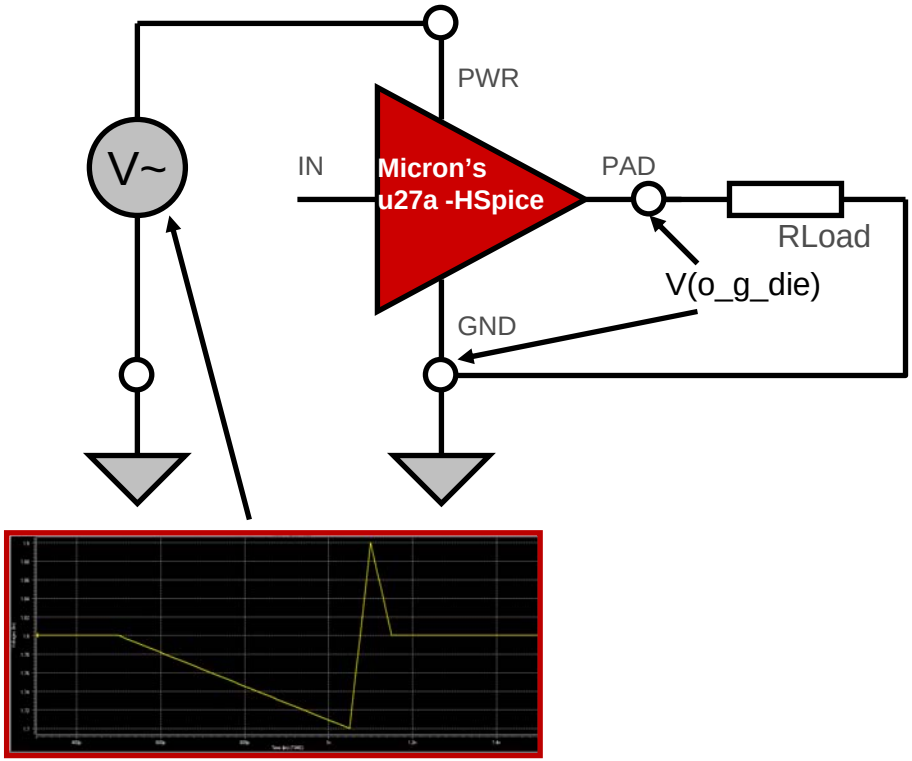
Test Results - IBIS
- Test Schematic – Ground changes



2 case for Input High-static and 2 case for Input Low-static:

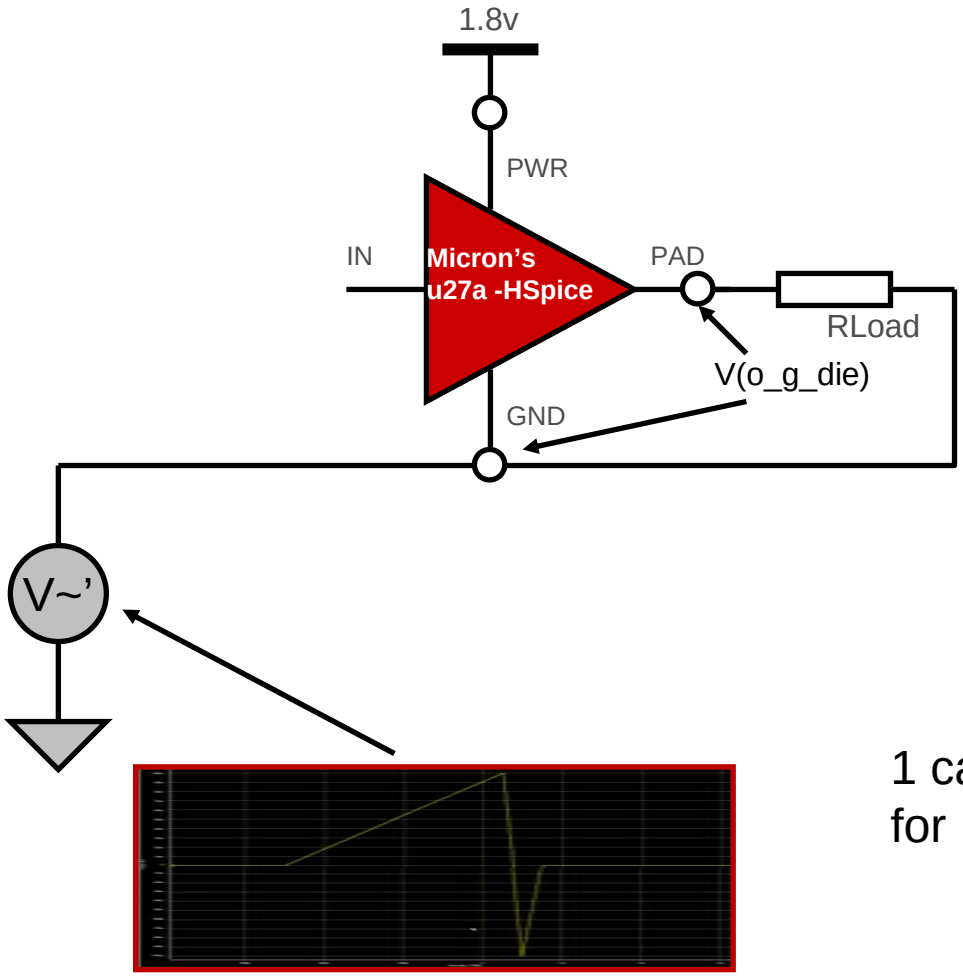
C_comp_pu=0.5	C_comp_pu=0.25
C_comp_pd=0.5	C_comp_pd=0.75

Test Results – HSpice transistor-level - Test Schematic – Power changes



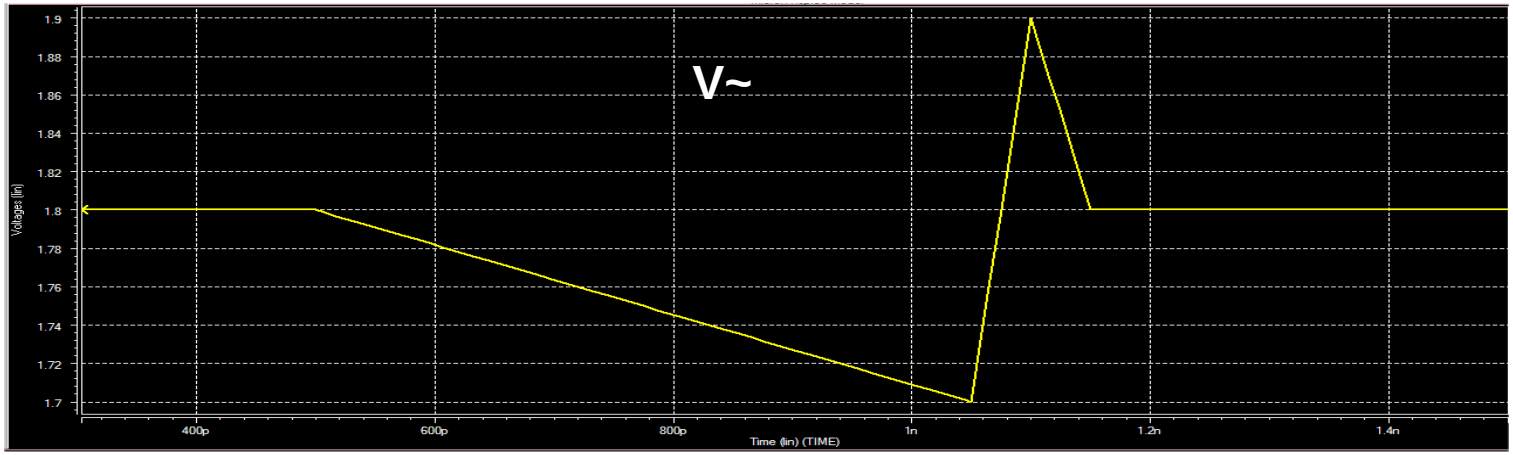
1 case for Input High-static and 1 case for Input Low-static:

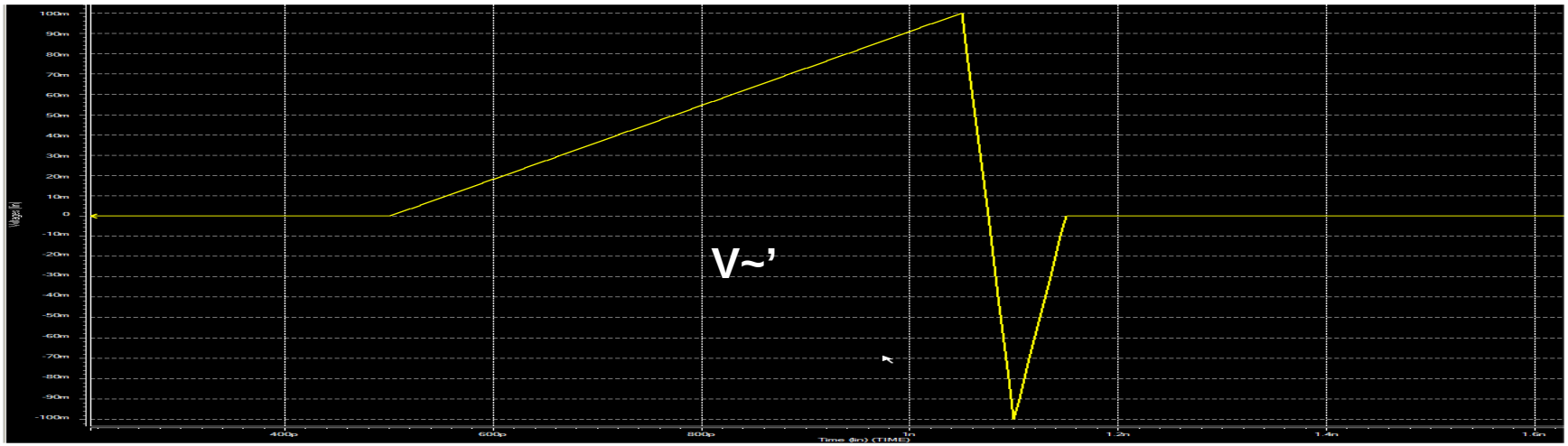
Test Results – HSpice transistor-level - Test Schematic – Ground changes



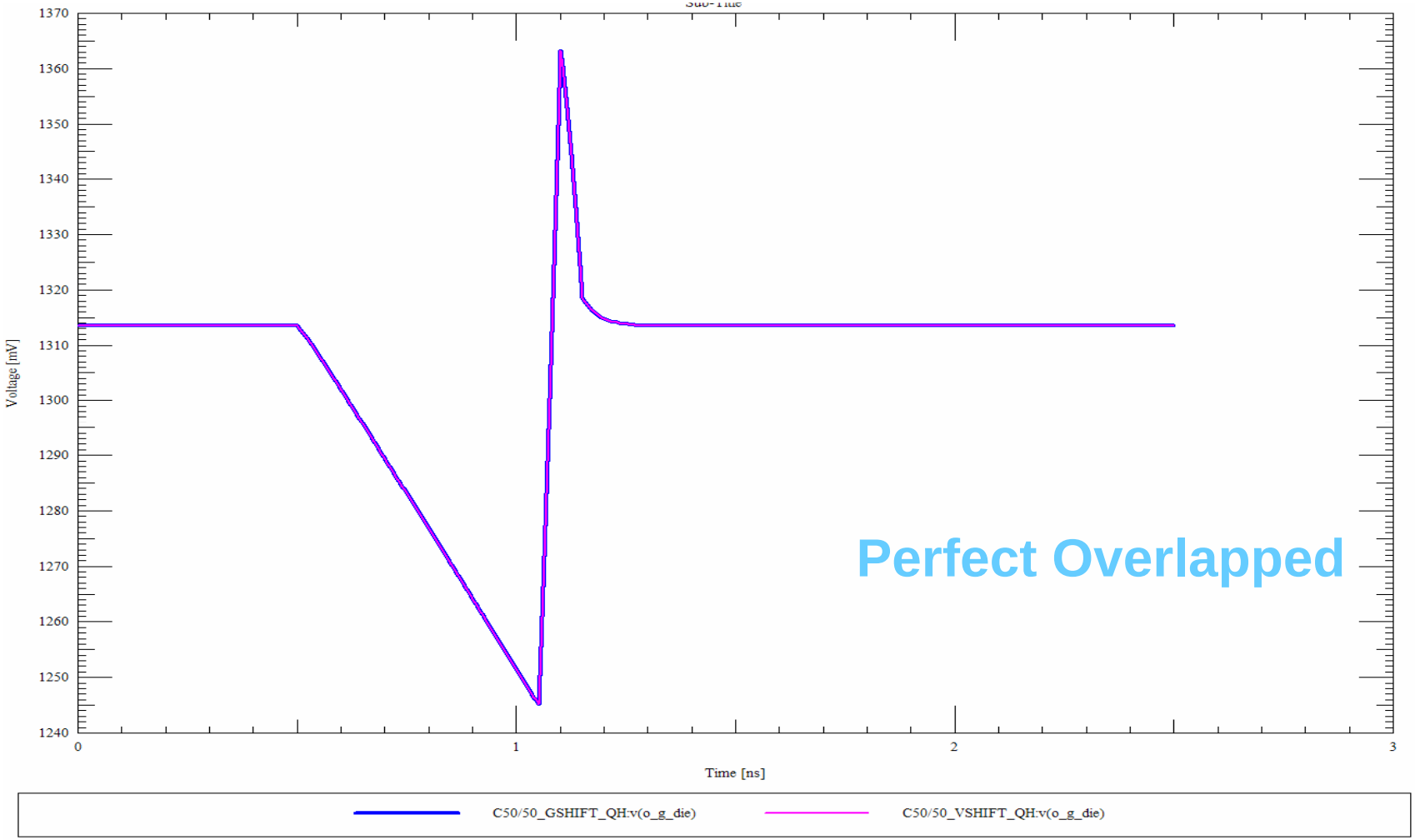
1 case for Input High-static and 1 case for Input Low-static:

Test results
- V~ and V~’ Setting

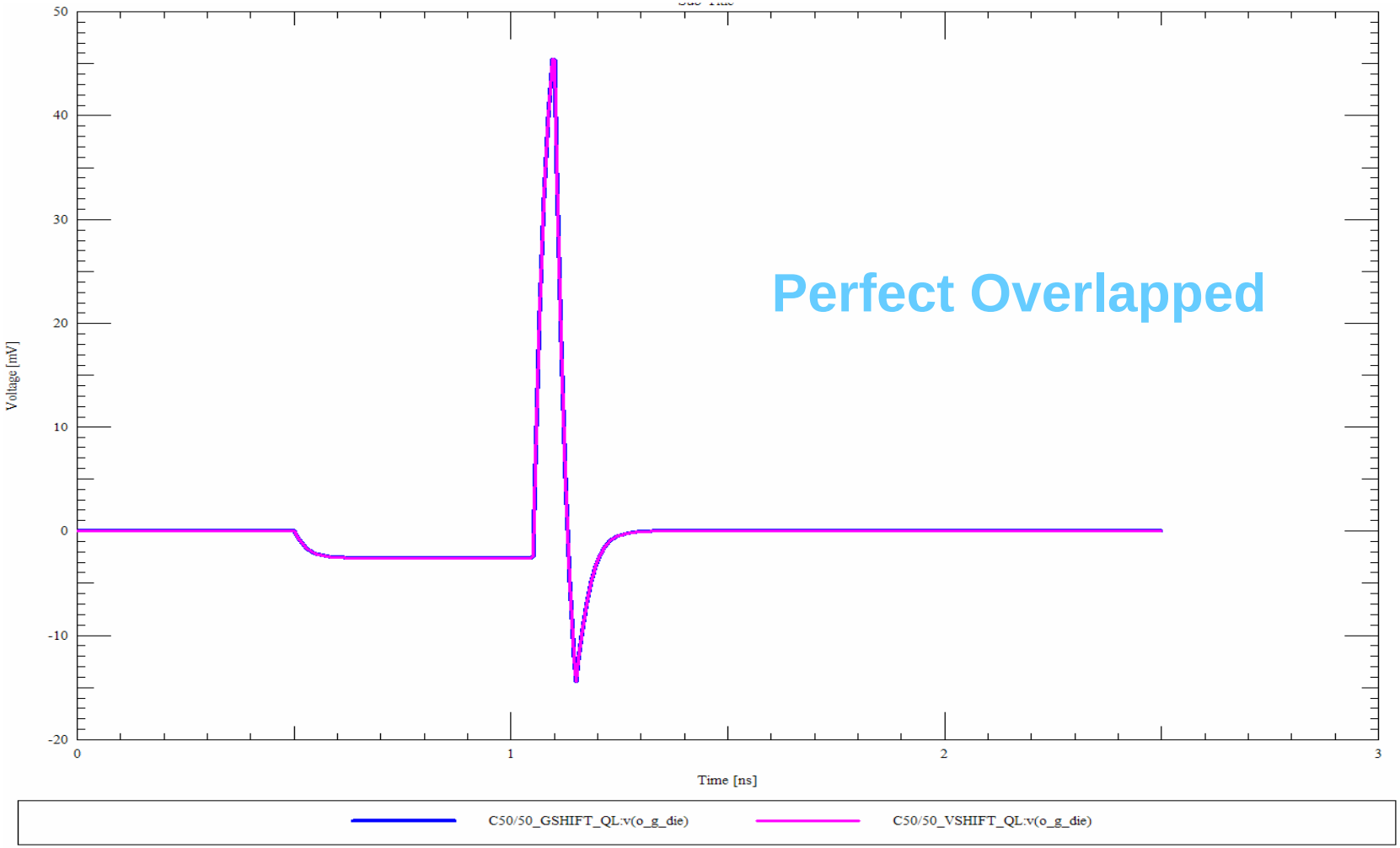




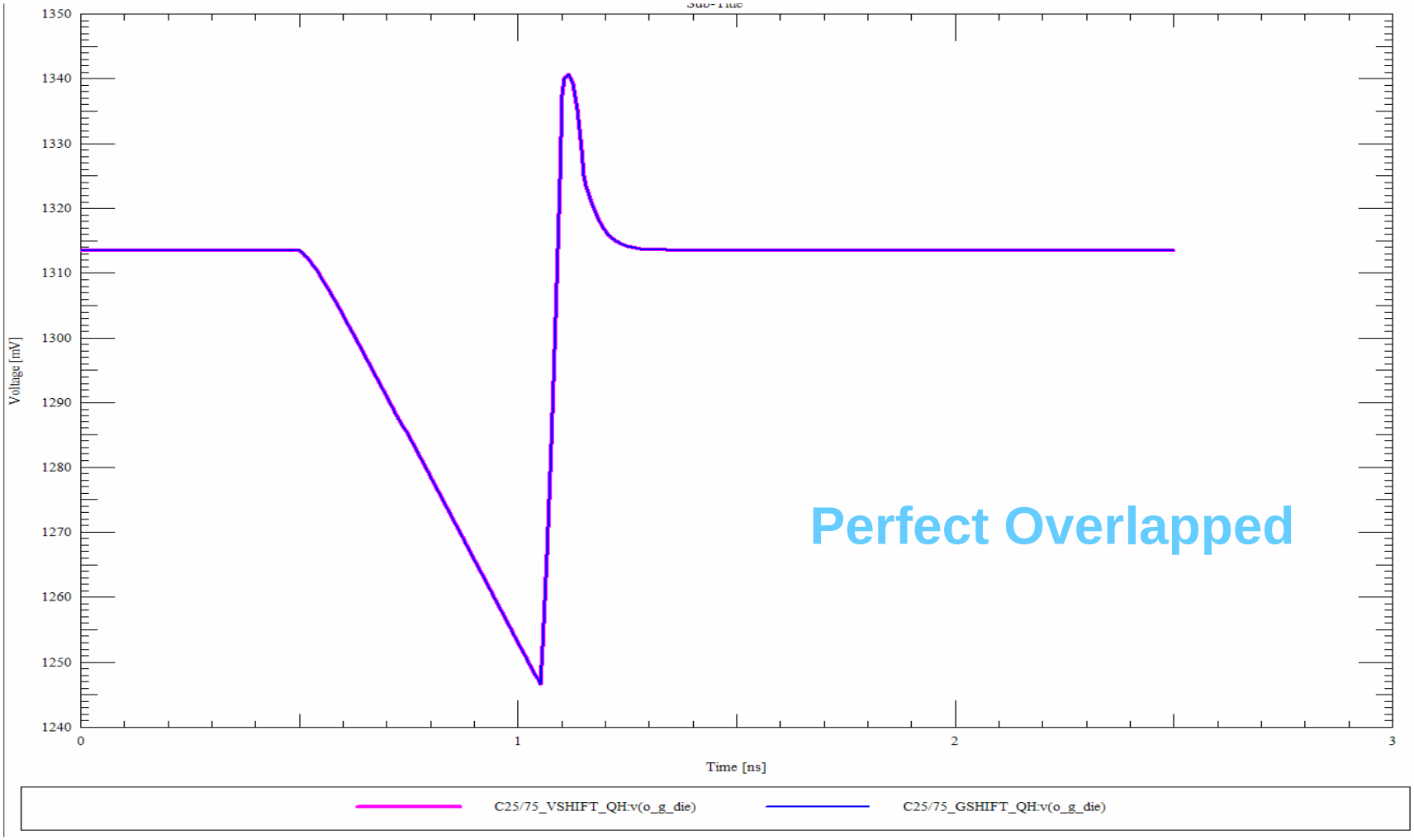
Test Results –IBIS C_Comp_50/50 - Input High-Static



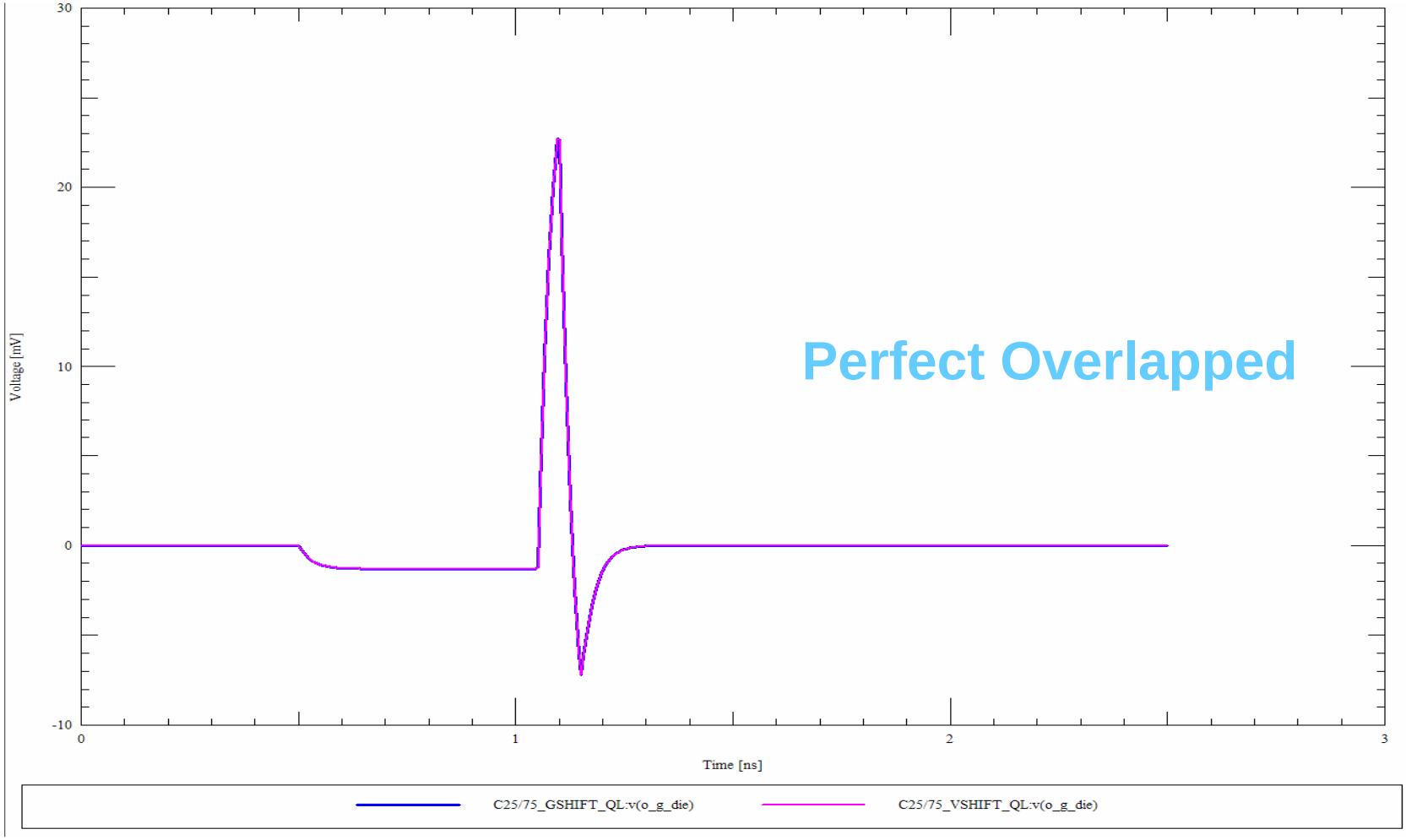
Test Results –IBIS C_Comp_50/50 - Input Low-Static



Test Results –IBIS C_Comp_25/75 - Input High-Static

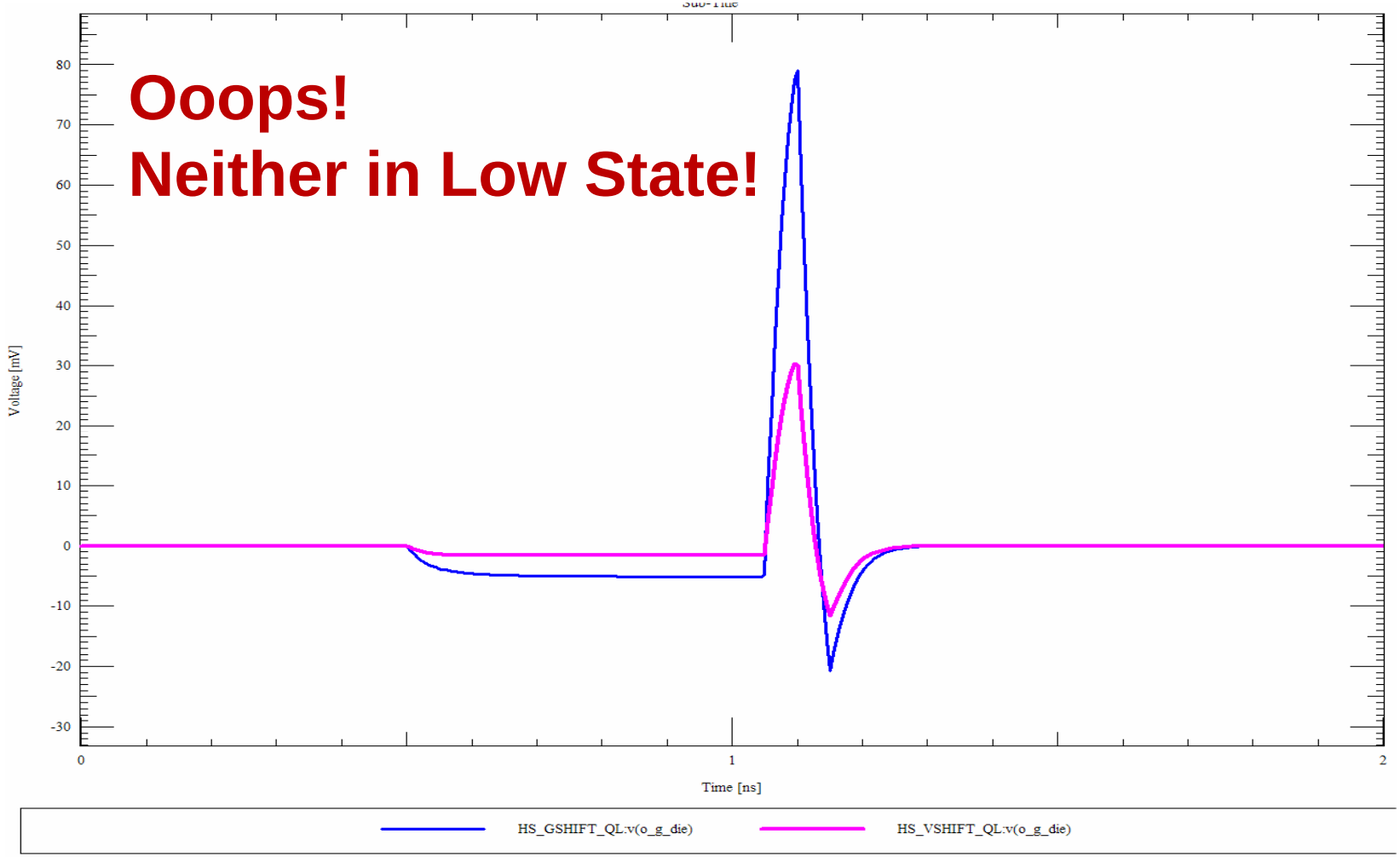


Test Results –IBIS C_Comp_25/75 - Input Low-Static



Test Results –HSpice transistor-level - Input High-Static

Test Results –HSpice transistor-level - Input Low-Static



Conclusions

- IBIS model simulations give the same output currents for Quiet-Lines with Power Supply changes on Buffer Power-node or Buffer Ground-node
- HSpice transistor-level model simulations give the different output currents for Quiet-Lines with Power Supply changes on Buffer Power-node or Buffer Ground-node

Power and Ground parasitic configurations both are needed for using IBIS in non-ideal power supply test cases!!!