



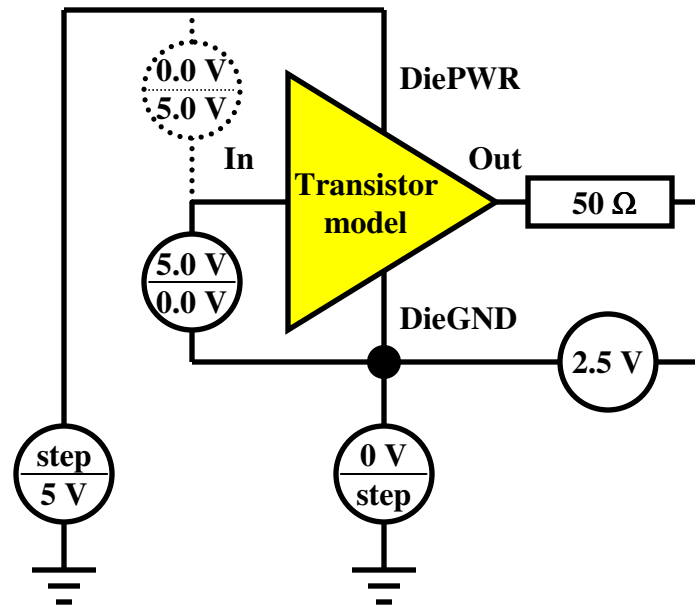
# Quiet line experiment

**IBIS Open Forum Teleconference**

**October 7, 2005**

**Arpad Muranyi**  
**Signal Integrity Engineering**  
**Intel Corporation**  
[arpad.muranyi@intel.com](mailto:arpad.muranyi@intel.com)

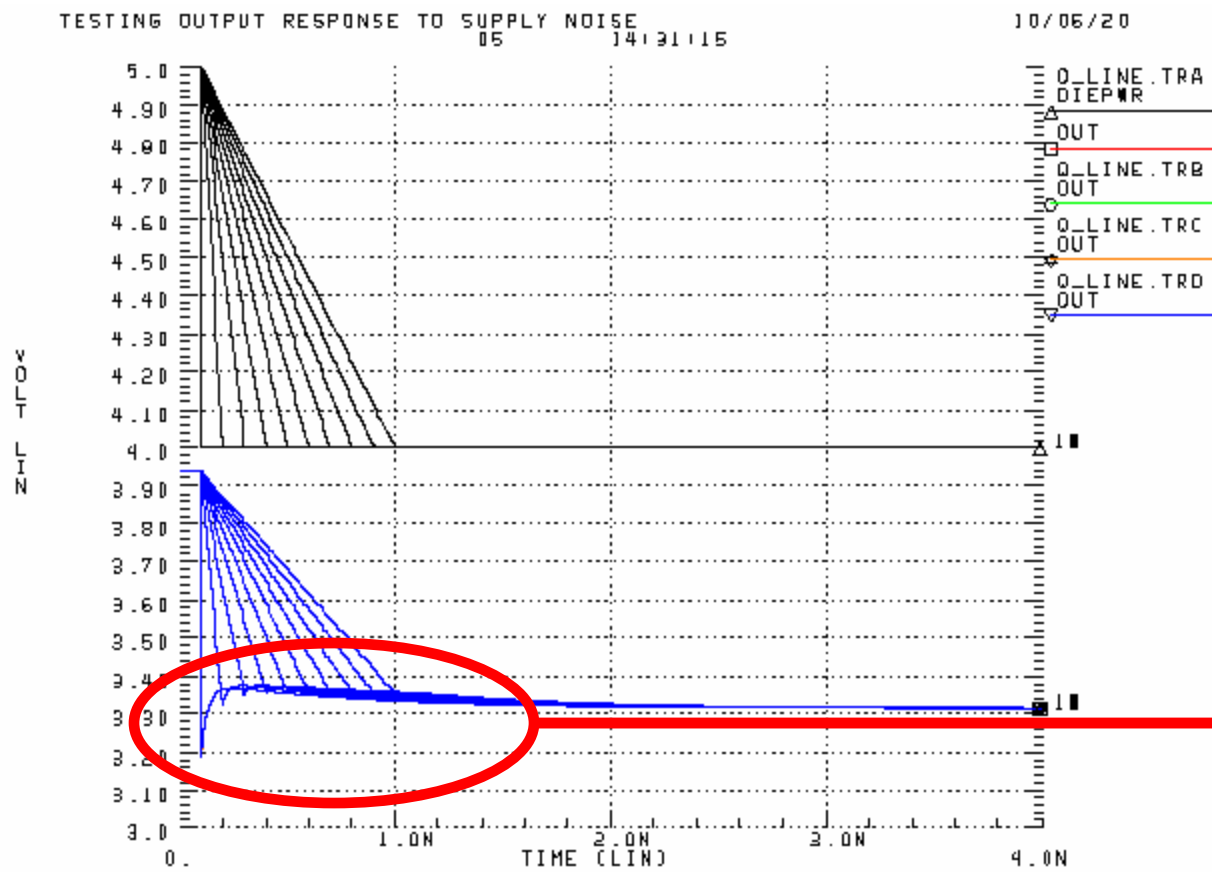
# Simulation circuit using ‘IBIS class’ transistor model



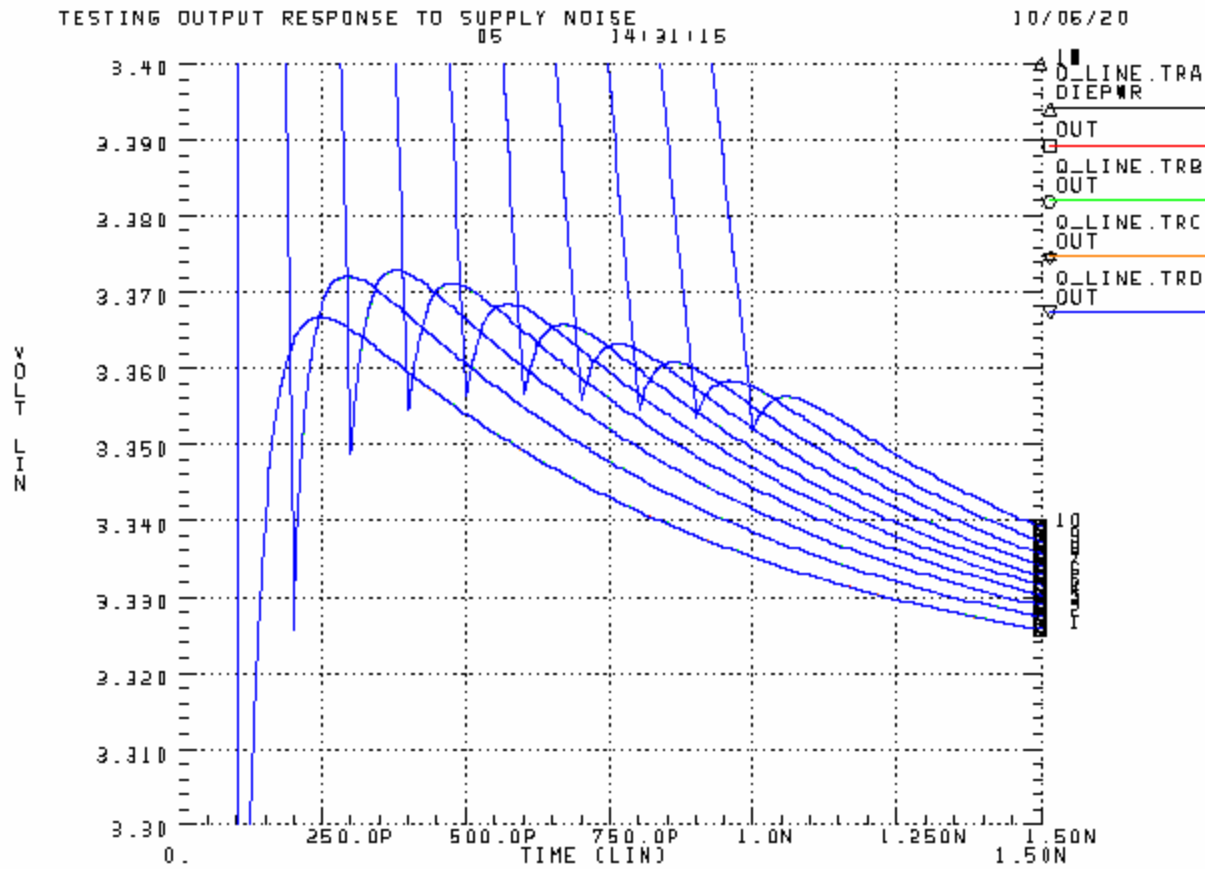
# HSPICE simulation file

```
Testing Output Response to Supply Noise
*****
.OPTIONS POST=1 POST_VERSION=9007 PROBE ACCURATE RMAX=0.5
.TRAN 1.0ps 4.0ns SWEEP Tpoint LIN 10 101e-12 1001e-12
.LIB 'Process.lib' Typ
*****
.PROBE
+ DiePWR = V(DiePWR,DieGND)
+ DieGND = V(DieGND)
+ Out = V(Out,DieGND)
*****
.param Tpoint = 101ps
*
*Vvcc DiePWR 0 DC= 5.0
Vvcc DiePWR 0 PWL
+ 0.0 5.0
+ 0.1ns 5.0
+ Tpoint 4.0
+ 10.0ns 4.0
*
Vgnd DieGND 0 DC= 0.0
*Vgnd DieGND 0 PWL
*+ 0.0 0.0
*+ 0.1ns 0.0
*+ Tpoint 1.0
*+ 10.0ns 1.0
*
Vin In DieGND DC= 5.0
*Vin DiePWR In DC= 0.0
*****
X0 In Out DiePWR DiePWR DieGND DieGND DieGND IO_buf
* in out pu pc pd gc en
*
Rload Out Vtt R= 50.0
Vload Vtt DieGND DC= 2.5
*****
.END
*****
```

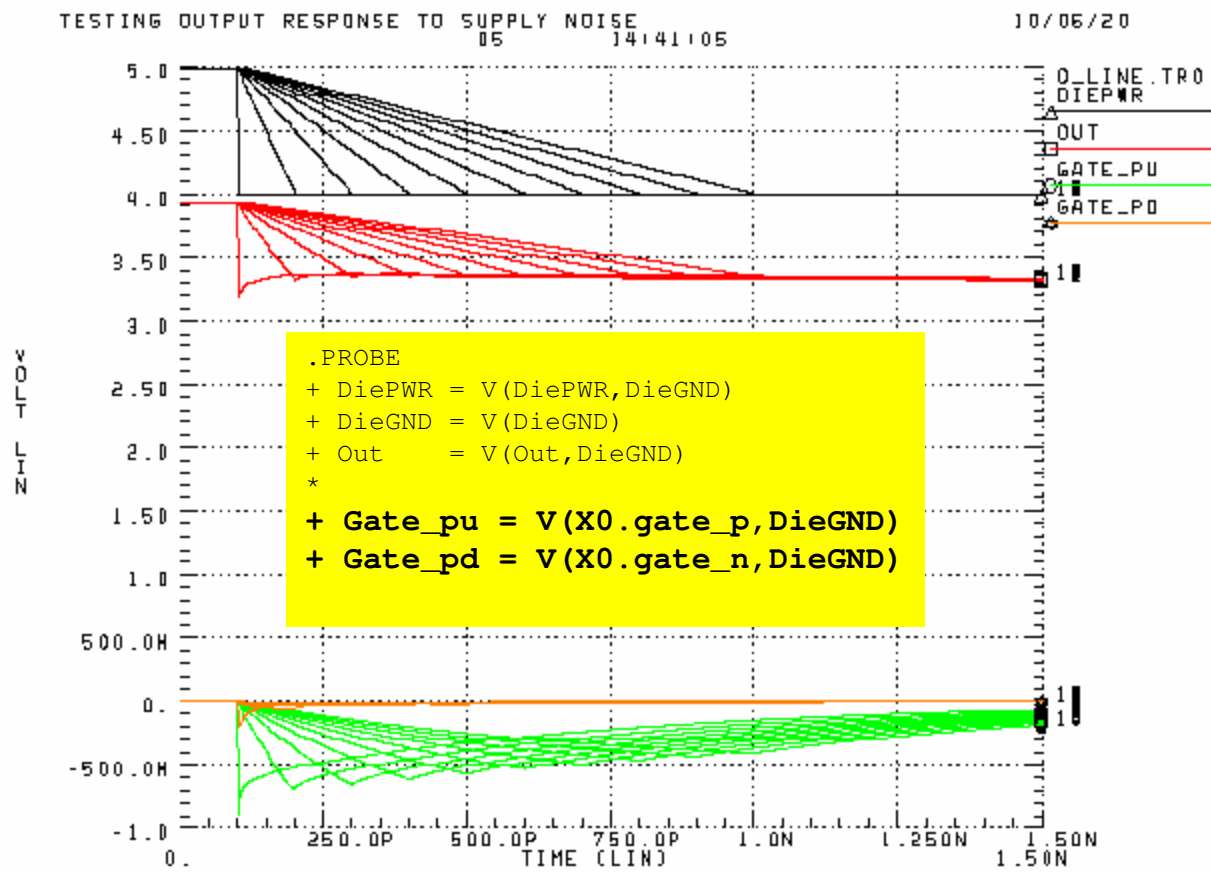
# The four configurations give identical results (high state)



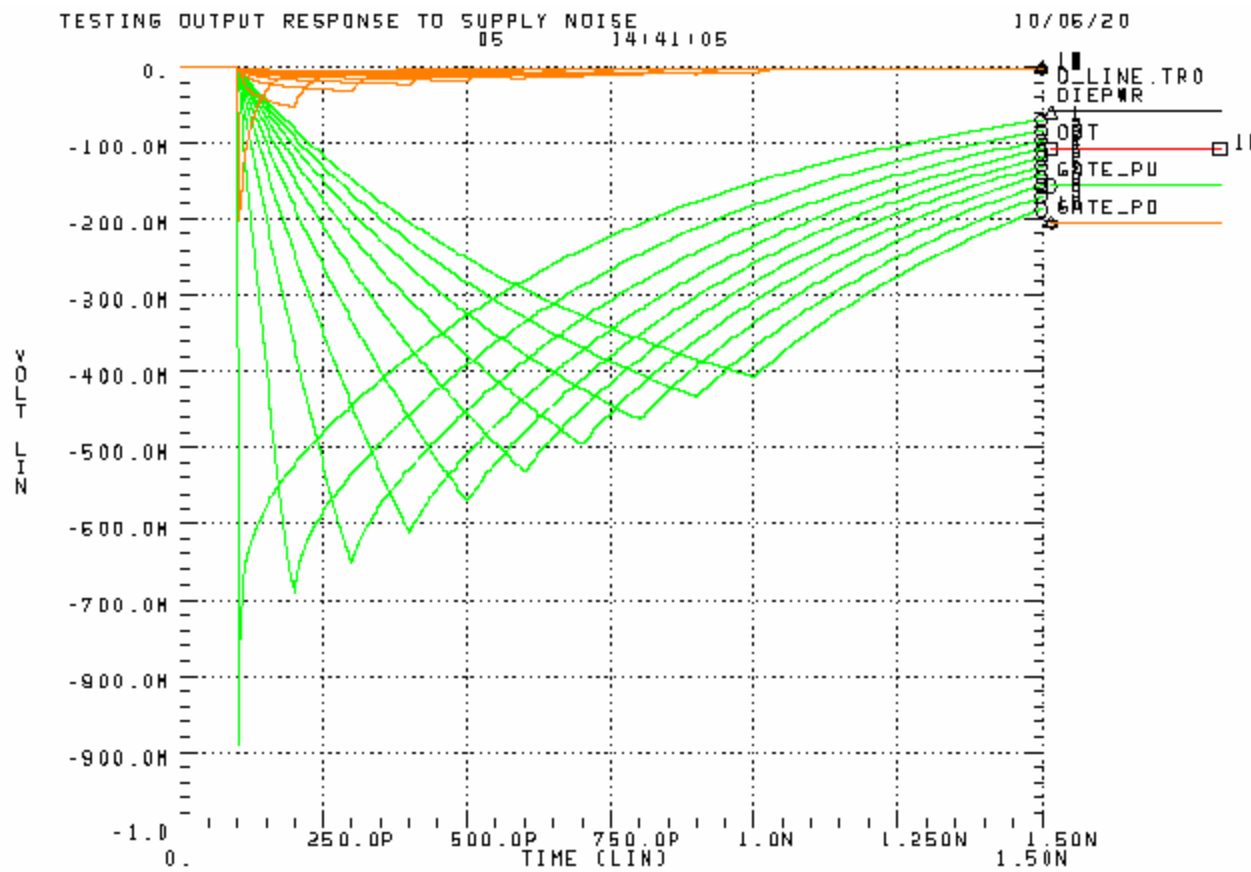
# Zooming in to see the details...



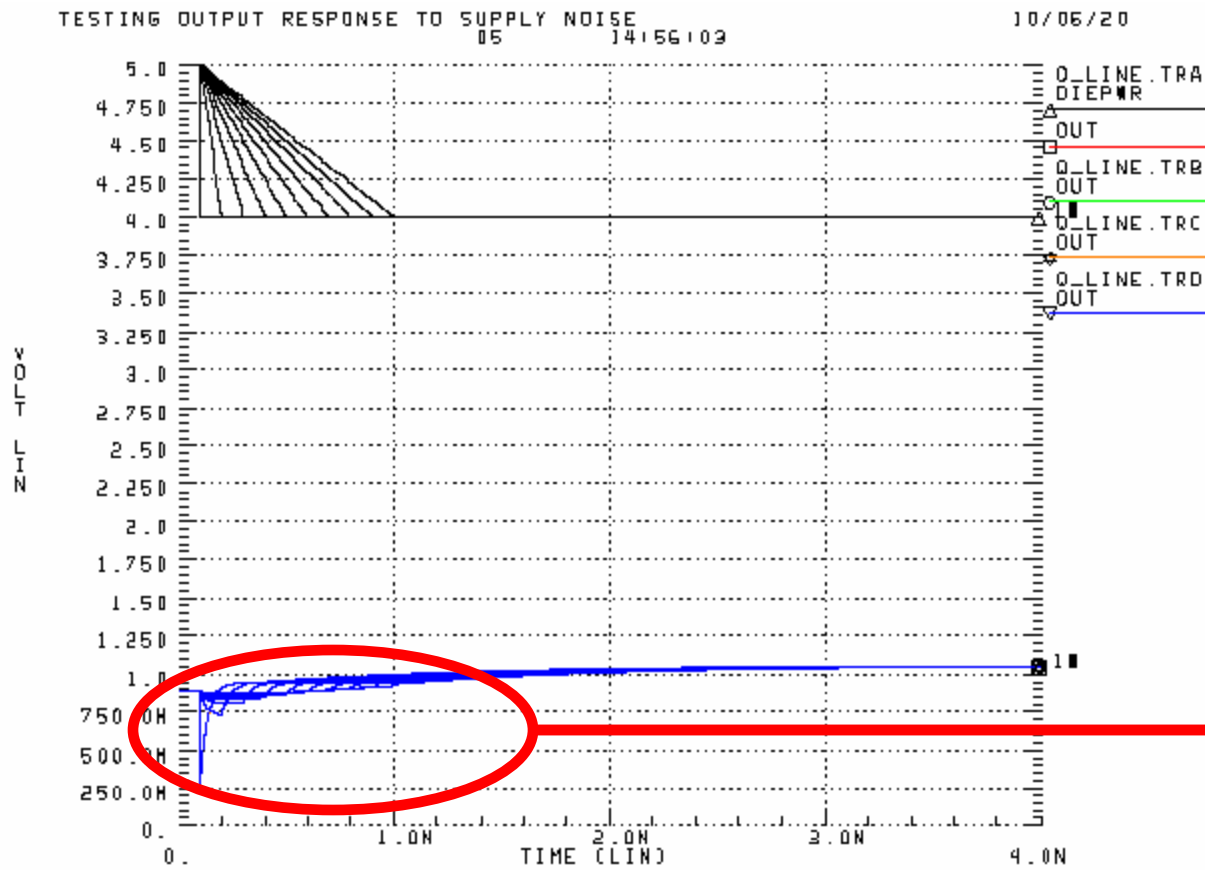
# Gate voltage of the output transistors



# Zooming in to see the details...

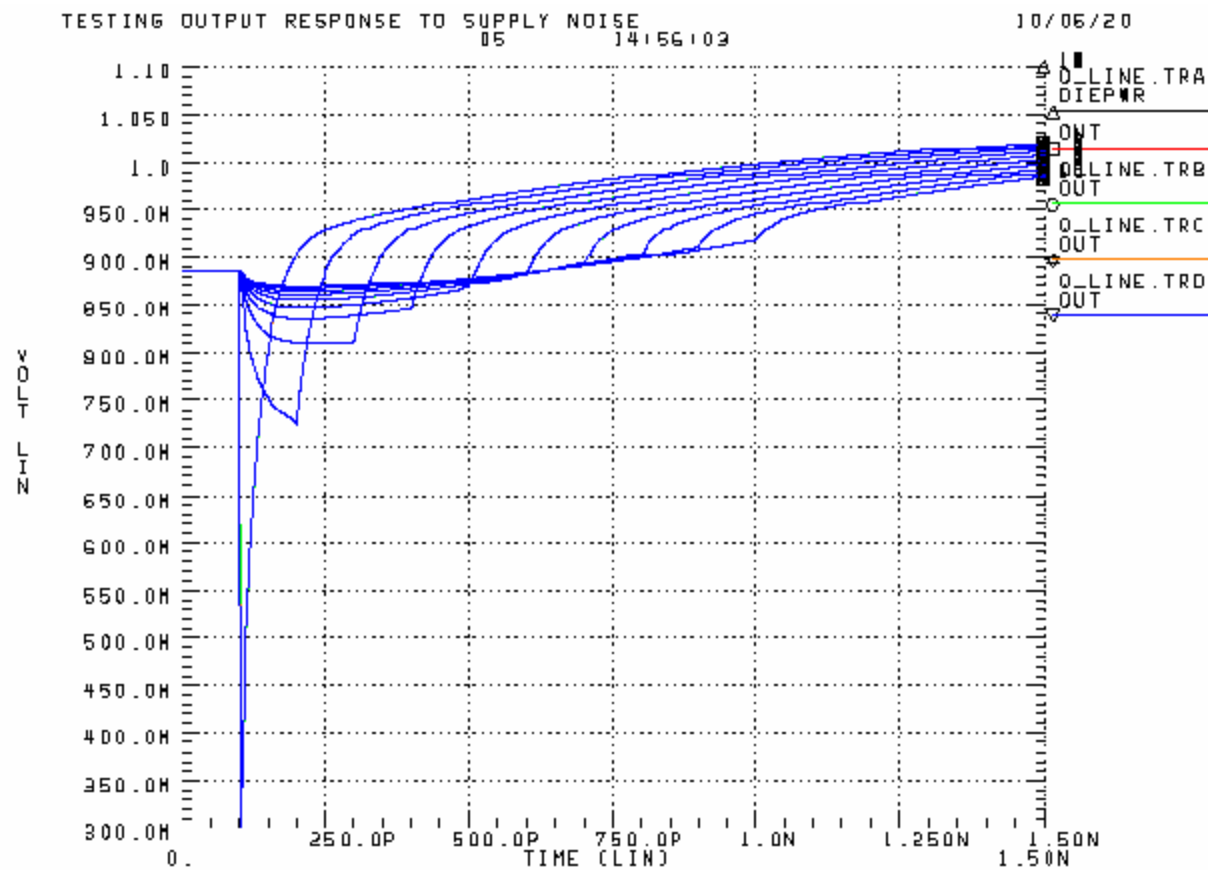


# The four configurations give identical results (low state)

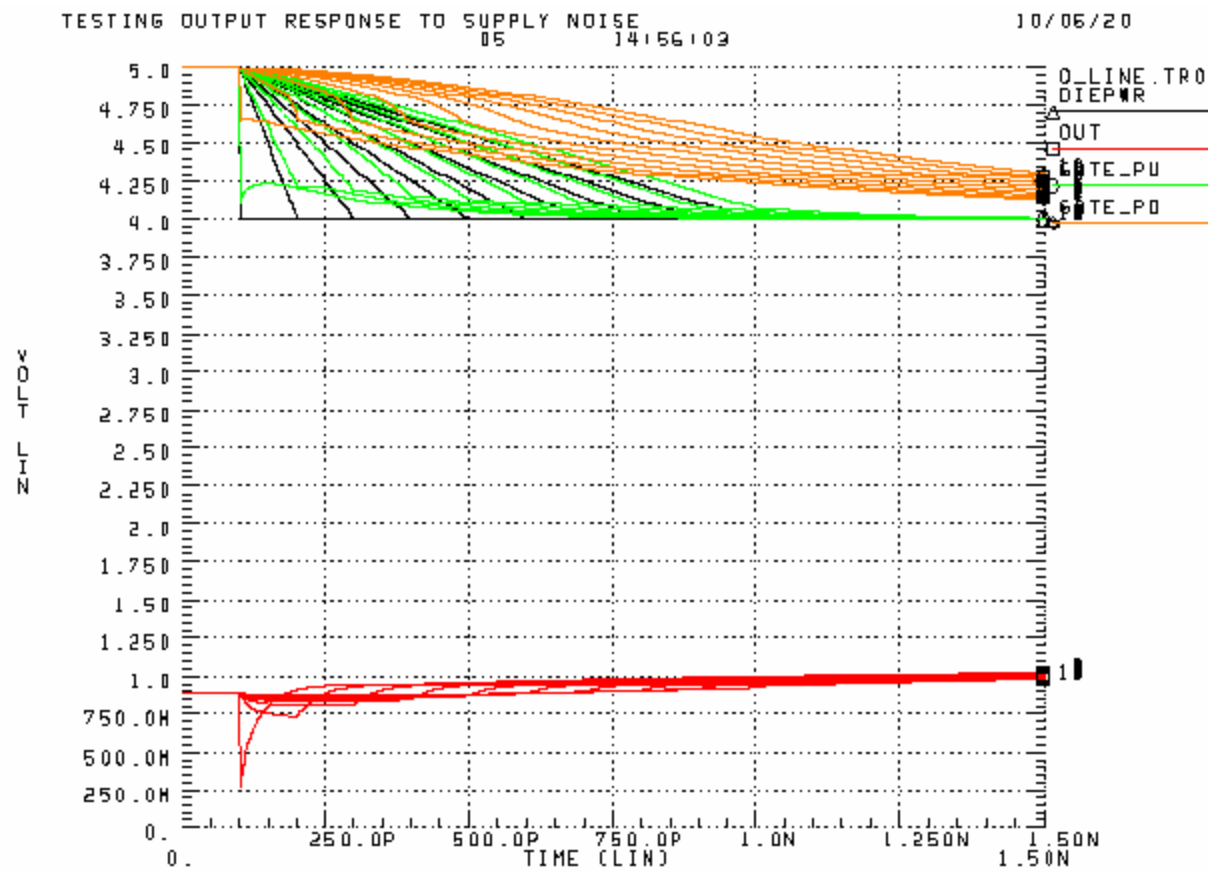




# Zooming in to see the details...



# Gate voltage of the output transistors





# Conclusions

- Whether we are modulating the top or bottom supply voltage **DOES NOT MATTER**
- Due to internal RC effects the gate voltage of the output transistors will not be able to follow rapid supply voltage variations instantaneously
- The gate modulation effect cannot be modeled by DC measurements alone
- We have to find a good way to describe these AC effects in a general way before BIRD97/98 can be completed