Quiet line experiment

IBIS Open Forum Teleconference

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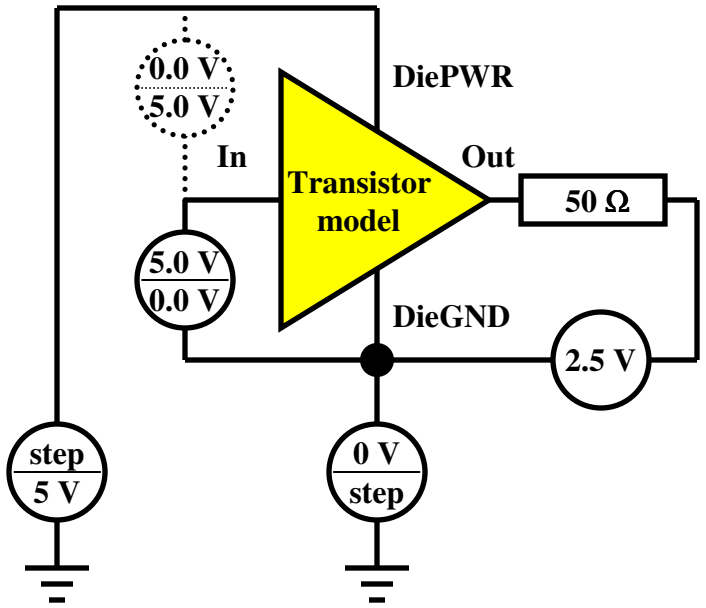
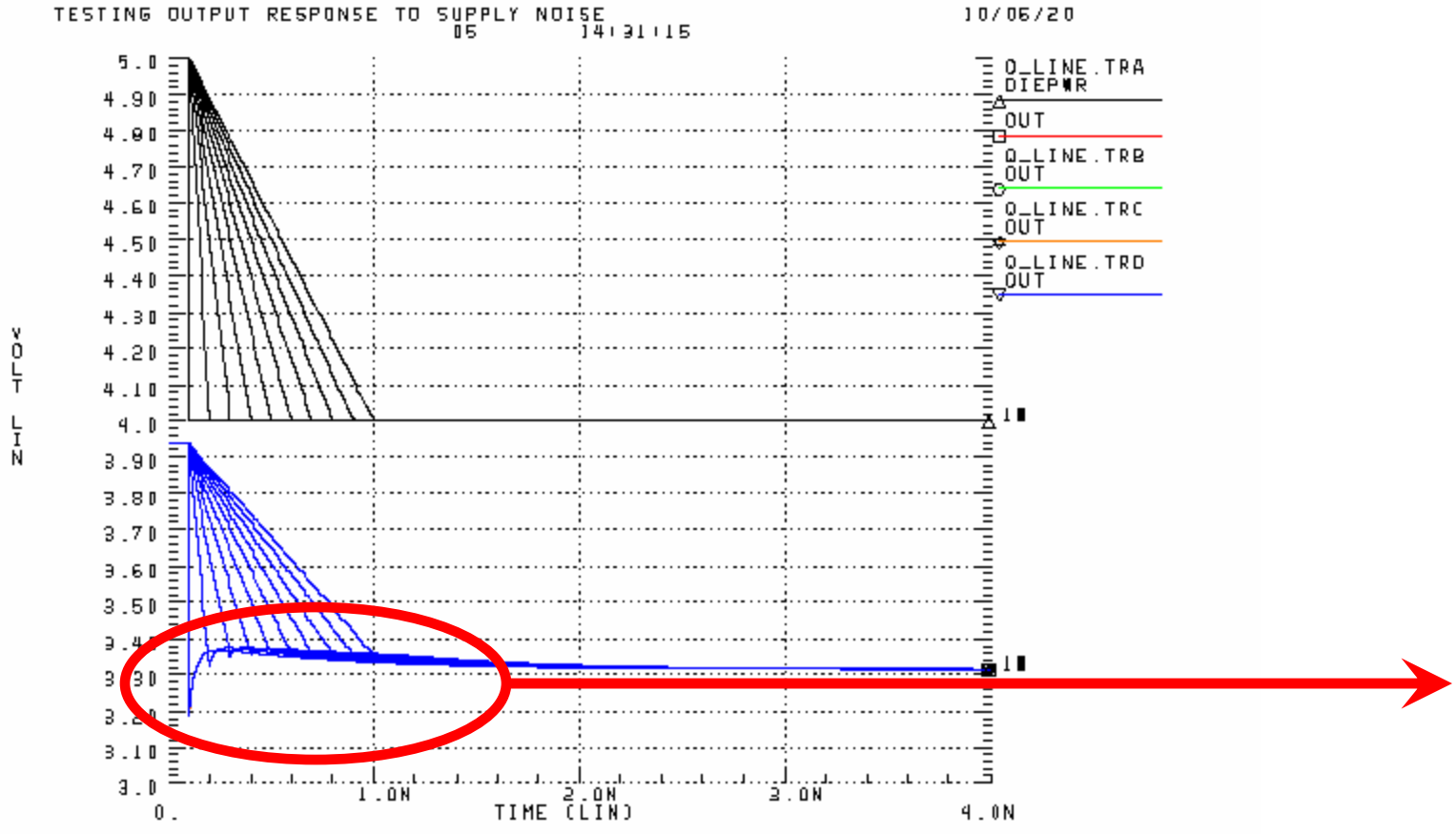
Simulation circuit using “IBIS class” transistor model



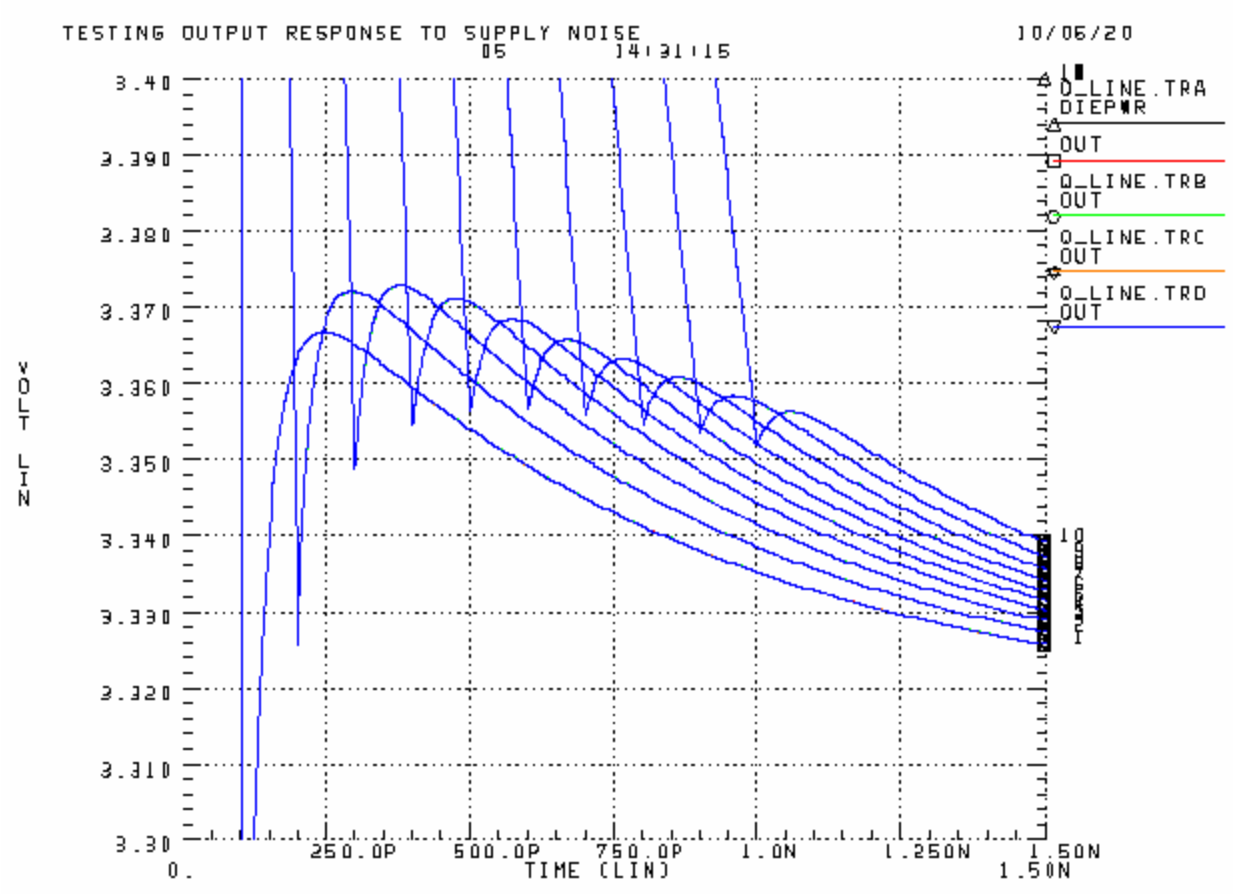
HSPICE simulation file

```
Testing Output Response to Supply Noise
*********************************************************************
.OPTIONS POST=1 POST_VERSION=9007 PROBE  ACCURATE  RMAX=0.5
.TRAN 1.0ps  4.0ns  SWEEP  Tpoint  LIN  10  101e-12 1001e-12
.LIB  'Process.lib'  Typ
*********************************************************************
.PROBE
+ DiePWR = V(DiePWR,DieGND)
+ DieGND = V(DieGND)
+ Out    = V(Out,DieGND)
*********************************************************************
.param Tpoint = 101ps
*
*Vvcc  DiePWR  0  DC= 5.0
Vvcc  DiePWR  0  PWL
+  0.0        5.0
+  0.1ns      5.0
+  Tpoint     4.0
+ 10.0ns      4.0
*
Vgnd  DieGND  0   DC= 0.0
*Vgnd  DieGND  0   PWL
*+  0.0        0.0
*+  0.1ns      0.0
*+  Tpoint     1.0
*+ 10.0ns      1.0
*
Vin   In      DieGND  DC= 5.0
*Vin   DiePWR  In      DC= 0.0
*********************************************************************
X0  In  Out  DiePWR  DiePWR  DieGND  DieGND  DieGND  IO_buf
*   in  out   pu      pc      pd      gc      en
*
Rload  Out  Vtt     R=  50.0
Vload  Vtt  DieGND  DC=  2.5
*********************************************************************
.END
*********************************************************************
```

The four configurations give identical results (high state)



Zooming in to see the details…



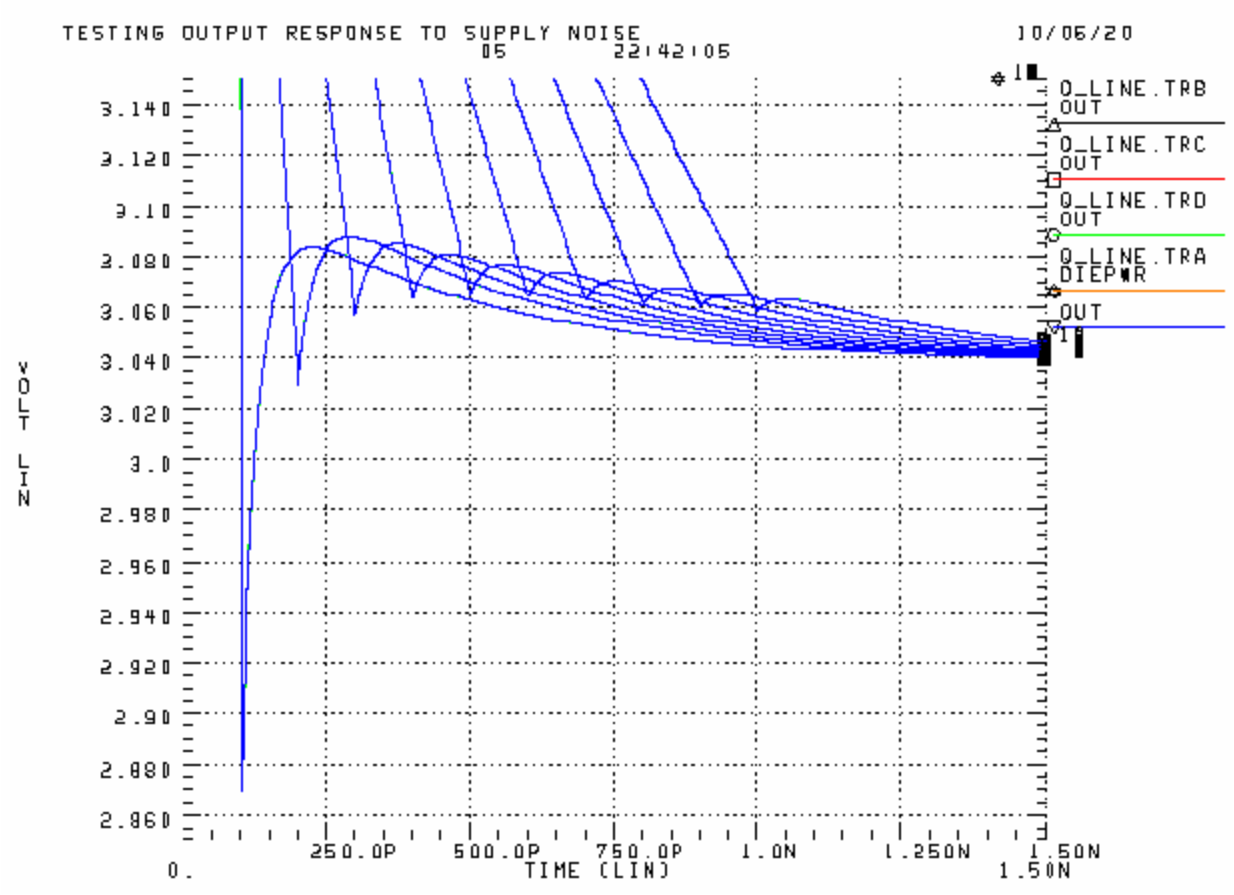
Make the PU and PD asymmetric

```
*********************************************************************************
.SUBCKT  IO_buf  d_in pad DiePWR p_clamp DieGND g_clamp enable
*********************************************************************************
X1  enable  en_b            DiePWR  DieGND  INVERTER
X2  d_in    en_b    pre_p1  DiePWR  DieGND  NAND2
X3  d_in    enable  pre_n1  DiePWR  DieGND  NOR2
X4  pre_p1  pre_p2          DiePWR  DieGND  INVERTER  mult_p=2  mult_n=2
X5  pre_n1  pre_n2          DiePWR  DieGND  INVERTER  mult_p=2  mult_n=2
X6  pre_p2  pre_p2  gate_p  DiePWR  DieGND  NAND2     mult_p=4  mult_n=2
X7  pre_n2  pre_n2  gate_n  DiePWR  DieGND  NOR2      mult_p=2  mult_n=4
*
Mp  pad gate_p DiePWR  p_clamp  PMOS  L=0.800U W=43.40U NRD=0.0897 NRS=0.0737
+                              AS=434.0P AD=217.0P PS=106.8U PD=53.40U
+                              M=12
Mn  pad gate_n DieGND g_clamp  NMOS  L=0.800U W=43.40U NRD=0.0897 NRS=0.0714
+                              AS=434.0P AD=217.0P PS=106.8U PD=53.40U
+                              M=6
*C1  pre_p2  DieGND  C=0.07pF
*C2  pre_n2  DieGND  C=0.07pF
*C3  gate_p  DieGND  C=0.04pF
*C4  gate_n  DieGND  C=0.03pF
*
R1  pad     rcv_in  R=200
*C5  rcv_in  DieGND  C=0.2pF
X8  rcv_in  rcv_out         DiePWR  DieGND  INVERTER
*
```

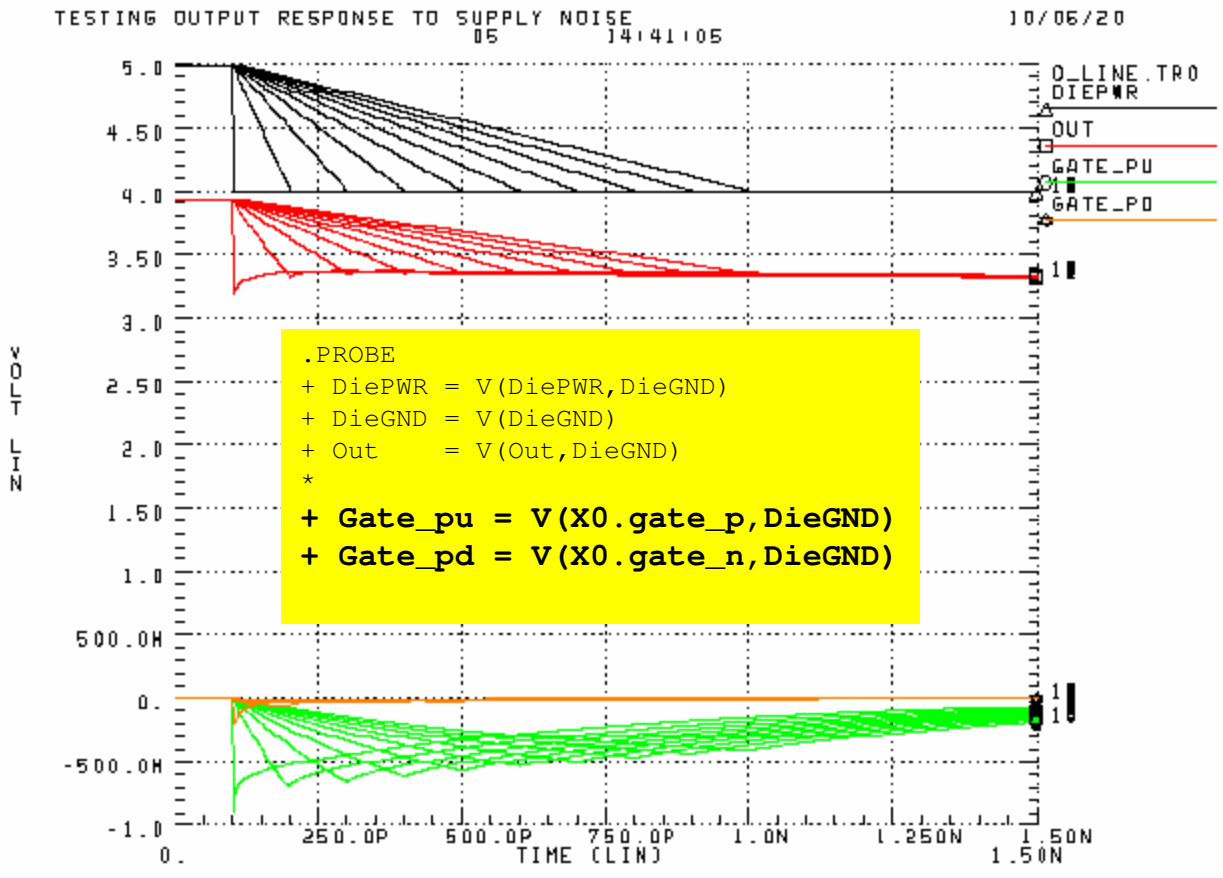
Chaged to M=6 to make PU and PD asymmetric

Adding or removing these capacitors doesn't make the agreement between the four conditions any weaker

PU reduced to half the strength - High state



Gate voltage of the output transistors



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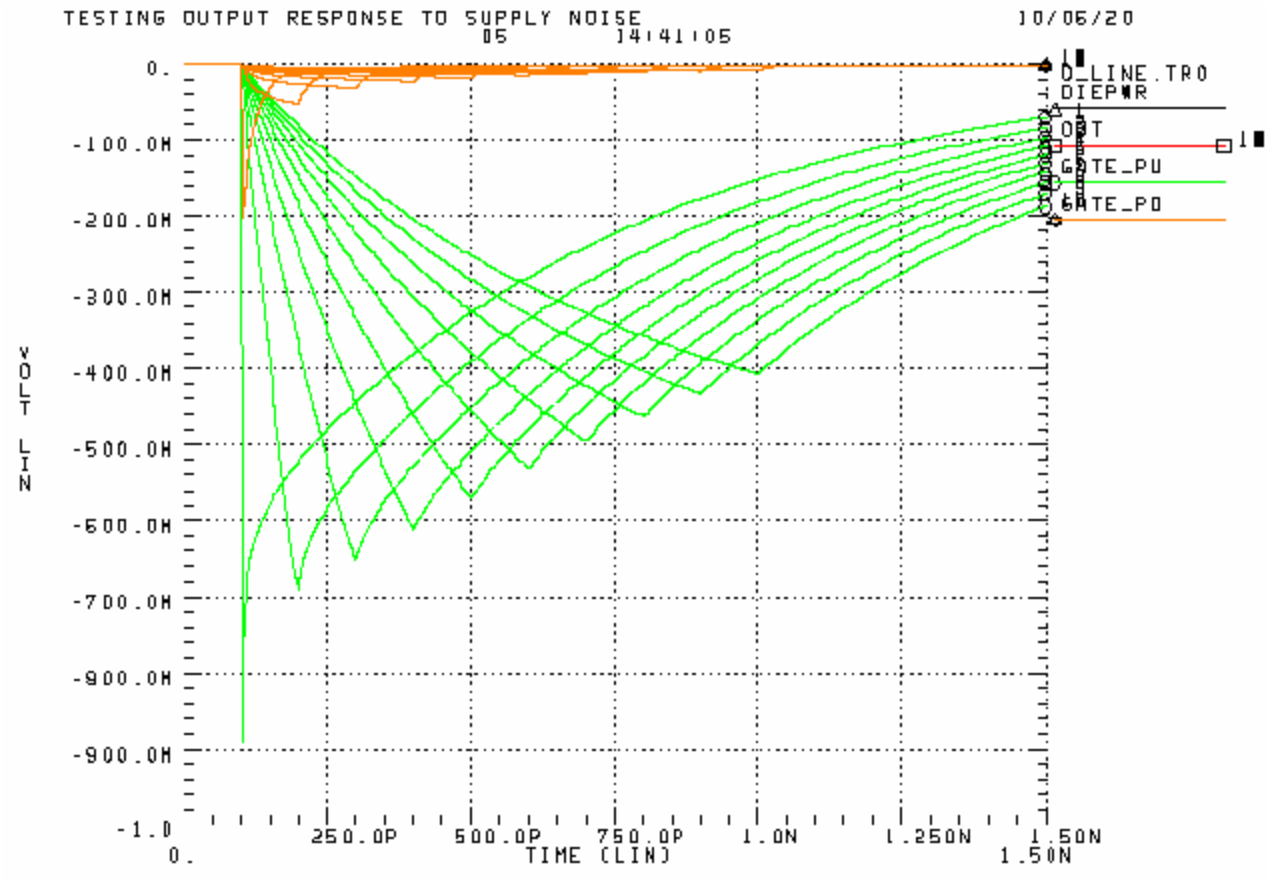
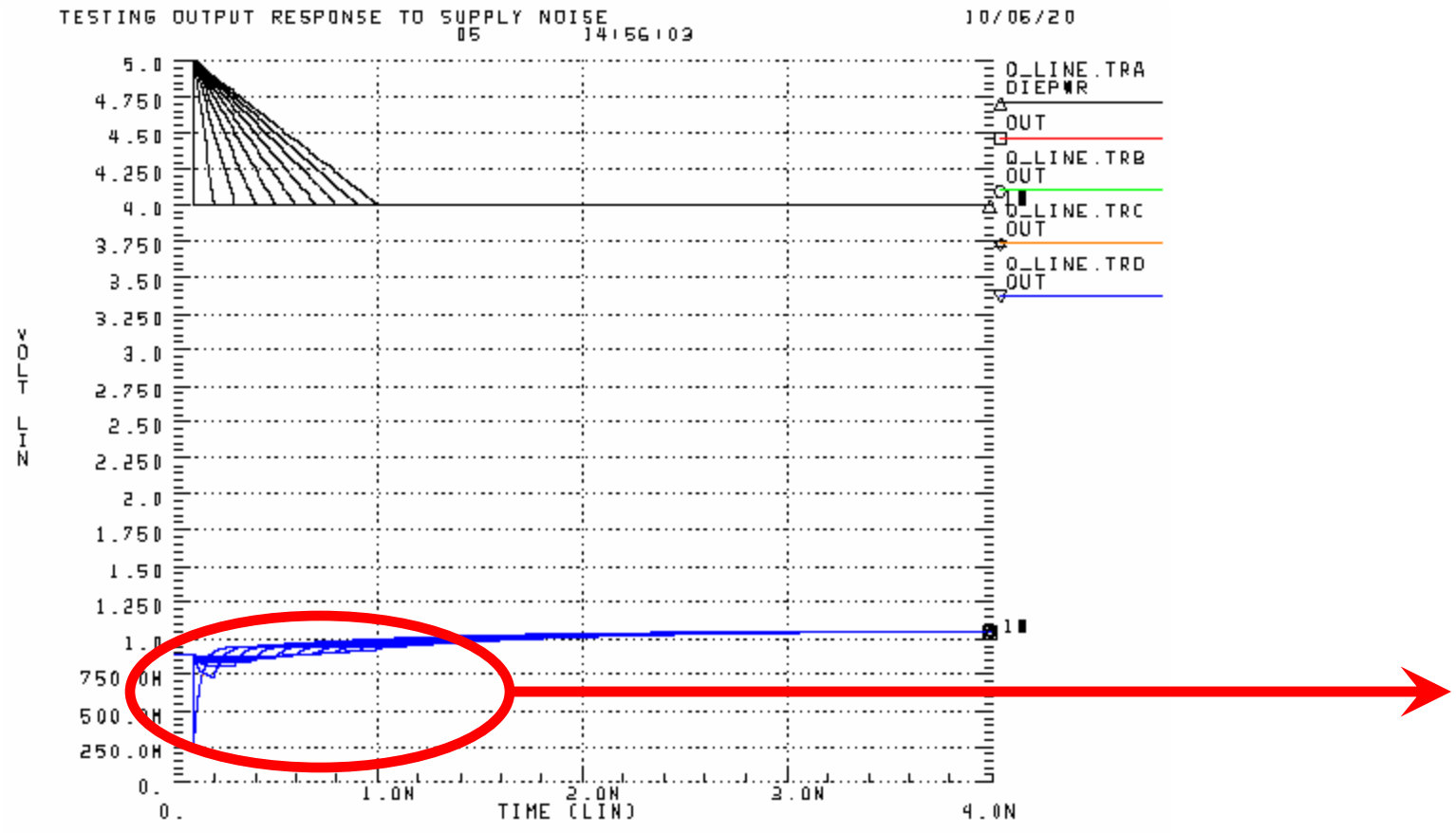


The four configurations give identical results (low state)



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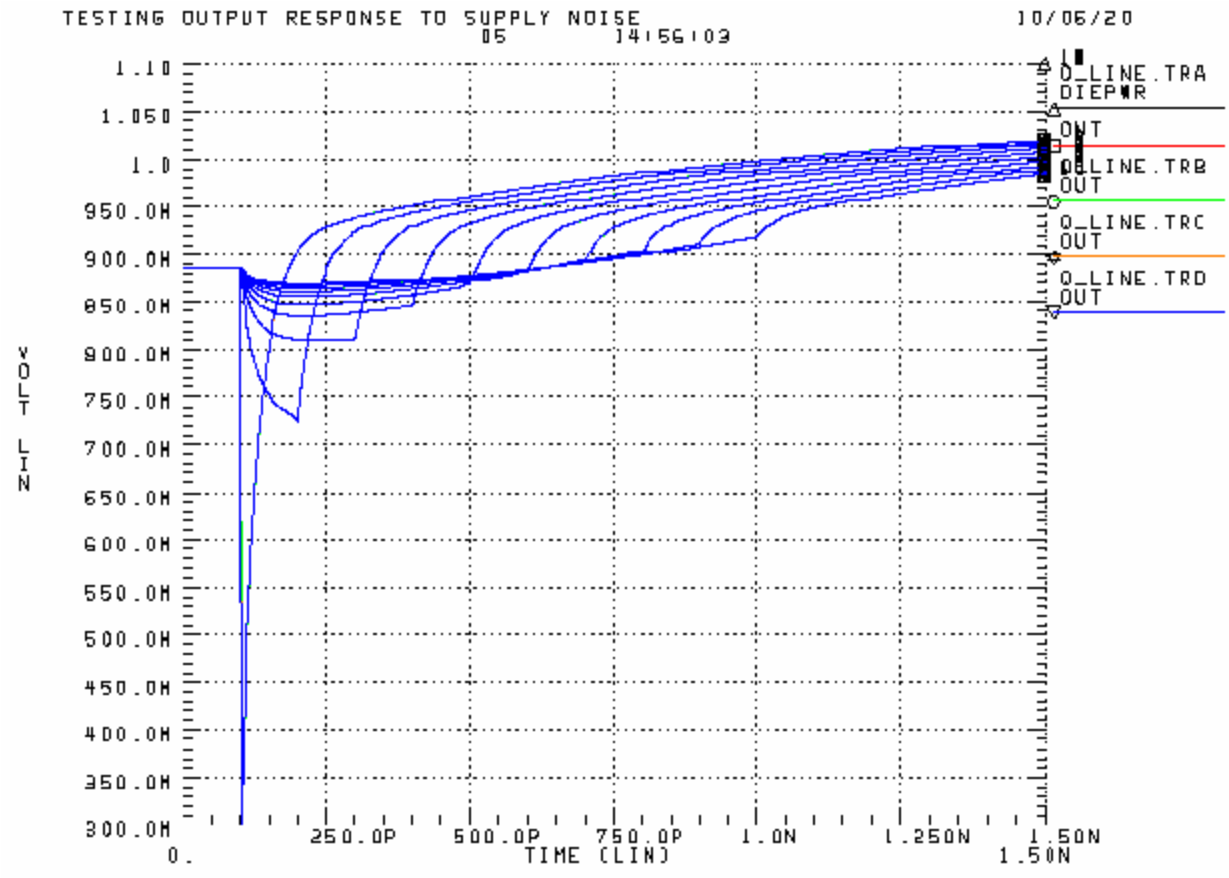
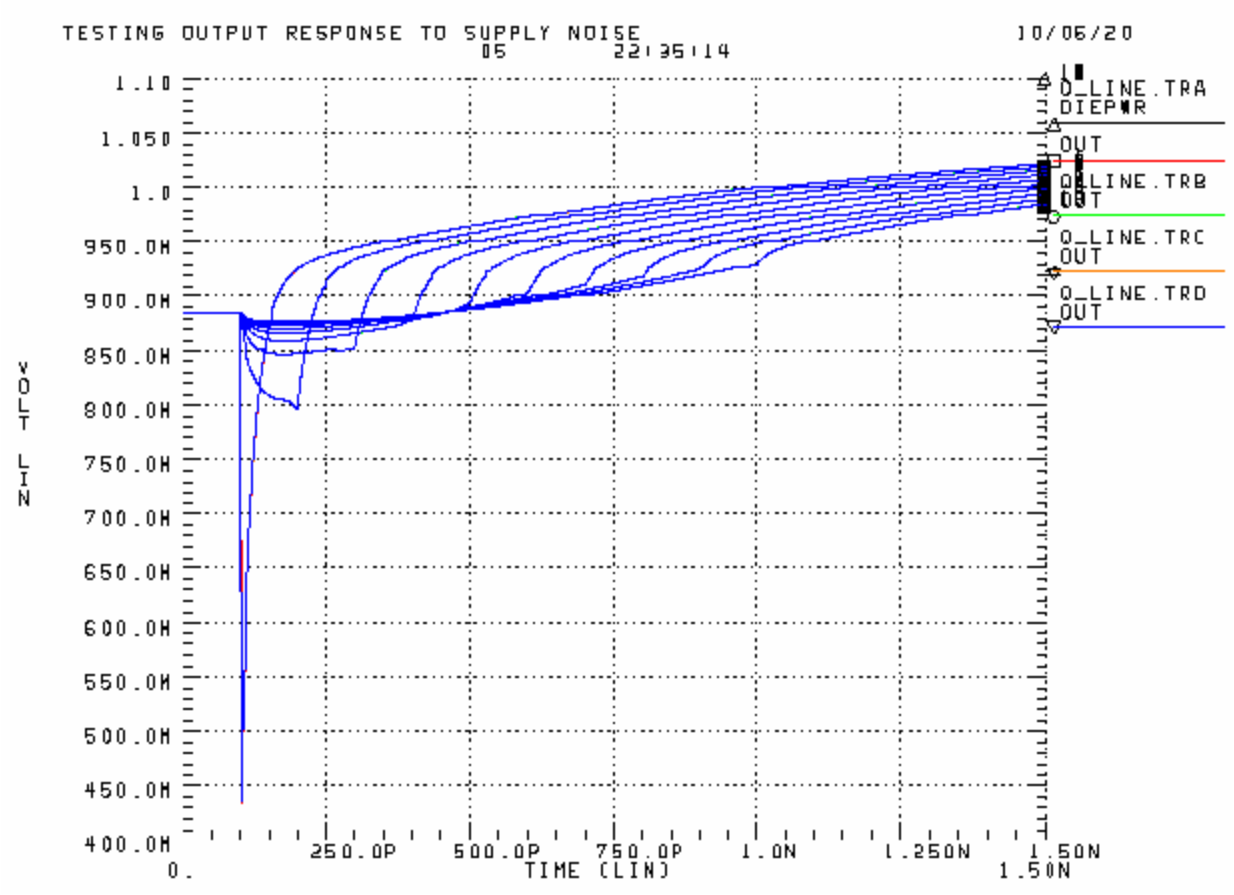
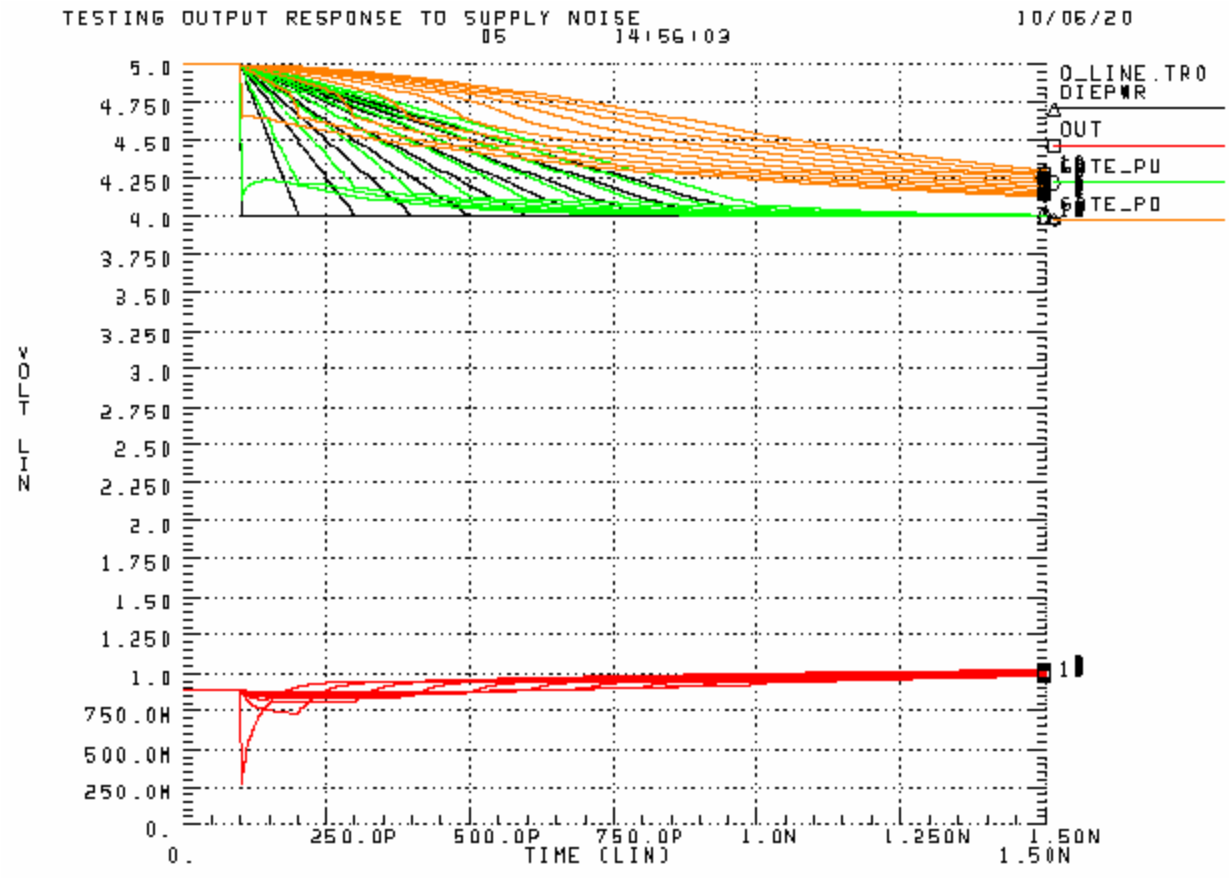


PU reduced to half the strength - Low state



Gate voltage of the output transistors



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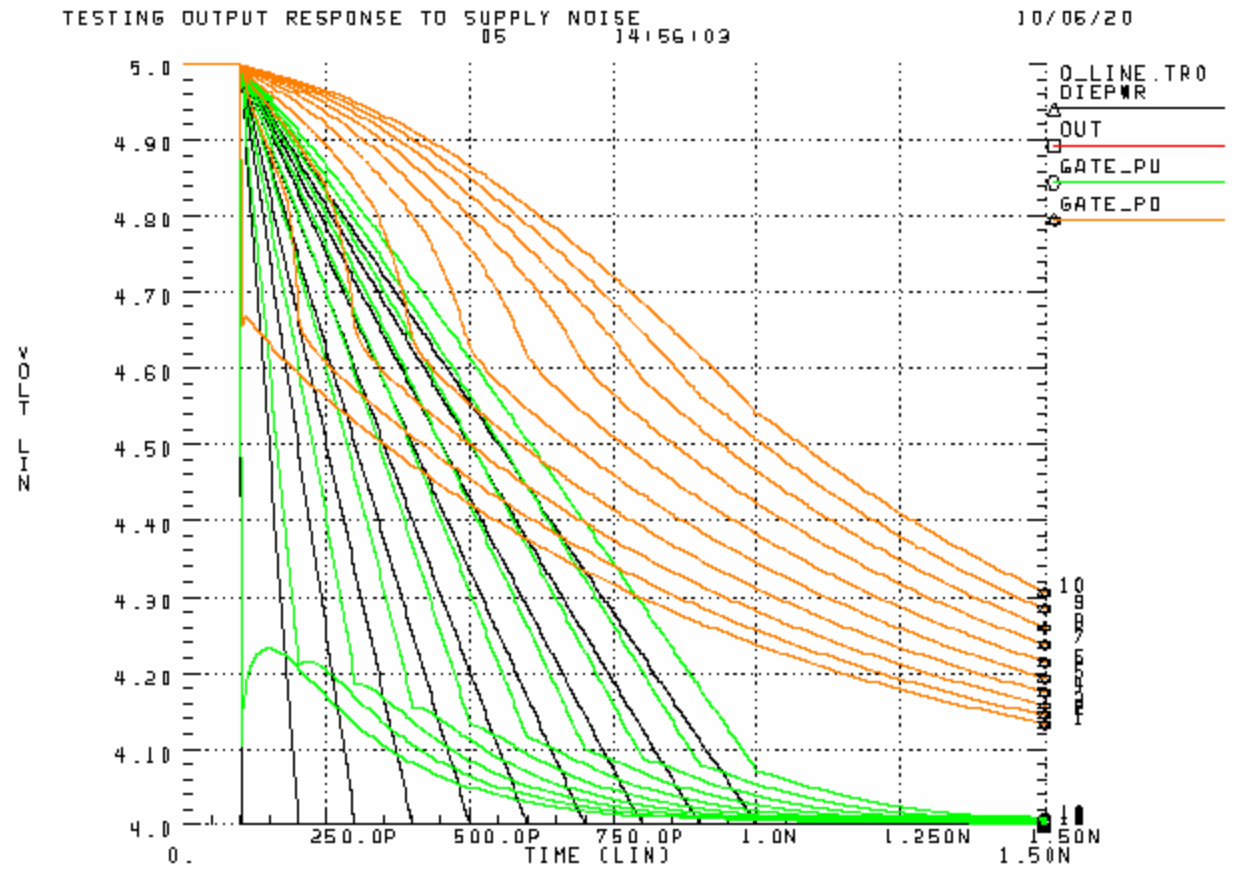

Conclusions

- **Whether we are modulating the top or bottom supply voltage *DOES NOT MATTER***
- **Due to internal RC effects the gate voltage of the output transistors will not be able to follow rapid supply voltage variations instantaneously**
- **The gate modulation effect cannot be modeled by DC measurements alone**
- **We have to find a good way to describe these AC effects in a general way before BIRD97/98 can be completed**